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1.8 /2.5 ,10 2 D d M L

Multi–Level Inputs w/ Internal Termination

B7 32M

Description

The NB7V32M is a differential $\div 2$ Clock divider with asynchronous reset. The differential Clock inputs incorporate internal 50 Ω termination resistors and will accept LVPECL, CML and LVDS logic levels.

The NB7V32M produces a \div 2 output copy of an input Clock operating up to 10 GHz with minimal jitter.

The RESET Pin is asserted on the rising edge. Upon power up, the internal flip flops will attain a random state; the Reset allows for the synchronization of multiple NB7V32M's in a system.

The 16 mA differential CML output provides matching internal 50 Ω termination which guarantees 400 mV output swing when externally receiver terminated with 50 Ω to V_{CC} .

The NB7V32M is the 1.8 V/2.5 V version of the NB7L32M (2.5 V/3.3 V) and is offered in a low profile 3 mm x 3 mm 16 pin QFN package. The NB7V32M is a member of the GigaComm family of high performance clock products. Application notes, models, and support documentation are available at www.onsemi.com.

Features

Maximum Input Clock Frequency > 10 GHz, typical Random Clock Jitter < 0.8 ps RMS 200 ps Typical Propagation Delay 35 ps Typical Rise and Fall Times Differential CML Outputs, 400 mV Peak to Peak, Typical Operating Range: $V_{CC} = 1.71$ V to 2.625 V with GND = 0 V Internal 50 Ω Input Termination Resistors QFN 16 Package, 3 mm x 3 mm 40 C to +85 C Ambient Operating Temperature These Devices are Pb Free and RoHS Compliant A L Y

= Wafer Lot = Year

= Assembly Location

NB7V32M

	VCC	R	VCC	VCC			
	16	15	14	13			
VTCLK					12	VCC	
CLK						Q	
CLK						Q	
						VCC	

5 6 7 8 VREFAC GND GND GND

Table 3. ATTRIBUTES

Characteristics	Value	
ESD Protection Human Body Model Machine Model	> 4 kV > 200 V	
Moisture Sensitivity 16–QFN	Level 1	
Flammability Rating Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in	
Transistor Count	164	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	GND = 0 V		3.0	V
V _{IN}	Positive Input Voltage	GND = 0 V		–0.5 to V _{CC} + 0.5 V	V
V _{INPP}	Differential Input Voltage D – D			1.89	V
I _{IN}	Input Current Through R_T (50 Ω Resistor)			40	mA
I _{OUT}	Output Current Through R_T (50 Ω Resistor)			40	mA
IVREFAC	VREFAC Sink/Source Current			1.5	mA
T _A	Operating Temperature Range			-40 to +85	С
T _{stg}	Storage Temperature Range			-65 to +150	С
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 lfpm 500 lfpm	QFN–16 QFN–16	42 35	C/W C/W
θJC	Thermal Resistance (Junction-to-Case) (Note 3)		QFN-16	4	C/W
T _{sol}	Wave Solder Pb-Free			265	С

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS POSITIVE CML OUTPUT V _{CC} =	1.71 V to 2.625 V; GND = 0 V; $T_A = -40$ C to 85 C (Note 4)
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Symbol	Characteristic		Min	Тур	Max	Unit
POWER	SUPPLY CURRENT					
I _{CC}	Power Supply Current (Inputs and Outputs Open)	/ _{CC} = 2.5 V 5% / _{CC} = 1.8 V 5%		90 80	100 90	mA
CML OU	TPUTS					
V _{OH}	Output HIGH Voltage (Note 5)	V _{CC} = 2.5 V V _{CC} = 1.8 V				

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SCALE 2:1







NOTE 3

BOTTOM VIEW



QFN16 3x3, 0.5P CASE 485G ISSUE G

	° XXXXX XXXXX	
XXXXX	= Specific De	vice Co
А	= Assembly I	ocation
L	= Wafer Lot	

Code

L = Year Υ

- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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