

# **72.5 V**, 10 GH ÷4 Cl ck h CML O.

#### Multi-Level Inputs w/ Internal Termination

## NB7V33M

#### Description

The NB7V33M is a differential ÷4 Clock divider with asynchronous reset. The differential Clock inputs incorporate internal 4 output copy of an input Hz with minimal jitter. The Reset pin is

Upon powerup, the internal flip – flops be Reset allows for the synchronization of

system. The 16 mA differential CML ternal 50  $\Omega$  termination which guarantees externally receiver terminated with 50  $\Omega$ 

= Assembly Location L = Wafer Lot

= Year

= Work Weeh.45hese t9S7s4Jpp5110e0D12 0 0 1

The NB7 $\sqrt{33}$ M is the  $\div 4$  version of the NB7 $\sqrt{32}$ M ( $\div 2$ ) and is offered in a low profile 3 mm x 3 mm 16 pin QFN package.

The NB7 /33M is a member of the GigaComm<sup>™</sup> family of high performance clock products. Application notes, models, and support documentation are available at www.onsemi.com.

- Maximum Input Clock Frequency > 10 GHz, typical
- 260 ps Typical Propagation Delay
- 35 ps Typical Rise and Fall Times
- Differential CML Outputs, 400 mV Peak to Peak, Typical
- Operating Range:  $V_{CC} = 1.71 \text{ V}$  to 2.625 V with GND = 0 V
- nternal 50  $\Omega$  Input Termination Resistors
- Random Clock Jitter < 0.8 ps RMS
- QFN 16 Package, 3 mm x 3 mm
- 40°C to +85°C Ambient Operating Temperature
- These are Pb Free Devices

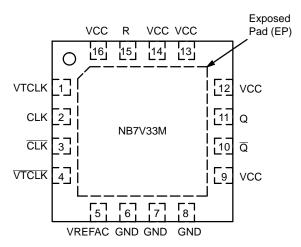


Figure 2. Pin Configuration (Top View)

# Table 1. TRUTH TABLE

Table 5. DC CHARACTERISTICS POSITIVE CML OUTPUT  $V_{CC} = 1.71 \text{ V}$  to 2.625 V; GND = 0 V;  $T_A = -40 ^{\circ}\text{C}$  to  $85 ^{\circ}\text{C}$  (Note 5)

Symbol	Characteristic		Min	Тур	Max	Unit
POWER	SUPPLY CURRENT					
I <sub>CC</sub>		CC = 2.5 V ± 5% CC = 1.8 V ± 5%		95 85	115 100	mA
CML OU	TPUTS					
V <sub>OH</sub>	Output HIGH Voltage (Note 6)	VCC = 2.5 V VCC = 1.8 V	V <sub>CC</sub> – 30 2470 1770	V <sub>CC</sub> - 10 2490 1790	V <sub>CC</sub> 2500 1800	mV
V <sub>OL</sub>	Output LOW Voltage (Note 6)	Vcc = 2.5 V Vcc = 1.8 V	V <sub>CC</sub> - 650 1850 V <sub>CC</sub> - 600 1200	V <sub>CC</sub> - 550 1950 V <sub>CC</sub> - 500 1300	V <sub>CC</sub> - 450 2050 V <sub>CC</sub> - 400 1400	mV
DIFFERE	ENTIAL INPUTS DRIVEN SINGLE-ENDED (Note 7) (Fig	ures 5 & 6)				
$V_{th}$	Input Threshold Reference Voltage Range (Note 8)		1050		V <sub>CC</sub> – 100	mV
$V_{IH}$	Single-ended Input HIGH Voltage		V <sub>th</sub> + 100		V <sub>CC</sub>	mV
$V_{IL}$	Single-ended Input LOW Voltage		GND		V <sub>th</sub> – 100	mV
$V_{ISE}$	Single-ended Input Voltage (V <sub>IH</sub> - V <sub>IL</sub> )		200		1200	mV
VREFAC						
V <sub>REFAC</sub>	Output Reference Voltage @100 μA for Capacitor- Cou	upled Inputs, Only $V_{CC} = 2.5 \text{ V}$ $V_{CC} = 1.8 \text{ V}$	V <sub>CC</sub> - 850 V <sub>CC</sub> - 750		V <sub>CC</sub> - 500 V <sub>CC</sub> - 450	mV
DIFFERE	ENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 7	& 8) (Note 9)				
$V_{IHD}$	Differential Input HIGH Voltage		1100		V <sub>CC</sub>	mV
$V_{ILD}$	Differential Input LOW Voltage		GND		V <sub>CC</sub> – 100	mV
$V_{ID}$	Differential Input Voltage (V <sub>IHD</sub> – V <sub>ILD</sub> )		100		1200	mV
$V_{CMR}$	Input Common Mode Range (Differential Configuration, Note 10) (Figure 9)		1050		V <sub>CC</sub> - 50	mV
I <sub>IH</sub>	Input HIGH Current (VTx/VTx Open)		-150		150	μΑ
I <sub>IL</sub>	Input LOW Current (VTx/VTx Open)		-150		150	μΑ
CONTRO	DL INPUT (Reset pin)					
V <sub>IH</sub>	Input HIGH Voltage for Control Pin		V <sub>CC</sub> – 200		V <sub>CC</sub>	mV
$V_{IL}$	Input LOW Voltage for Control Pin		GND		200	mV
I <sub>IH</sub>	Input HIGH Current		-150		150	μΑ
I <sub>IL</sub>	Input LOW Current		-150		150	μΑ
TERMIN	ATION RESISTORS					
R <sub>TIN</sub>	Internal Input Termination Resistor		45	50	55	Ω
R <sub>TOUT</sub>	Internal Output Termination Resistor		45	50	55	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

<sup>5.</sup> Input and output parameters vary 1:1 with V<sub>CC</sub>.
6. CML outputs loaded with 50–CC

**Table 6. AC CHARACTERISTICS**  $V_{CC} = 1.71 \text{ V}$  to 2.625 V; GND = 0 V;  $T_A = -40 ^{\circ}\text{C}$  to  $85 ^{\circ}\text{C}$  (Note 11)

Symbol Characteristic Min Typ Max U
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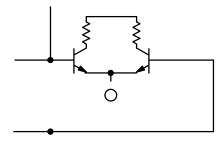
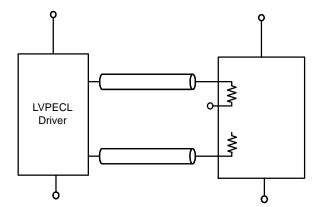


Figure 4. Input Structure



#### **DEVICE ORDERING INFORMATION**

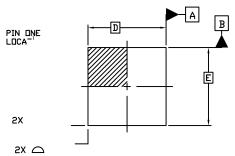
Device	Package	Shipping <sup>†</sup>
NB7V33MMNG	QFN-16 (Pb-Free)	123 Units / Rail
NB7V33MMNHTBG	QFN-16 (Pb-Free)	100 / Tape & Reel
NB7V33MMNTXG	QFN-16 (Pb-Free)	3,000 / Tape & Reel

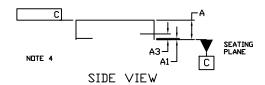
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging

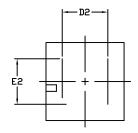


#### QFN16 3x3, 0.5P CASE 485G ISSUE G

**DATE 08 OCT 2021** 







NOTE 3

BOTTOM VIEW

# GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code A = Assembly Location

L = Wafer Lot Y = Year W = Work Week ■ Pb-Free Package

(Note: Microdot may be in either location)

<sup>\*</sup>This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

