# 1.8 V / 2.5 V Differential D Flip-Flop w/ Reset and CML Outputs

## Multi−Level Inputs w/ Internal Termination

# NB7V52M

**QFN−16**
**MN SUFFIX**
**CASE 485G**

**MARKING DIAGRAM***

| | |
|---|---|
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb−Free Package |

*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

### Description

The NB7V52M is a 10 GHz differential D flip−flop with a differential asynchronous Reset. The differential D/$\overline{D}$, CLK/$\overline{CLK}$ and R/$\overline{R}$ inputs incorporate dual internal 50 Ω termination resistors and will accept LVPECL, CML, LVDS logic levels.

When Clock transitions from logic Low to High, Data will be transferred to the differential CML outputs. The differential Clock inputs allow the NB7V52M to also be used as a negative edge triggered device.

The 16 mA differential CML outputs provide matching internal 50 Ω termination and produce 400 mV output swings when externally receiver terminated with a 50 Ω resistor to $V_{CC}$.

The NB7V52M is offered in a low profile 3 mm x 3 mm 16−pin QFN package. The NB7V52M is a member of the GigaComm™ family of high performance clock products. Application notes, models, and support documentation are available at www.onsemi.com.

### Features

- Maximum Input Clock Frequency > 10 GHz
- Maximum Input Data Rate > 10 Gb/s
- Random Clock Jitter < 0.8 ps RMS, Max
- 200 ps Typical Propagation Delay
- 35 ps Typical Rise and Fall Times
- Differential CML Outputs, 400 mV Peak−to−Peak, Typical
- Operating Range: $V_{CC}$ = 1.71 V to 2.625 V with $V_{EE}$ = 0 V
- Internal 50 Ω Input Termination Resistors
- QFN−16 Package, 3mm x 3mm
- −40°C to +85°C Ambient Operating Temperature
- These are Pb−Free Devices

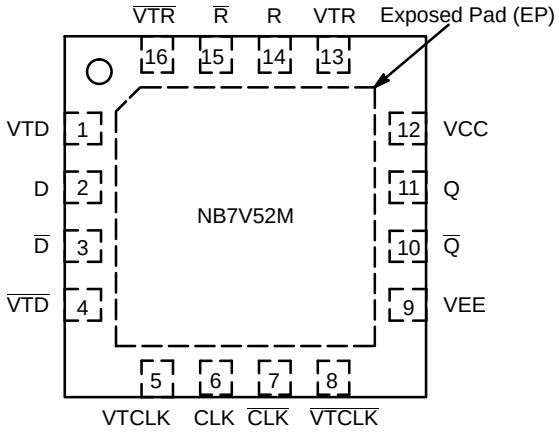

VTR
R
R
VTR
Exposed Pad (EP)
16
15
14
13
VTD
1
D
2
D
3
VTD
4
NB7V52M
12
VCC
11
Q
10
Q
9
VEE
5
6
7
8
VTCLK
CLK
CLK
VTCLK

**Table 2. ATTRIBUTES**

| Characteristics | | Value |
|---|---|---|
| ESD Protection | Human Body Model<br>Machine Model | > 2 kV<br>> 200 V |
| Moisture Sensitivity | 16−QFN | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in |
| Transistor Count | | 173 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive Power Supply | $V_{EE}$ = 0 V | | 3.0 | V |
| $V_{IO}$ | Positive Input/Output Voltage | $V_{EE}$ = 0 V | −0.5 ≤ VIO ≤ VCC + 0.5 | −0.5 to $V_{CC}$ +0.5 | V |
| $V_{INPP}$ | Differential Input Voltage \|CLK − $\overline{CLK}$\|, \|D − $\overline{D}$\|, \|R − $\overline{R}$\| | | | 1.89 | V |
| $I_{OUT}$ | Output Current Through $R_{TOUT}$ (50 Ω Resistor) | Continuous<br>Surge | | 34<br>40 | mA |
| $I_{IN}$ | Input Current Through $R_{TIN}$ (50 Ω Resistor) | | | ±40 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) (Note 3) | 0 lfpm<br>500 lfpm | QFN−16<br>QFN−16 | 42<br>35 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) (Note 3) | | QFN−16 | 4 | °C/W |
| $T_{sol}$ | Wave Solder Pb−Free | | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

**Table 4. DC CHARACTERISTICS, Multi−Level Inputs** $V_{CC}$ = 1.71 V to 2.625 V, $V_{EE}$ = 0 V, $T_A$ = −40°C to +85°C (Note 4)

| Symbol | Characteristic | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **POWER SUPPLY CURRENT** | | | | | | |
| $I_{CC}$ | Power Supply Current (Inputs and Outputs Open) | $V_{CC}$ = 2.5 V<br>$V_{CC}$ = 1.8 V | | 90<br>70 | 110<br>90 | mA |
| **CML OUTPUTS** | | | | | | |
| $V_{OH}$ | Output HIGH Voltage (Note 5) | $V_{CC}$ = 2.5 V<br>$V_{CC}$ = 1.8 V | $V_{CC}$ – 30<br>2470<br>1770 | $V_{CC}$ – 10<br>2490<br>1790 | $V_{CC}$<br>2500<br>1800 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 5) | $V_{CC}$ = 2.5 V | $V_{CC}$ – 650<br>1850 | $V_{CC}$ – 500<br>2000 | $V_{CC}$ – 400<br>2100 | mV |
| | | $V_{CC}$ = 1.8 V | $V_{CC}$ – 600<br>1200 | $V_{CC}$ – 450<br>1350 | $V_{CC}$ – 350<br>1450 | |
| **DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE−ENDED** (Note 6) (Figures 5 and 7) | | | | | | |
| $V_{th}$ | Input Threshold Reference Voltage Range (Note 7) | | 1000 | | $V_{CC}$ − 100 | mV |
| $V_{IH}$ | Single−Ended Input HIGH Voltage | | $V_{th}$ + 100 | | $V_{CC}$ | mV |
| $V_{IL}$ | Single−Ended Input LOW Voltage | | $V_{EE}$ | | $V_{th}$ − 100 | mV |
| $V_{ISE}$ | Single−Ended Input Voltage ($V_{IH}$ − $V_{IL}$) | | 200 | | 1200 | mV |
| **DIFFERENTIAL D/$\overline{D}$, CLK/$\overline{CLK}$, R/$\overline{R}$ INPUTS DRIVEN DIFFERENTIALLY** (Figures 6 and 8) (Note 8) | | | | | | |
| $V_{IHD}$ | Differential Input HIGH Voltage | | 1100 | | $V_{CC}$ | mV |
| $V_{ILD}$ | Differential Input LOW Voltage | | $V_{EE}$ | | $V_{CC}$ − 100 | mV |
| $V_{ID}$ | Differential Input Voltage ($V_{IHD}$ − $V_{ILD}$) | | 100 | | 1200 | mV |
| $V_{CMR}$ | Input Common Mode Range (Differential Configuration, Note 9) (Figure 10) | | 1050 | | $V_{CC}$ − 50 | mV |
| $I_{IH}$ | Input HIGH Current ($VT_x$/$\overline{VT_x}$ Open) | | −250 | | 250 | μA |
| $I_{IL}$ | Input LOW Current ($VT_x$/$\overline{VT_x}$ Open) | | −250 | | 250 | μA |
| **TERMINATION RESISTORS** | | | | | | |
| $R_{TIN}$ | Internal Input Termination Resistor | | 45 | 50 | 55 | Ω |
| $R_{TOUT}$ | Internal Output Termination Resistor | | 45 | 50 | 55 | Ω |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. Input and output parameters vary 1:1 with $V_{CC}$.
5. CML outputs loaded with 50 Ω to $V_{CC}$ for proper operation.
6. $V_{th}$, $V_{IH}$, $V_{IL,}$, and $V_{ISE}$ parameters must be complied with simultaneously.
7. $V_{th}$ is applied to the complementary input when operating in single−ended mode.
8. $V_{IHD}$, $V_{ILD,}$ $V_{ID}$

**Table 5. AC CHARACTERISTICS** $V_{CC}$ = 1.71 V to 2.625 V; $V_{EE}$ = 0 V; $T_A$ = −40°C to 85°C (Note 10)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Input Clock Frequency | | | | |

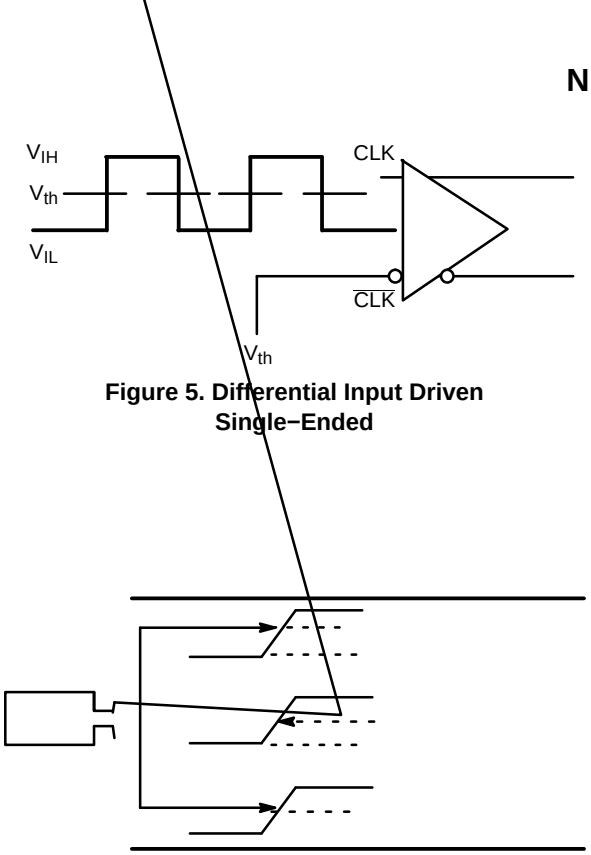



**Figure 5. Differential Input Driven Single−Ended**

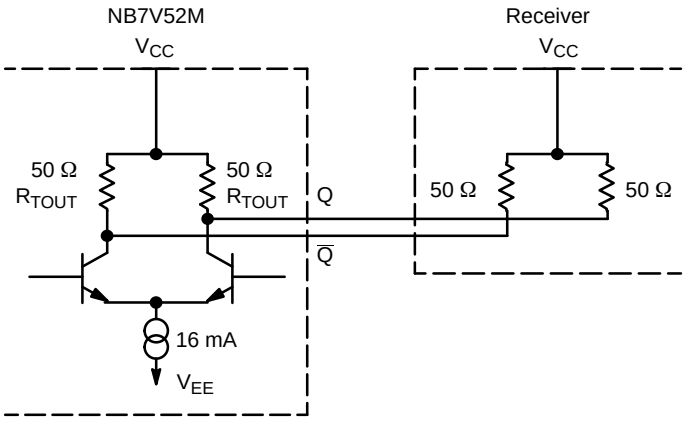
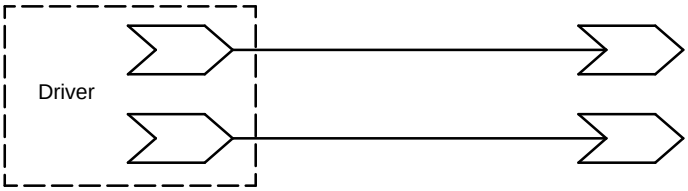
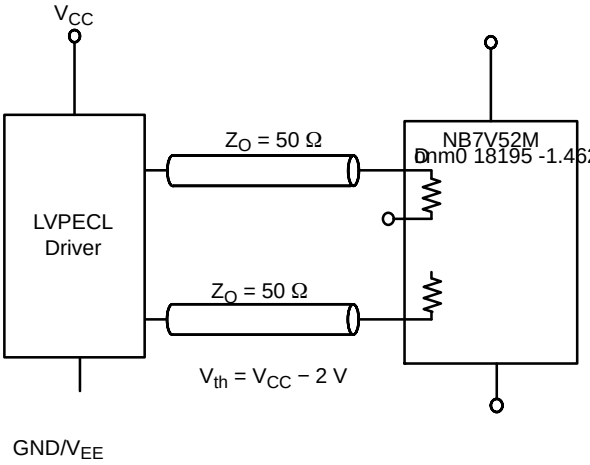



**Figure 11. Typical CML Output Structure and Termination**




$V_{CC}$
$Z_O$ = 50 Ω
NB7V52M
LVPECL
Driver
$Z_O$ = 50 Ω
$V_{th}$ = $V_{CC}$ − 2 V
GND/$V_{EE}$

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NB7V52MMNG | QFN−16<br>(Pb−free) | 123 Units / Rail |
| NB7V52MMNHTBG | QFN−16<br>(Pb−free) | 100 / Tape & Reel |
| NB7V52MMNTXG | QFN−16<br>(Pb−free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**QFN16 3x3, 0.5P**
CASE 485G
ISSUE G

DATE 08 OCT 2021

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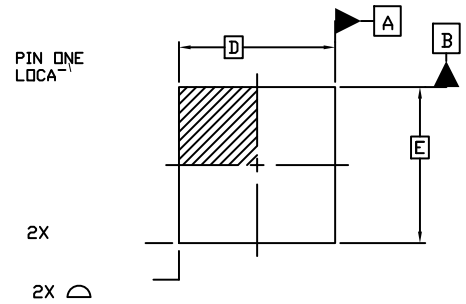
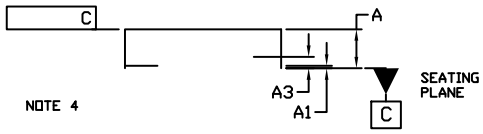
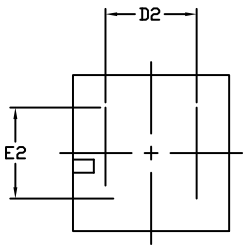
**SCALE 2:1**




SIDE VIEW




NOTE 3

BOTTOM VIEW

**GENERIC**
**MARKING DIAGRAM***


XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.