

1.8 V Differential 2:1 M Inp t to 1.2 V/1.8 V 1:6 CML Clock/Data Fano t B ffer / Translator

Multi-Level Inputs w/ Internal Termination

NB7V586M

Description

The NB7V586M is a differential 1–to–6 CML Clock/Data Distribution chip featuring a 2:1 Clock/Data input multiplexer with an input select pin. The INx/ $\overline{\text{INx}}$ inputs incorporate internal 50 Ω termination resistors and will accept differential LVPECL, CML, or LVDS logic levels (see Figure 12). The INx/ $\overline{\text{INx}}$ inputs and core logic are powered with a 1.8 V supply. The NB7V586M produces six identical differential CML output copies of Clock or Data. The outputs are configured as three banks of two differential pair. Each bank (or all three banks) have the flexibility of being powered by any combination of either a 1.8 V or 1.2 V supply.

The 16 mA differential CML output structure provides matching internal 50 Ω source terminations and 400 mV output swings when externally terminated with a 50 Ω resistor to V_{CCOX} (see Figure 11).

The 1:6 fanout design was optimized for low output skew and minimal jitter and is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data distribution applications operating up to 6 GHz or 10 Gb/s typical. The V_{REFAC} reference outputs can be used to rebias capacitor-coupled differential or single-ended input signals.

The NB7V586M is offered in a low profile 5x5 mm 32–pin Pb–Free QFN package. Application notes, models, and support documentation are available at www.onsemi.com.

The NB7V586M is a member of the GigaComm family of high performance clock products.

Features

Maximum Input Data Rate > 10 Gb/s Typical

Data Dependent Jitter < 10 ps

Maximum Input Clock Frequency > 6 GHz Typical

Random Clock Jitter < 0.8 ps RMS, Max

Low Skew 1:6 CML Outputs, 20 ps Max

2:1 Multi-Level Mux Inputs

175 ps Typical Propagation Delay

50 ps Typical Rise and Fall Times

Differential CML Outputs, 330 mV Peak-to-Peak, Typical

Operating Range: $V_{CC} = 1.71 \text{ V}$ to 1.89 V

Operating Range: $V_{CCO}x = 1.14 \text{ V}$ to 1.89 V

Internal 50 Ω Input Termination Resistors

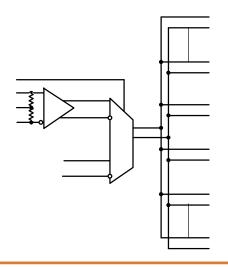


QFN32 MN SUFFIX CASE 488AM

MARKING DIAGRAM*

*For additional marking information, refer to Application Note <u>AND8002/D</u>.

SIMPLIFIED LOGIC DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

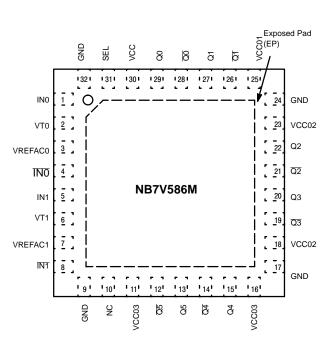


Figure 1. 32-Lead QFN Pinout (Top View)

Table 1. INPUT SELECT FUNCTION TABLE

SEL*	CLK Input Selected
0	IN0
1	IN1

Table 3. ATTRIBUTES

(Characteristics	Value			
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V			
Input Pullup Resistor (R _{PU})		75 kΩ			
Moisture Sensitivity (Note 3)		Level 1			
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in			
Transistor Count		308			
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test					

^{3.} For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	GND = 0 V		3.0	V
V _{CCOx}	Positive Power Supply	GND = 0 V		3.0	V
V _{IO}	Input/Output Voltage	GND = 0 V	$-0.5 \le V_{IO} \le V_{CC} + 0.5$	-0.5 to $V_{CC} + 0.5$	V
V _{INPP}	Differential Input Voltage IN _x - IN _x			1.89	V
I _{IN}	Input Current Through R _T (50 Ω Resistor)			±40	mA
I _{OUT}	Output Current	Continuous Surge		34 40	mA
I _{VFREFAC}	V _{REFAC} Sink/Source Current			±1.5	mA
T _A	Operating Temperature Range			-40 to +85	С
T _{stg}	Storage Temperature Range			-65 to +150	С
θJA	Thermal Resistance (Junction–to–Ambient) (Note 4)	0 lfpm 500 lfpm	QFN-32 QFN-32	31 27	C/W C/W
$\theta_{\sf JC}$	Thermal Resistance (Junction-to-Case) (Note 4)	Standard Board	QFN-32	12	C/W
T _{sol}	Wave Solder Pb-Free			265	С

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these

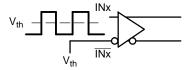
Table 5. DC CHARACTERISTICS – CML OUTPUT V_{CC} = 1.8 V $\pm 5\%$, V_{CCO1} = 1.2 V $\pm 5\%$ or 1.8 V $\pm 5\%$, V_{CCO2} = 1.2 V $\pm 5\%$ or 1.8 V $\pm 5\%$, V_{CCO3} = 1.2 V $\pm 5\%$ or 1.8 V $\pm 5\%$ or 1.

Symbol	Characteristic		Min	Тур	Max	Unit
POWER	WER SUPPLY CURRENT (Inputs and Outputs open)					
I _{CC}	Power Supply Current for V _{CC} Power Supply Current for VCCOx	(Inputs and Outputs Open) (Inputs and Outputs Open)		75 95	125 105	mA
CML OU	CML OUTPUTS (Note 6)					
V _{OH}	Output HIGH Voltage	V _{CC} = 1.8 V, VCCOx = 1.8 V V _{CC} = 1.8 V, VCCOx = 1.2 V	V _{CCOx} – 40 1760 1160	V _{CCOx} – 20 1780 1180	V _{CCOx} 1800 1200	mV

Table 6. AC CHARACTERISTICS $V_{CC} = 1.8 \text{ V} \pm 5\%$, $V_{CCO1} = 1.2 \text{ V} \pm 5\%$ or $1.8 \text{ V} \pm 5\%$, $V_{CCO2} = 1.2 \text{ V} \pm 5\%$ or $1.8 \text{ V} \pm 5\%$, or $1.8 \text{ V} \pm 5\%$, or $1.8 \text{ V} \pm 5\%$, $V_{CCO3} = 1.2 \text{ V} \pm 5\%$ or $1.8 \text{ V} \pm 5\%$, $V_{CCO3} = 1.2 \text{ V} \pm 5\%$ or $1.8 \text{ V} \pm 5\%$, $V_{CCO3} = 1.2 \text{ V} \pm 5\%$ or $1.8 \text{ V} \pm 5\%$, $V_{CCO3} = 1.2 \text{ V} \pm 5\%$ or $1.8 \text{ V} \pm 5\%$, $V_{CCO3} = 1.2 \text{ V} \pm 5\%$ or $1.8 \text{ V} \pm 5\%$, $V_{CCO3} = 1.2 \text{ V} \pm 5\%$ or $1.8 \text{ V} \pm 5\%$, $V_{CCO3} = 1.2 \text{ V} \pm 5\%$ or $1.8 \text{ V} \pm 5\%$, $V_{CCO3} = 1.2 \text{ V} \pm 5\%$ or $1.8 \text{ V} \pm 5\%$, $V_{CCO3} = 1.2 \text{ V} \pm 5\%$ or $1.8 \text{ V} \pm 5\%$, $V_{CCO3} = 1.2 \text{ V} \pm 5\%$ or $1.8 \text{ V} \pm 5\%$, $V_{CCO3} = 1.2 \text{ V} \pm 5\%$ or $1.8 \text{ V} \pm 5\%$, $V_{CCO3} = 1.2 \text{ V} \pm 5\%$ or $1.8 \text{ V} \pm 5\%$, $V_{CCO3} = 1.2 \text{ V} \pm 5\%$, $V_{CCO3} = 1$

Characteristic	Min	Тур	Max	Unit
Maximum Input Clock Frequency, V _{OUTPP} ≥ 200 mV	4.0	6.0		GHz
Maximum Operating Input Data Rate (PRBS23)	10			Gbps
Output Voltage Amplitude (See Figures 4, Note 15) $f_{in} \le 4.0 \text{ GHz}$	200	330		mV
٨	Maximum Input Clock Frequency, V _{OUTPP} ≥ 200 mV Maximum Operating Input Data Rate (PRBS23)	Maximum Input Clock Frequency, V _{OUTPP} ≥ 200 mV 4.0 Maximum Operating Input Data Rate (PRBS23) 10	Maximum Input Clock Frequency, $V_{OUTPP} \ge 200 \text{ mV}$ 4.0 6.0 Maximum Operating Input Data Rate (PRBS23) 10	Maximum Input Clock Frequency, V _{OUTPP} ≥ 200 mV 4.0 6.0 Maximum Operating Input Data Rate (PRBS23) 10

 t_{PLH}, t_{PHL} Propagation Delay to Output Differential @ 1 GHz, $IN_x/INmV$



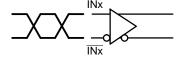


Figure 6. Differential Input Driven Single-Ended

Figure 7. Differential Inputs Driven Differentially

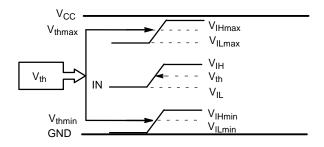


Figure 8. V_{th} Diagram

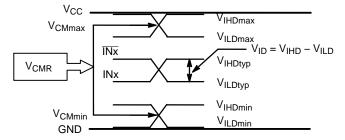
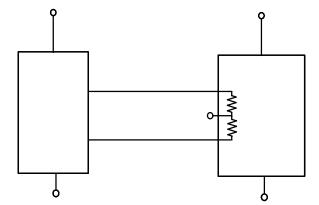


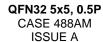
Figure 9. $V_{\rm CMR}$ Diagram



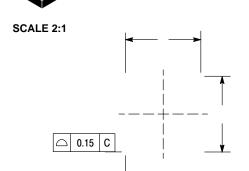


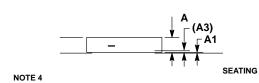
MECHANICAL CASE OUTLINE

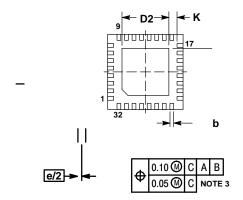
PACKAGE DIMENSIONS



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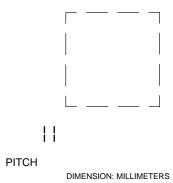






RECOMMENDED

DOCUMENT NUMBER:



			MAX	
		0.80	1.00	
	A1		0.05	
	A3	0.20 REF		
	b	0.18	0.30	
	D 5.00 BSC			
	D2	2.95	3.25	
E 5.00 BSC				
	E2	2.95	3.25	
	е	0.50 BSC		
	K	0.20		
	٦	0.30	0.50	
	L1		0.15	

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AWLYYWW=

Free indicator, "G" or

98AON20032D

