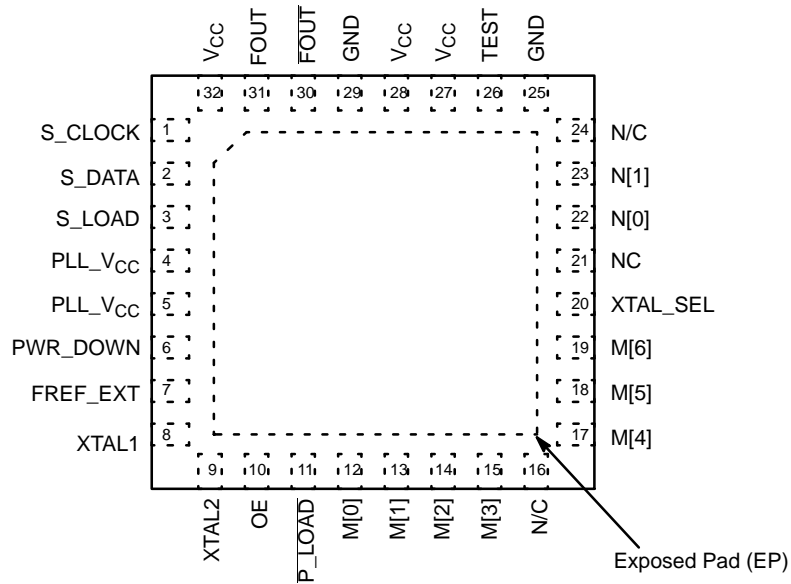






# NBC12439A



**Figure 2. 32-Lead QFN (Top View)**

The following gives a brief description of the functionality of the NBC12349A Inputs and Outputs. Unless explicitly stated, all inputs are CMOS/TTL compatible with either pull up or pulldown resistors. The PECL outputs are capable of driving two series terminated 50 transmission lines on the incident edge.

**Table 3. PIN FUNCTION DESCRIPTION**

Pin Name	Function	Description
<b>INPUTS</b>		
XTAL1, XTAL2	Crystal Inputs	These pins form an oscillator when connected to an external series-resonant crystal.
S_LOAD*	CMOS/TTL Serial Latch Input (Internal Pulldown Resistor)	This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH; thus, the data must be stable on the HIGH-to-LOW transition of S_LOAD for proper operation.
S_DATA*	CMOS/TTL Serial Data Input (Internal Pulldown Resistor)	This pin acts as the data input to the serial configuration shift registers.
S_CLOCK*	CMOS/TTL Serial Clock Input (Internal Pulldown Resistor)	This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge.
P_LOAD**	CMOS/TTL Parallel Latch Input (Internal Pullup Resistor)	This pin loads the configuration latches with the contents of the parallel inputs. The latches will be transparent when this signal is LOW; therefore, the parallel data must be stable on the LOW-to-HIGH transition of P_LOAD for proper operation.
M[6:0]**	CMOS/TTL PLL Loop Divider Inputs (Internal Pullup Resistor)	These pins are used to configure the PLL loop divider. They are sampled on the LOW-to-HIGH transition of P_LOAD. M[6] is the MSB, M[0] is the LSB.
N[1:0]**	CMOS/TTL Output Divider Inputs (Internal Pullup Resistor)	These pins are used to configure the output divider modulus. They are sampled on the LOW-to-HIGH transition of P_LOAD.
OE**	CMOS/TTL Output Enable Input (Internal Pullup Resistor)	Active HIGH Output Enable. The Enable is synchronous to eliminate possibility of runt pulse generation on the FOUT output. When Disabled, FOUT goes LOW and FOUT.
FREF_EXT*		

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**Table 3. PIN FUNCTION DESCRIPTION** (continued)

Pin Name	Function	Description
<b>OUTPUTS</b>		
FOUT, FOUT	PECL Differential Outputs	These differential, positive-referenced ECL signals (PECL) are the outputs of the synthesizer.
TEST	CMOS/TTL Output	The function of this output is determined by the serial configuration bits T[2:0].
<b>POWER</b>		
V <sub>CC</sub>	Positive Supply for the Logic	The positive supply for the internal logic and output buffer of the chip, and is connected to +3.3 V or +5.0 V.
PLL_V <sub>CC</sub>	Positive Supply for the PLL	This is the positive supply for the PLL and is connected to +3.3 V or +5.0 V.
GND	Negative Power Supply	These pins are the negative supply for the chip and are normally all connected to ground.
-	Exposed Pad for QFN-32 only	The Exposed Pad (EP) on the QFN-32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to GND.

\* When left Open, these inputs will default LOW.

\*\* When left Open, these inputs will default HIGH.

**Table 4. ATTRIBUTES**

Characteristics	Value
Internal Input Pulldown Resistor	

# NBC12439A

**Table 6. DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V} \pm 5\%$ ;  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ )

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$V_{IH}$ LVCMOS/ LVTTTL	Input HIGH Voltage	$V_{CC} = 3.3\text{ V}$	2.0			V
$V_{IL}$ LVCMOS/ LVTTTL	Input LOW Voltage	$V_{CC} = 3.3\text{ V}$			0.8	V
$I_{IN}$	Input Current				1.0	mA
$V_{OH}$	Output HIGH Voltage	TEST $I_{OH} = -0.8\text{ mA}$	2.5			V
$V_{OL}$	Output LOW Voltage	TEST $I_{OL} = 0.8\text{ mA}$			0.4	V
$V_{OH}$ PECL	Output HIGH Voltage	FOUT FOUT $V_{CC} = 3.3\text{ V}$ (Notes 2, 3)	2.155		2.405	V
$V_{OL}$ PECL	Output LOW Voltage	FOUT FOUT $V_{CC} = 3.3\text{ V}$ (Notes 2, 3)	1.355		1.675	V
$I_{CC}$	Power Supply Current	$V_{CC}$ PLL_ $V_{CC}$	44 19	58 23	80 28	mA mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit

F30.022C Tm.0018 .5 BT 0 8407498 398.660 trans1.77 .3-.0017 90.3113 Tc[2 0 9(19)T]E/F1 33.56T85200102 30001T5561 .90786.1764 Tm21 Tm.0

# NBC12439A

**Table 8. AC CHARACTERISTICS** ( $V_{CC} = 3.135 \text{ V to } 5.25 \text{ V } \pm 5\%$ ;  $T_A = -40^\circ\text{C to } 85^\circ$ )

## FUNCTIONAL DESCRIPTION

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by 2 before being sent to the phase detector. With a 16 MHz crystal, this provides a reference frequency of 8 MHz. Although this data sheet illustrates functionality only for a 16 MHz crystal, Table 9, any crystal in the 10 – 20 MHz range can be used, Table 11.

The VCO within the PLL operates over a range of 400 to 800 MHz. Its output is scaled by a divider, M divider, that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and the loop filter force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve loop lock.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This N output divider is configured through either the serial or the parallel interfaces and can provide one of four division ratios (1, 2, 4, or 8). This divider extends the performance of the part while providing a 50% duty cycle.

The output driver is driven differentially from the output divider and is capable of driving a pair of transmission lines terminated into 50  $\Omega$  to  $V_{CC} - 2.0$  V. The positive reference

for the output driver and the internal logic is separated from the power supply for the phase locked loop to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[6:0] and N[1:0] inputs to configure the internal counters. Normally upon system reset, the  $\overline{P\_LOAD}$  input is held LOW until sometime after power becomes valid. On the LOW to HIGH transition of  $\overline{P\_LOAD}$ , the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[6:0] and N[1:0] inputs to reduce component count in the application of the chip.

The serial interface logic is implemented with a fourteen bit shift register scheme. The register shifts once per rising edge of the S\_CLOCK input. The serial input S\_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. With P\_LOAD held high, the configuration latches will capture the value of the shift register on the HIGH to LOW edge of the S\_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.

**Table 9. PROGRAMMING VCO FREQUENCY FUNCTION TABLE WITH 16 MHZ CRYSTAL**

VCO Frequency (MHz)	M Count Divisor	64	32	16	8	4	2	1
		M6	M5	M4	M3	M2	M1	M0
400	25	0	0	1	1	0	0	1
416	26	0	0	1	1	0	1	0
432	27	0	0	1	1	0	1	1
448	28	0	0	1	1	1	0	0
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
752	47	0	1	0	1	1	1	1
768	48	0	1	1	0	0	0	0
784	49	0	1	1	0	0	0	1
800	50	0	1	1	0	0	1	0

## PROGRAMMING INTERFACE

Programming the NBC12439A is accomplished by properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can be represented by this formula:

$$F_{OUT} = ((F_{XTAL} \text{ or } F_{REF\_EXT} \div 2) \times 2 M) \div N \quad (\text{eq. 1})$$

This can be simplified to:

$$F_{OUT} = (F_{XTAL} \text{ or } F_{REF\_EXT}) \times M \div N \quad (\text{eq. 2})$$

where  $F_{XTAL}$  is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be  $25 \leq M \leq 50$  for a 16 MHz input reference. See Table 11.

Assuming that a 16 MHz reference frequency is used the above equation reduces to:

$$F_{OUT} = 16M \div N \quad (\text{eq. 3})$$

Substituting the four values for N (1, 2, 4, 8) yields:

**Table 10. PROGRAMMABLE OUTPUT DIVIDER FUNCTION**

N1	N0	N Divider	F <sub>OUT</sub>
----	----	-----------	------------------



Table 11. FREQUENCY OPERATING RANGE

Most of the signals available on the TEST output pin are useful only for performance verification of the device itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110, the device is placed in PLL bypass mode. In this mode the S\_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S\_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. Figure 5 shows the functional setup of the PLL bypass mode. Because the S\_CLOCK is a CMOS level the input frequency is limited to 250 MHz or less. This means the fastest the FOUT pin can be toggled via the S\_CLOCK is 250 MHz as the minimum divide ratio of the N counter is 1. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

T2	T1	T0	TEST OUTPUT
0	0	0	SHIFT REGISTER OUT
0	0	1	HIGH
0	1	0	FREF
0	1	1	M COUNTER OUT
1	0	0	FOUT
1	0	1	LOW
1	1	0	PLL BYPASS
1	1	1	FOUT ÷ 4

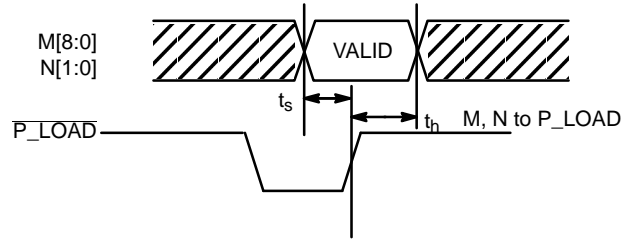


Figure 3. Parallel Interface Timing Diagram

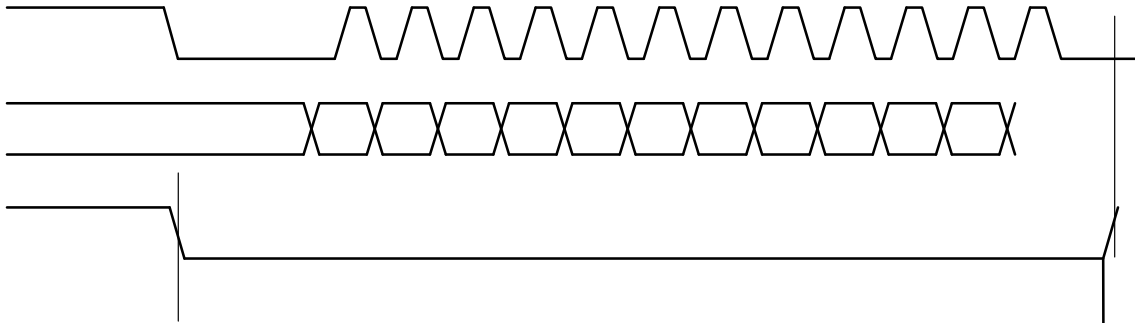


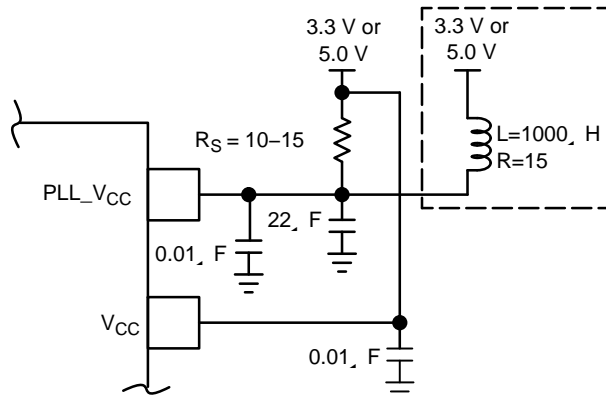
Figure 4. Serial Interface Timing Diagram

## APPLICATIONS INFORMATION

### Using the On-Board Crystal Oscillator

NBC12439A feature a fully integrated on board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large load capacitors. The oscillator is totally self contained so that the only external component required is the crystal per Figure 6 (do not use crystal load caps). As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal

capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.



**Figure 7. Power Supply Filter**

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. Figure 7 shows a 1000  $\mu$ H choke. This value choke will show a significant impedance at 10 KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL\_VCC pin, a low DC resistance inductor is required (less than 15  $\Omega$ ). Generally, the resistor/capacitor filter will be cheaper, easier to implement, and provide an adequate level of supply filtering.

The NBC12439A provides sub nanosecond output edge rates and therefore a good power supply bypassing scheme is a must. The important aspect of the layout is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the NBC12439A outputs. It is imperative that low inductance chip capacitors are used. It is equally important that the board layout not introduce any of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

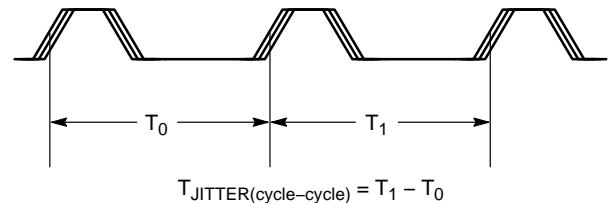
The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on board oscillator. Note the provisions for placing a resistor across the crystal oscillator terminals as discussed in the crystal oscillator section of this data sheet.

Although the NBC12439A has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

### Jitter Performance

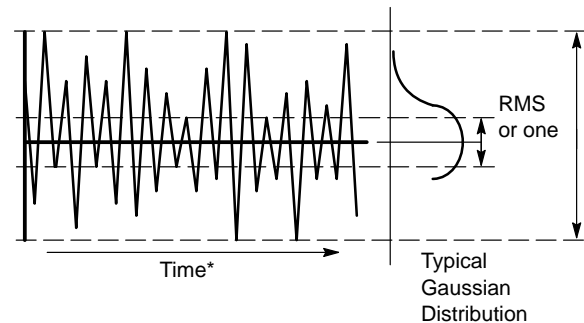
Jitter is a common parameter associated with clock generation and distribution. Clock jitter can be defined as the deviation in a clock's output transition from its ideal position.

**Cycle to Cycle Jitter** (short term) is the period variation between adjacent periods over a defined number of observed cycles. The number of cycles observed is application dependent but the JEDEC specification is 1000 cycles. See Figure 8.



**Figure 8. Cycle-to-Cycle Jitter**

**Random Peak to Peak Jitter** is the difference between the highest and lowest acquired value and is represented as the width of the Gaussian base. See Figure 9.



**Figure 9. Random Peak-to-Peak and RMS Jitter**

post processing software can analyze the data to find the maximum and minimum periods.

Recent hardware and software developments have resulted in advanced jitter measurement techniques. The Tektronix TDS series oscilloscopes have superb jitter analysis capabilities on non contiguous clocks with their histogram and statistics capabilities. The Tektronix TDSJIT2/3 Jitter Analysis software provides many key timing parameter measurements and will extend that capability by making jitter measurements on contiguous clock and data cycles from single shot acquisitions.

M1 by Amherst was used as well and both test methods correlated.

This test process can be correlated to earlier test methods and are more accurate. All of the jitter data reported on the NBC12439A was collected in this manner

# NBC12439A

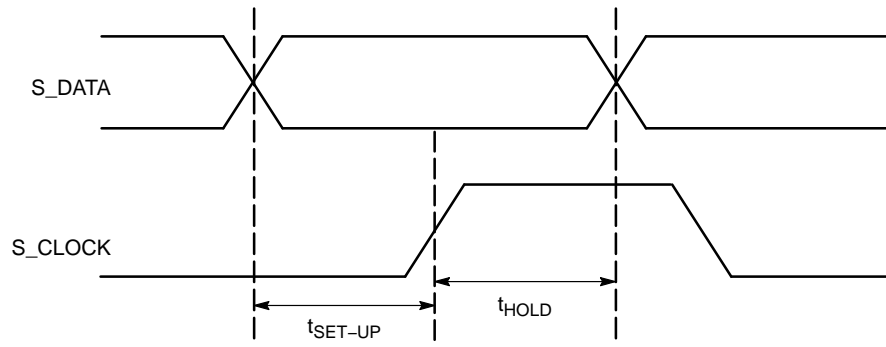


Figure 12. Setup and Hold

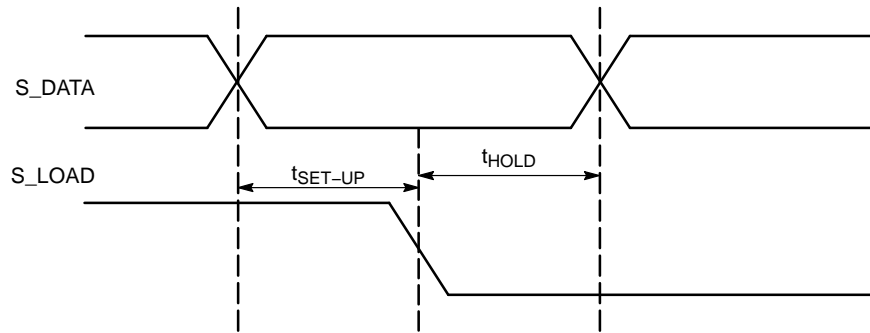


Figure 13. Setup and Hold

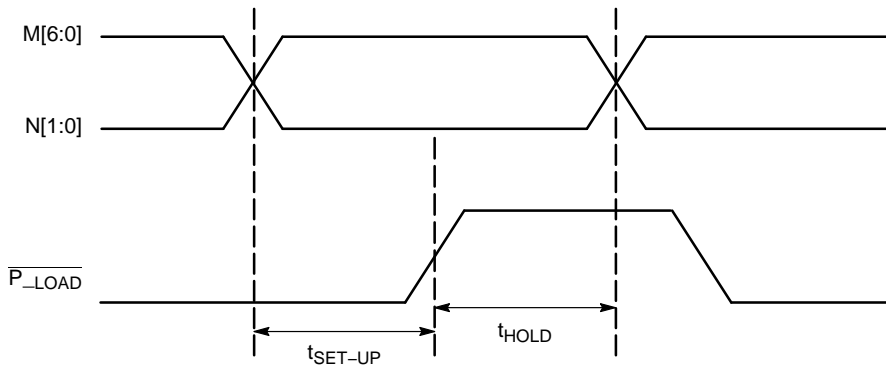


Figure 14. Setup and Hold

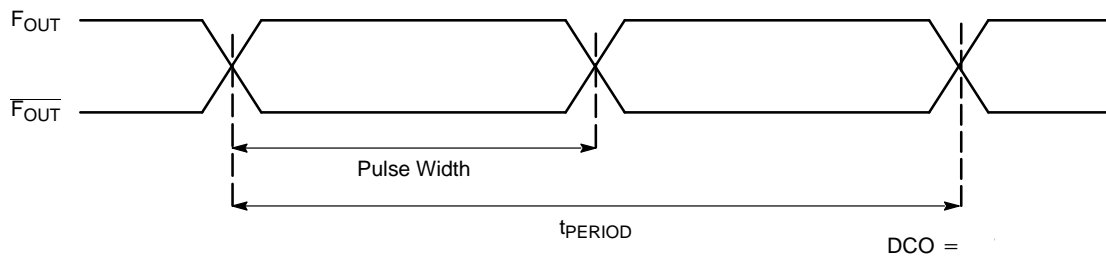


Figure 15. Output Duty Cycle

# NBC12439A

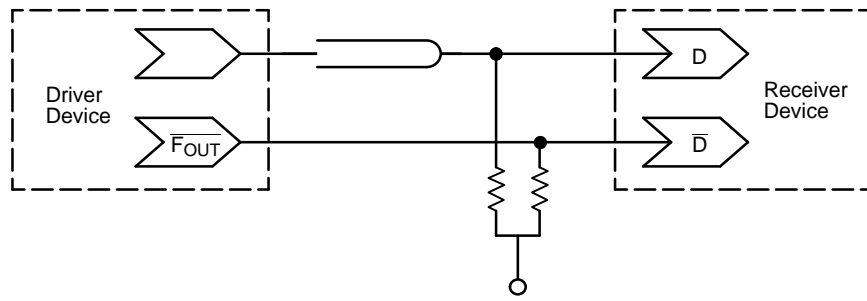
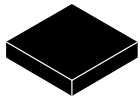


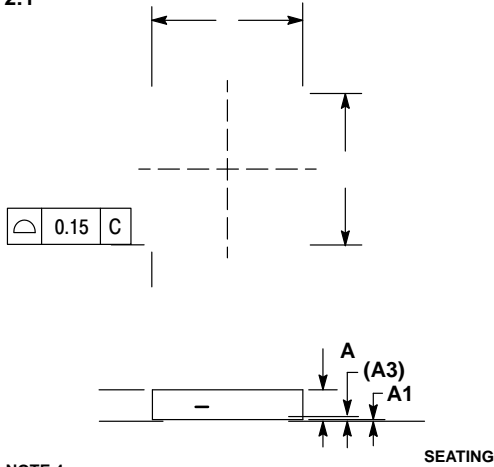
Figure 16. Typical Termination for Output Driver and Device Evaluation  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)



**QFN32 5x5, 0.5P**  
CASE 488AM  
ISSUE A

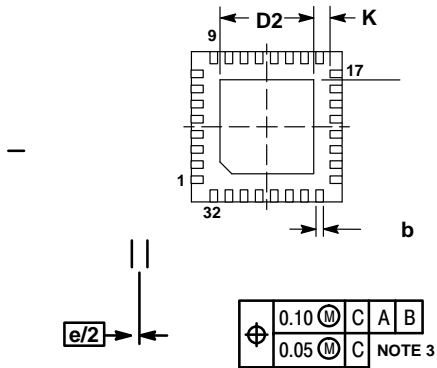
DATE 23 OCT 2013

SCALE 2:1



NOTE 4

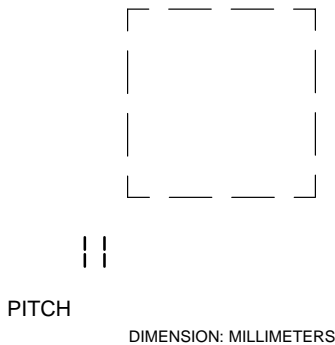
	MAX
A1	0.80 1.00
A3	0.20 REF 0.05
b	0.18 0.30
D	5.00 BSC
D2	2.95 3.25
E	5.00 BSC
E2	2.95 3.25
e	0.50 BSC
K	0.20
L	0.30 0.50
L1	0.15



XXXXXXXXXX  
XXXXXXXXXX  
AWLYYYWW■

■Free indicator, "G" or

**RECOMMENDED**



PITCH

DIMENSION: MILLIMETERS

<b>DOCUMENT NUMBER:</b>	<b>98AON20032D</b>	



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