DATA SHEET
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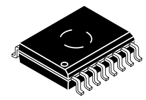
I la ed High C e IGBT Ga e D i e

NCD57001



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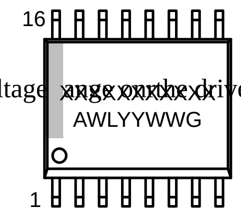
SOIC−16 WB
CASE 751G−03

NCD57001 is a high current single channel IGBT driver with internal galvanic isolation, designed for high system efficiency and reliability in high power applications. Its features include complementary inputs, open drain FAULT and Ready outputs, active Miller clamp, accurate UVLOs, DESAT protection, and soft turn off at DESAT. NCD57001 accommodates both 5 V ... (UL1577 rating) galvanic isolation ... the input side ... 1200 V ... wide bias voltage range on the driver negative voltage capability.

IORM

MARKING DIAGRAM

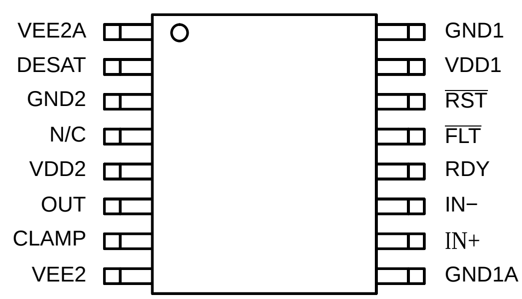


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

- High Current Output (+4/ 6 A) at IGBT Miller Plateau Voltages
- Low Output Impedance for Enhanced IGBT Driving
- Short Propagatio
- Active Miller Clamp to Prevent Spurious Gate Turn on
- DESAT Protection with Programmable Delay
- Negative Voltage (Down to 9 V) Capability for DESAT
- Soft Turn Off During IGBT Short Circuit
- IGBT Gate Clamping During Short Circuit
- IGBT Gate Active Pull Down
- Tight UVLO Thresholds for Bias Flexibility
- Wide Bias Voltage Range including Negative VEE2
- 3.3 V to 5 V Input Supply Voltage
- Designed for AEC Q100 Certification
- 5000 V Galvanic Isolation (to meet UL1577 Requirements)
- 1200 V Working Voltage (per VDE0884 10 Requirements)
- High Transient Immunity
- High Electromagnetic Immunity
- These Devices are Pb Free, Halogen Free and are RoHS Compliant

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

Typical Applications

- Solar Inverters
- Motor Control
- Uninterruptible Power Supplies (UPS)
- Industrial Power Supplies
- Welding

PIN DESCRIPTION

Pin Name	No.	I/O	Description
V_{EE2A}	1	Power	

SAFETY AND INSULATION RATINGS

Symbol	Parameter		Value	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage	< 150 V_{RMS}	I − IV	
		< 300 V_{RMS}	I − IV	
		< 450 V_{RMS}	I − IV	
		< 600 V_{RMS}	I − IV	
		< 1000 V_{RMS}	I − III	
CTI				

ABSOLUTE MAXIMUM RATINGS (Over operating free−air temperature range unless otherwise noted) (Note 1)

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD1}−GND1	Supply voltage, input side	−0.3	6	V
V_{DD2}−GND2	Positive Power Supply, output side	−0.3	25	V
V_{EE2}−GND2	Negative Power Supply, output side	−10	0.3	V
V_{DD2}−V_{EE2} (V_{MAX2})	Differential Power Supply, output side	0	25	V

OPERATING RANGES (Note 6)

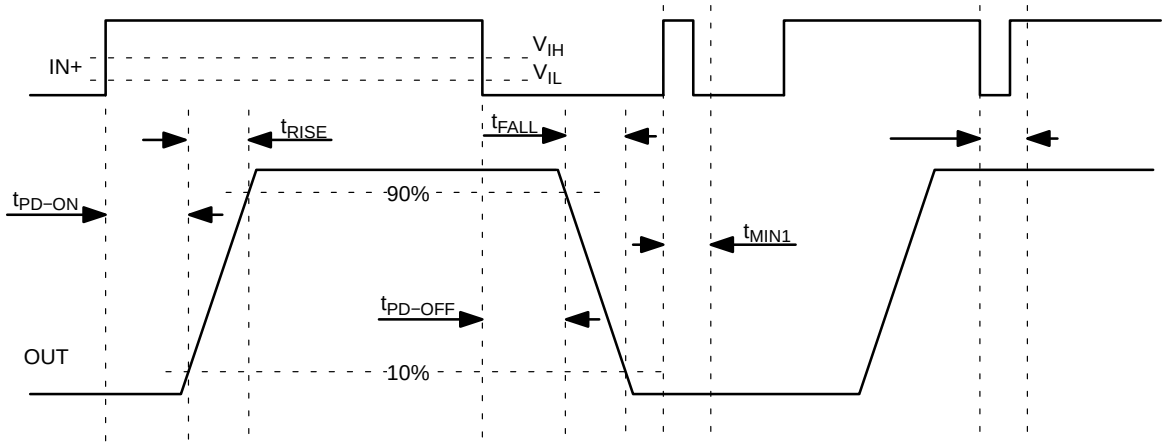
Symbol	Parameter	Min	Max	Unit
V_{DD1}−GND1	Supply voltage, input side	UVLO1	5.5	V
V_{DD2}−GND2	Positive Power Supply, output side	UVLO2	24	V
V_{EE2}−GND2	Negative Power Supply, output side	−10	0	V
V_{DD2}−V_{EE2} (V_{MAX2})	Differential Power Supply, output side	0	24	V
V_{IL}	Low level input voltage at IN+, IN−, /RST	0		

ELECTRICAL CHARACTERISTICS (V_{DD1} = 5 V, V_{DD2} = 15 V, V_{EE2} = −8 V. For typical values T_A = 25 C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
LOGIC INPUT AND OUTPUT						
V_{IL}	IN+, IN−, /RST Low Input Voltage		−	−	0.3 x V_{DD1}	V
V_{IH}	IN+, IN−, /RST High Input Voltage		0.7 x V_{DD1}	−	−	V
$V_{IN-HYST}$	Input Hysteresis Voltage		−	0.15 x V_{DD1}	−	V
I_{IN-L}, I_{RST-L}	IN−, /RST Input Current (50 kΩ pull−up resistor)	V_{IN-}/V_{RST} = 0 V	−	−100	−	μA
I_{IN+H}	IN+ Input Current (50 kΩ pull−down resistor)	V_{IN+} = 5 V	−	100	−	μA
I_{RDY}						

ELECTRICAL CHARACTERISTICS (V_{DD1} = 5 V, V_{DD2} = 15 V, V_{EE2} = −8 V. For typical values T_A = 25 C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
t_{PD-ON}	IN+, IN− to Output High Propagation Delay	C_{LOAD} = 10 nF V_{IH} to 10% of output change for PW > 150 ns. OUT and CLAMP pins are connected together	40	60	90	ns
t_{PD-OFF}	IN+, IN− to Output Low Propagation Delay	C_{LOAD} = 10 nF V_{IL} to 90% of output change for PW > 150 ns. OUT and CLAMP pins are connected together				


IN+
V_{IH}
V_{IL}
t_{RISE}
t_{FALL}
t_{PD-ON}
90%
t_{MIN1}
t_{PD-OFF}
OUT
10%

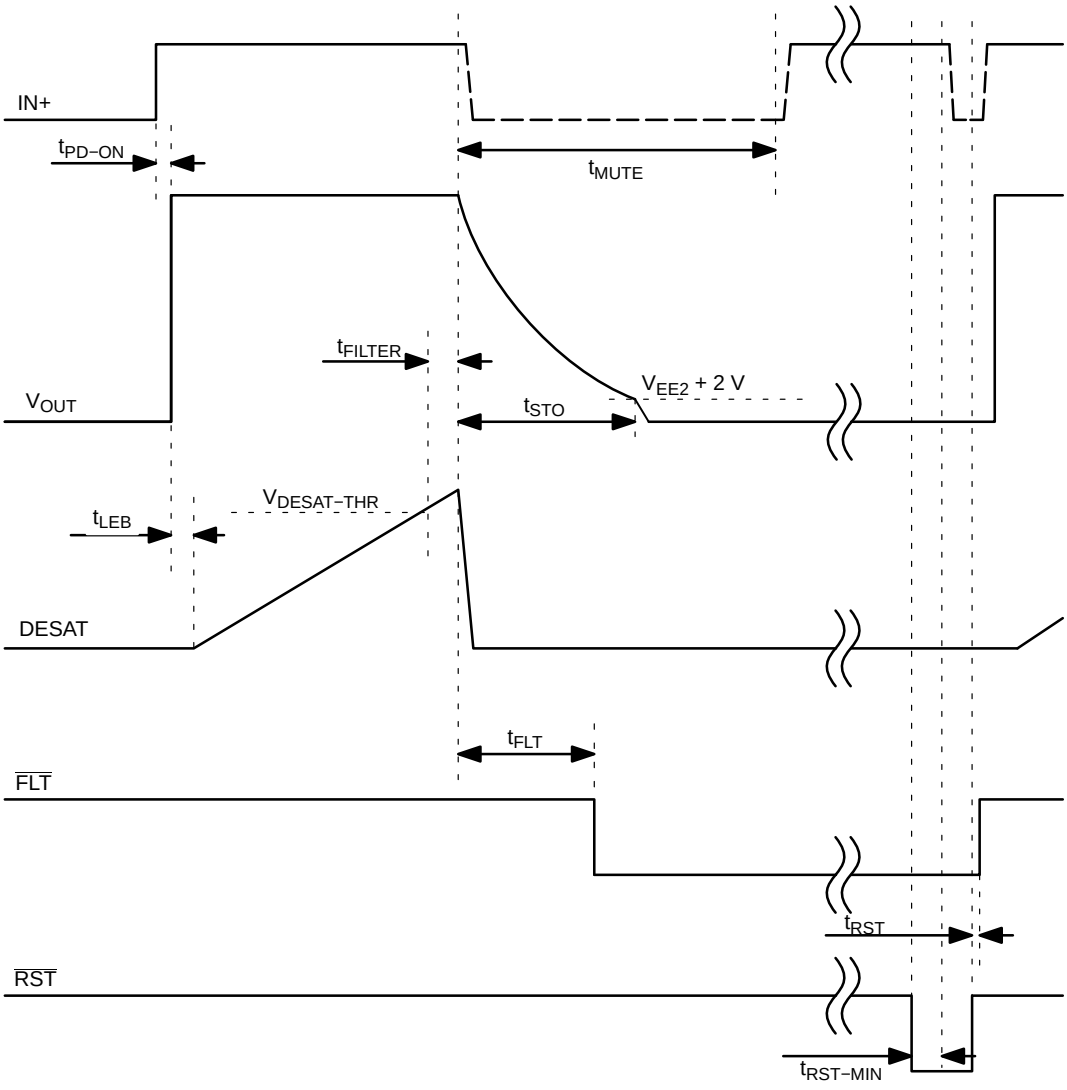


Figure 5. DESAT Response Waveform

TYPICAL CHARACTERISTICS

(Conditions for the following figures are the same as stated for ELECTRICAL CHARACTERISTICS Table unless otherwise noted. Typical and/or average values are used.) (continued)

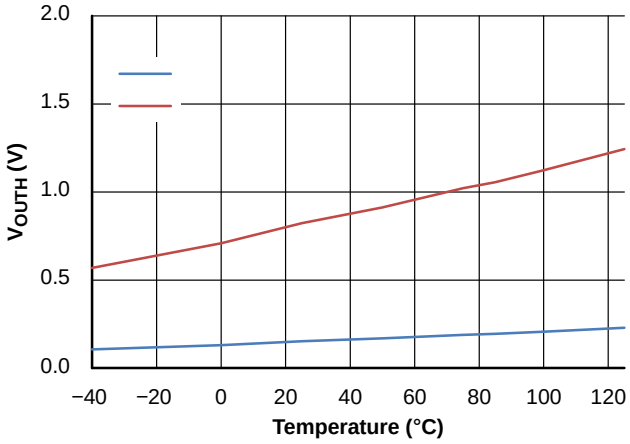


Figure 12. Output Voltage Drop, Sourcing

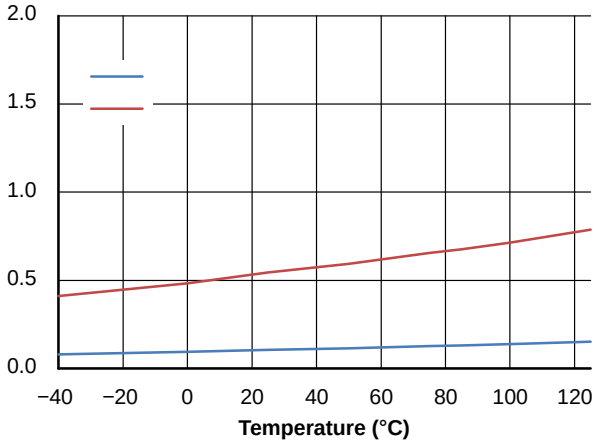


Figure 13. Output Voltage Drop, Sinking

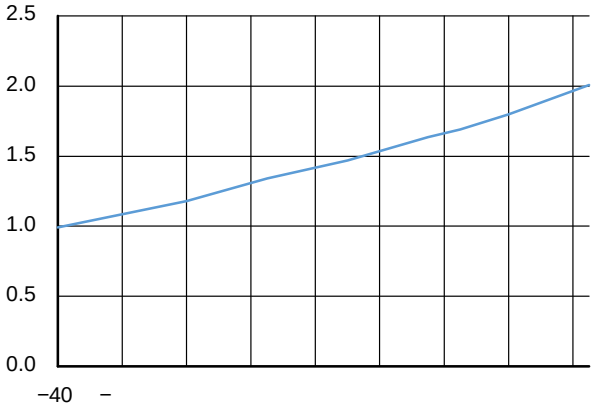


Figure 14. CLAMP Voltage Drop

Figure 15. IGBT Short Circuit Clamp Voltage Drop

Figure 16. Propagation Delay

Figure 17. Rise and Fall Time

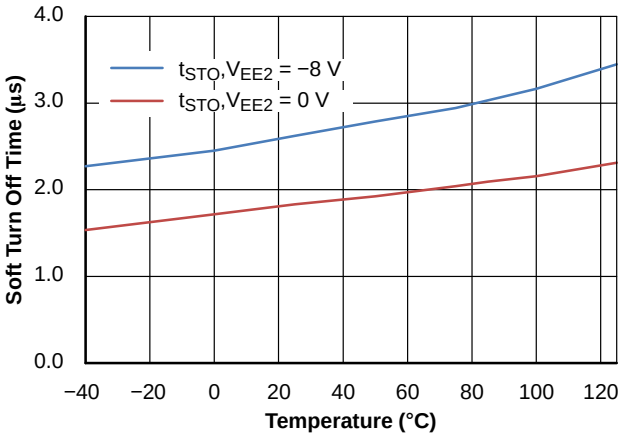


Figure 18. Soft Turn Off Time

FEATURE DESCRIPTIONS

Under Voltage Lockout (UVLO)

UVLO ensures correct switching of IGBT connected to the driver output.

- The IGBT is turned off, if the supply V_{CC1} drops below $V_{UVLO1\ OUT\ OFF}$ and the RDY pin output goes to low.
- The driver output does not start to react to the input signal on V_{IN} until the V_{CC1} rises above the $V_{UVLO1\ OUT\ ON}$ again. If the supply V_{CC1} increase over $V_{UVLO1\ OUT\ ON}$, the RDY pin output goes to be open drain and outputs continue to switch IGBT
- The IGBT is turned off, if the supply V_{CC2} drops below $V_{UVLO2\ OUT\ OFF}$ and the RDY pin output goes to low.
- The driver output does not start to react to the input signal on V_{IN} until the V_{CC1} rises above the $V_{UVLO1\ OUT\ ON}$ again. If the supply V_{DD1} increases over $V_{UVLO1\ OUT\ ON}$, the RDY pin output goes to be open drain and outputs continue to switch IGBT
- VEE2 is not monitored.

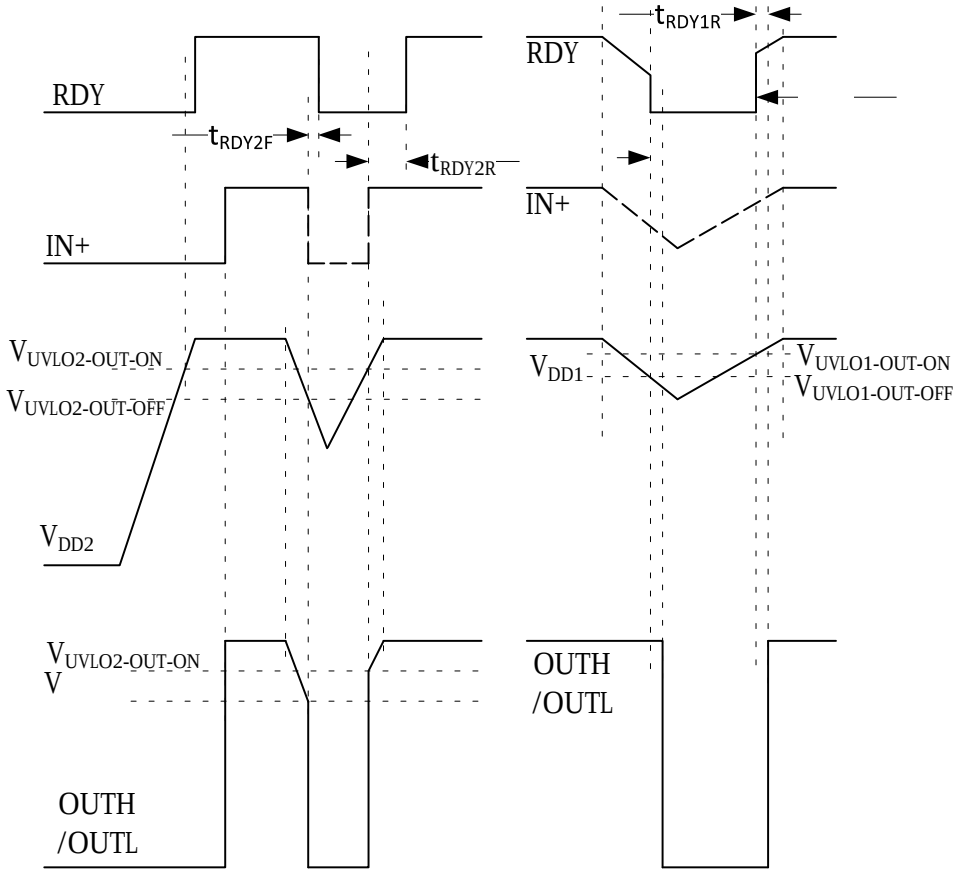


Figure 19. UVLO Diagram

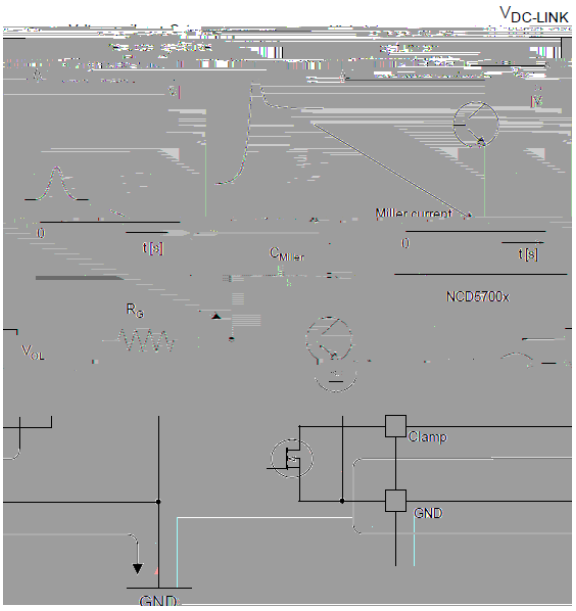


Figure 20. Current Path without Miler Clamp Protection

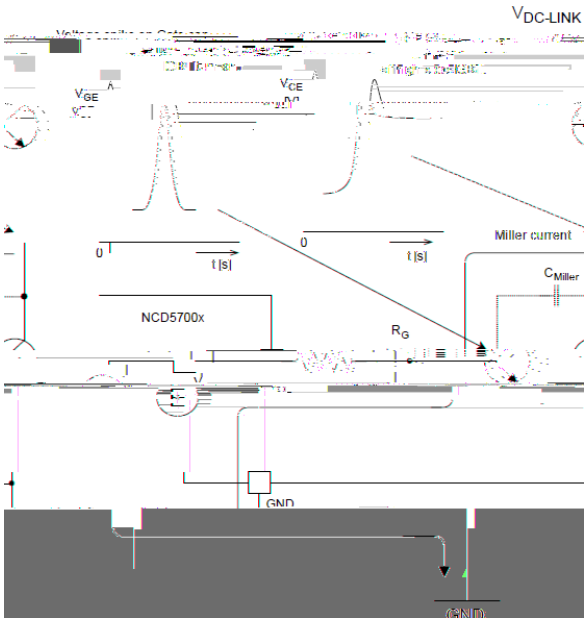


Figure 21. Current Path with Miler Clamp Protection

Non−inverting and Inverting Input Pin (IN+, IN−)

NCD57001 has two possible input modes to control IGBT. Both inputs have defined minimum input pulse width to filter occasional glitches.

- Non inverting input IN+ controls the driver output while inverting input IN is set to LOW
- Inverting input IN controls the driver output while non inverting input IN+ is set to HIGH

Warning: When the application use an independent or separate power supply for the control unit ant the input side of the driver, all inputs should be protected by a serial resistor (In case of a power failure of the driver, the driver may be damaged due to overloading of the input protection circuits)

Desaturation Protection (DESAT)

Desaturation protection ensures the protection of IGBT at short circuit. When the V_{CESAT} voltage goes up and reaches the set limit, the output is driven low and /FLT output is activated. Blanking time can be set by internal current source and an external capacitor. To avoid false DESAT triggering and minimize blanking time, fast switching diodes with low internal capacitance are recommended. All DESAT protective diodes internal capacitances builds voltage divider with the blanking capacitor.

Warning: Both external protective diodes are recommended for the protection against voltage spikes caused by IGBT transients passing through parasitic capacitances.

DESAT Circuit Parameters Specification

$$t_{BLANK} = C_{BLANK} \cdot \frac{V_{DESAT-THR}}{I_{DESAT-CHG}}$$

$$V_{DESAT-THR} > R_{S-DESAT} \cdot I_{DESAT-CHG} + V_{F\ HV\ diode} + V_{CESAT\_IGBT}$$

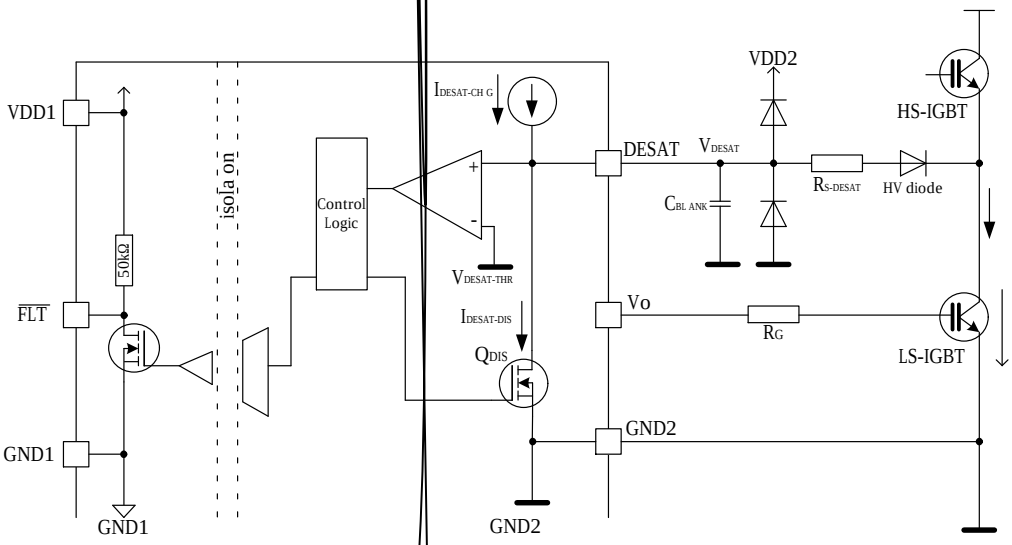
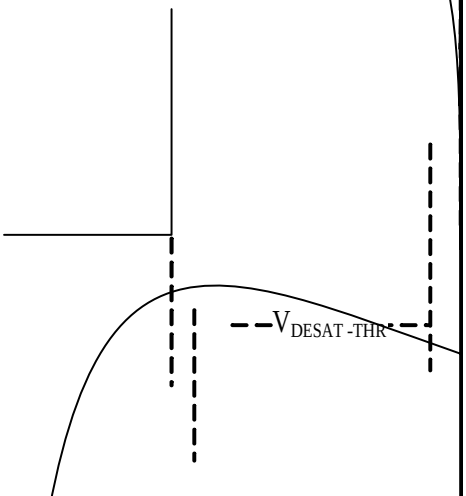


Figure 22. DESAT Protection Schematic



Fault Output Pin (FLT)

FLT open drain output provides feedback to the controller about driver DESAT protection conditions. The open drain FLT outputs of multiple NCD57001 devices can be wired together forming a single, common fault bus for interfacing directly to the microcontroller. FLT output has 50k internal pull up resistor to VDD1.

Ready Output Pin (RDY)

RDY open drain output provides feedback to the controller about driver UVLO and TSD protections conditions.

- If either side of device have insufficient supply (VDD1 or VDD2), the RDY pin output goes low; otherwise, RDY pin output is open drain.
- If the temperature crosses the TSD threshold, the RDY pin output goes low; otherwise, RDY pin output is open drain.

The open drain RDY outputs of multiple NCD57001 devices can be “OR”ed together.

Reset Input Pin (RST)

Reset input pin has internal pull up resistor to VDD1. In normal condition the RST pin is connected to HIGH, to reset FAULT conditions connect RST pin to LOW. In applications that does not allow to control the reset, RST pin should be connected to IN+, the driver will be reset by each input pulse.

RESET Input

- FLT input is used to set back FLT output after DESAT conditions disappear

Warning: When the application use an independent or separate power supply for the control unit ant the input side of the driver, all inputs should be protected by a serial resistor (In case of a power failure of the driver, the driver may be damaged due to overloading of the input protection circuits)

Power Supply (VDD1, VDD2, VEE2)

NCD57001 is designed to support two different power supply configurations, bipolar or unipolar power supply. For reliable high output current the suitable external power capacitors required. Parallel combination of 100 nF + 4.7 μF ceramic capacitors is optimal for a wide range of applications using IGBT. For reliable driving IGBT modules (containing several parallel IGBT’s) is a higher capacity required (typically 100 nF + 10 μF). Capacitors should be as close as possible to the driver’s power pins.

- In bipolar power supply the driver is typically supplied with a positive voltage of 15 V at VDD2 and negative voltage 5 V at VEE2 (Figure 24). Negative power supply prevents a dynamic turn on throughout the internal IGBT input capacitance.
- In Unipolar power supply the driver is typically supplied with a positive voltage of 15 V at VDD2. Dynamic turn on throughout the internal IGBT input capacitance could be prevented by Active Miler Clamp function. CLAMP output should be directly connected to IGBT gate (Figure 25).

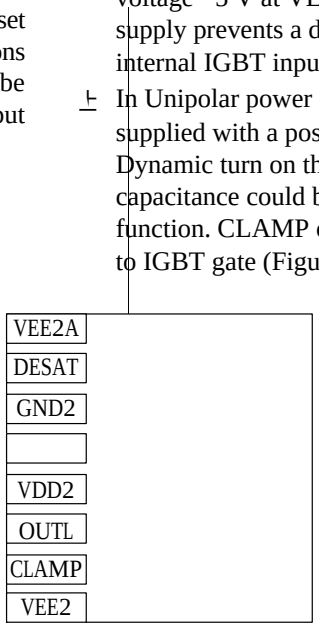


Figure 24. Bipolar Power Supply

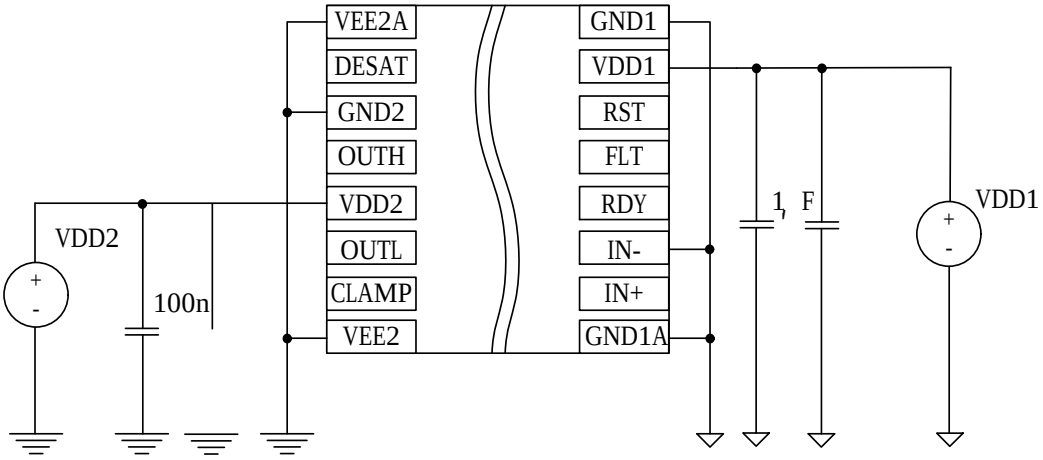


Figure 25. Unipolar Power Supply

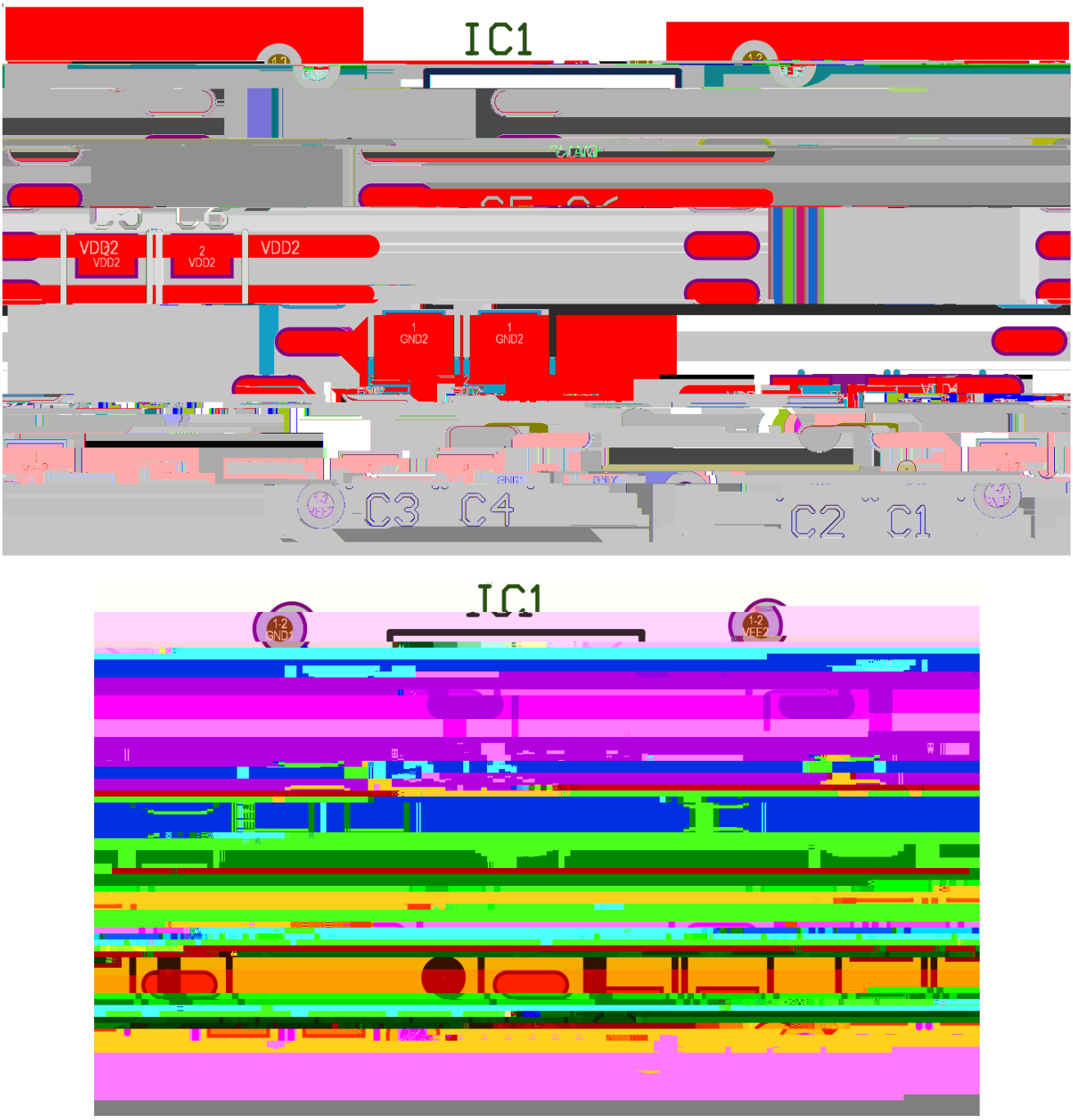


Figure 27. Recommended Basic Bipolar Power Supply PCB Design

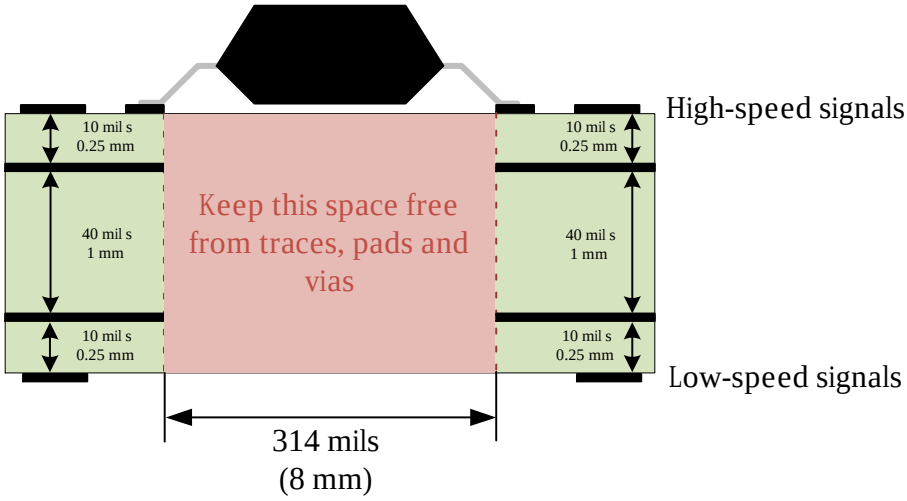


Figure 28. Recommended Layer Stack

SOIC

−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.