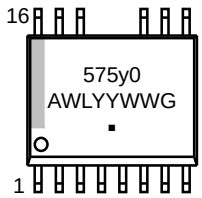
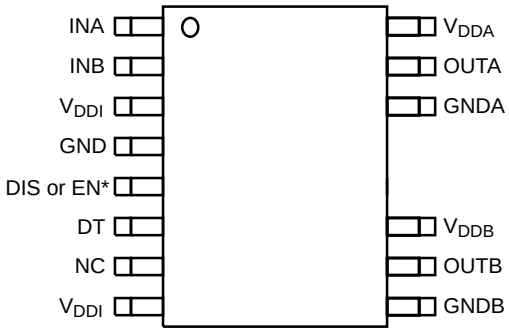
CASE 752AJ



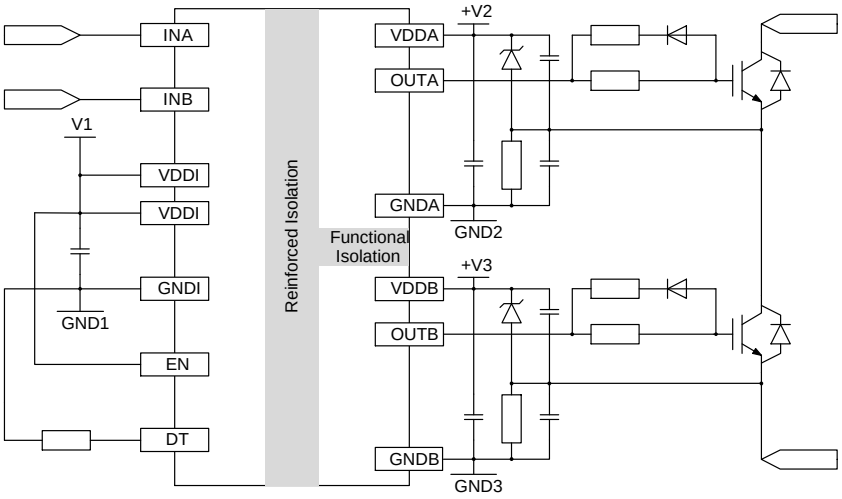
PIN CONNECTIONS



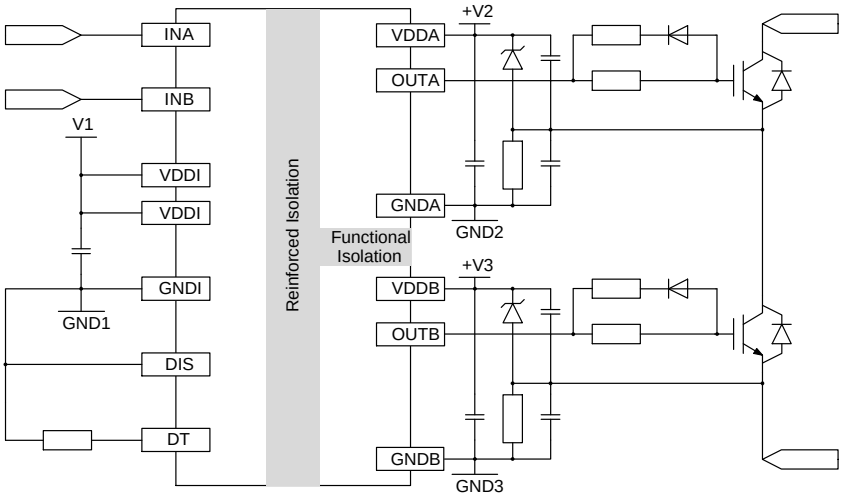
NCx575y0
x = D or V
y = 3 or 4

* depends on variant

Figure 1. Simplified Block Diagram



NCx57530



NCx57540

Figure 2. Typical Application, High and Low Side IGBT Gate Drive (Dead Time added)

Table 1. FUNCTION DESCRIPTION

Pin Name	No.	I/O	Description
INA	1	Input	A non-inverting gate driver input that defines OUTA.

Table 2. SAFETY AND INSULATION RATINGS

Symbol	Parameter		Value	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage	< 150 V_{RMS}	I–IV	–
		< 300 V_{RMS}	I–IV	–
		< 450 V_{RMS}	I–IV	–
		< 600 V_{RMS}	I–IV	–
		< 1000 V_{RMS}	I–III	–
CTI	Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1)		600	–
	Climatic Classification		40/125/21	–
	Pollution Degree (DIN VDE 0110/1.89)		2	–
V_{PR}	Input−to−Output Test Voltage, Method b, $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC		2250	V_{PK}
V_{IORM}	Maximum Working Insulation Voltage		1200	V_{PK}
V_{IOWM}	Maximum Working Insulation Voltage		870	V_{RMS}
V_{IOTM}	Highest Allowable Over Voltage		8400	V_{PK}
E_{CR}	External Creepage		8.0	mm
E_{CL}	External Clearance		8.0	mm
DTI	Insulation Thickness		17.3	μm
T_{Case}	Safety Limit Values – Maximum Values in Failure; Case Temperature		150	°C
$P_{S,INPUT}$	Safety Limit Values – Maximum Values in Failure; Input Power		264	mW
$P_{S,OUTPUT}$	Safety Limit Values – Maximum Values in Failure; Output Power		1136	mW
R_{IO}	Insulation Resistance at TS, V_{IO} = 500 V		10^9	Ω

Table 3. ABSOLUTE MAXIMUM RATINGS (Note 1) Over operating free−air temperature range unless otherwise noted

Symbol	Parameter	Minimum	Maximum	Unit
V_{DDI}−GNDI	Supply voltage, low voltage side	−0.3	22	V
V_{DDA}−GNDA	Supply voltage, high voltage side, channel A	−0.3	36	V
V_{DDB}−GNDB	Supply voltage, high voltage side, channel B	−0.3	36	V
V_{OUTA}	Gate driver output voltage, channel A	GNDA − 0.3	V_{DDA} + 0.3	V
V_{OUTB}	Gate driver output voltage, channel B	GNDB − 0.3	V_{DDB} + 0.3	V
I_{PK-SRC}	Gate−driver output sourcing current (maximum pulse width = 10 μs, minimum period = 5 ms, V_{DDA} – GNDA = V_{DDB} – GNDB = 15 V)	–	6.5	A
I_{PK-SNK}	Gate−driver output sinking current (maximum pulse width = 10 μs, minimum period = 5 ms, V_{DDA} – GNDA = V_{DDB} – GNDB = 15 V)	–	6.5	A
t_{CLP}	Maximum Short Circuit Clamping Time (I_{OUTA_CLAMP} = I_{OUTB_CLAMP} = 500 mA)	–	10	μs
V_{LIM}−GNDI	Voltage at INA, INB, DIS, DT	−0.3	V_{DDI} + 0.3	V
PD	Power Dissipation (Note 3)	–	1060	mW
T_J(max)	Maximum Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
ESDHBM	ESD Capability, Human Body Model (Note 4)	–	±4	kV
ESDCDM	ESD Capability, Charged Device Model (Note 4)	–	±2	kV
MSL	Moisture Sensitivity Level	–	1	–
T_{SLD}				

4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114).
   ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−C101).
   Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78, 25°C.
5. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 4. THERMAL CHARACTERISTICS

Parameter	Conditions	Symbol	Value	Unit
Thermal Resistance, Junction−to−Air	100 mm^2, 2 oz Copper, 1 Surface Layer	$R_{\theta JA}$	81	°C/W
	100 mm^2, 2 oz Copper, 2 Surface Layers and 2 Internal Power Plane Layers		57	

Table 5. RECOMMENDED OPERATING RANGES (Note 6)

Symbol	Parameter	Minimum	Maximum	Unit
V_{DDI}−GNDI				

Dead−Time (DT)

The dead time pin is controlling the integrated interlock and dead time generator.

- If DT pin is connected to V_{DDI} the interlock and dead time generator are disabled. The channels A and B are completely independent.
- If DT pin is floating the interlock is enabled but dead time generator is disabled. There is a minimal dead time shorter than 20 ns.
- If there is a resistor R_{DT}

In the “Overlap corrected” column the dead time is met but the signals are overlapping so just the non overlapping parts pass to the output.

Inputs INA, INB, DIS, EN

Unused inputs INA, INB, DIS should be tied to GNDI. Unused EN should be tied to V_{DDI}.

INA, INB in order to set OUTA and OUTB high, respectively (see Figures 7, 8 and Figures 9, 10).

As a side effect of this feature is that the t_{UVR} time is always prolonged by a $t_{UVR\ spread}$. The $t_{UVR\ spread}$ is the delay caused by the time before next rising edge of PWM signal comes.

Another note for the t_{UVR} is that it is valid if the V_{DD2} rises from just below $V_{UVLO\ OUT\ OFF}$ to $V_{UVLO\ OUT\ ON}$. The cold start time from $V_{DDA(B)}$ = 0 V to PWM at the output is t_{UVR} + startup time of the internal bias circuits. The whole time is about 20 μs and the internal bias circuit startup time is about 10 μs.

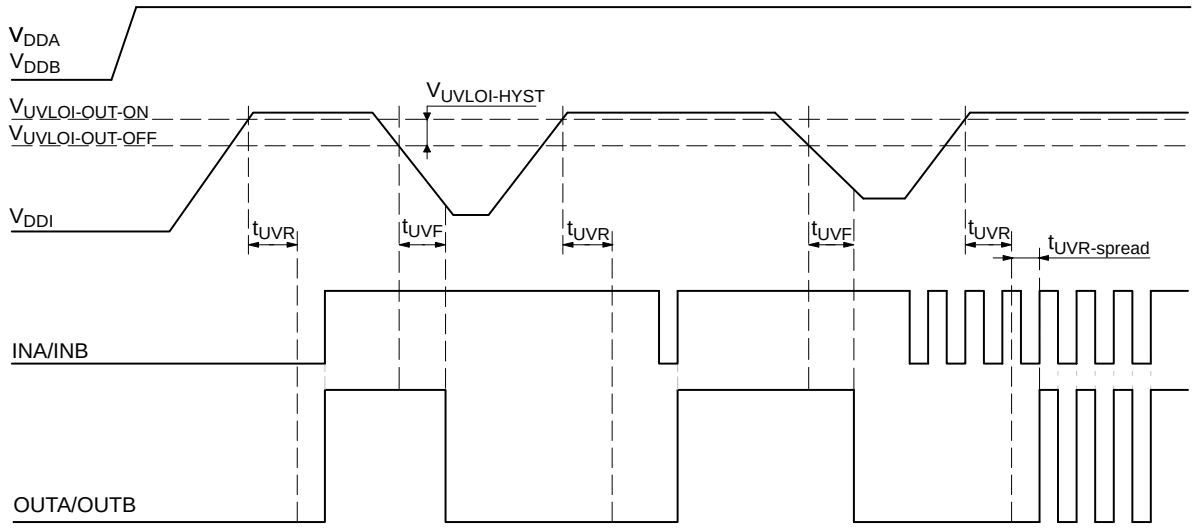


Figure 7. Output Ramp−up and Ramp−down Times during UVLOI

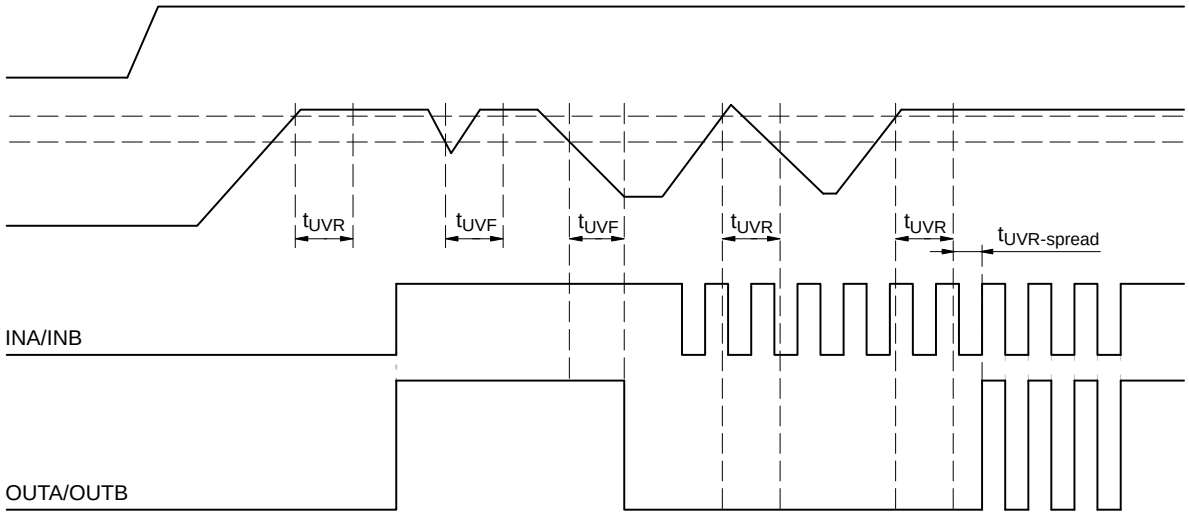


Figure 8. V_{DDI} Glitch Filtering

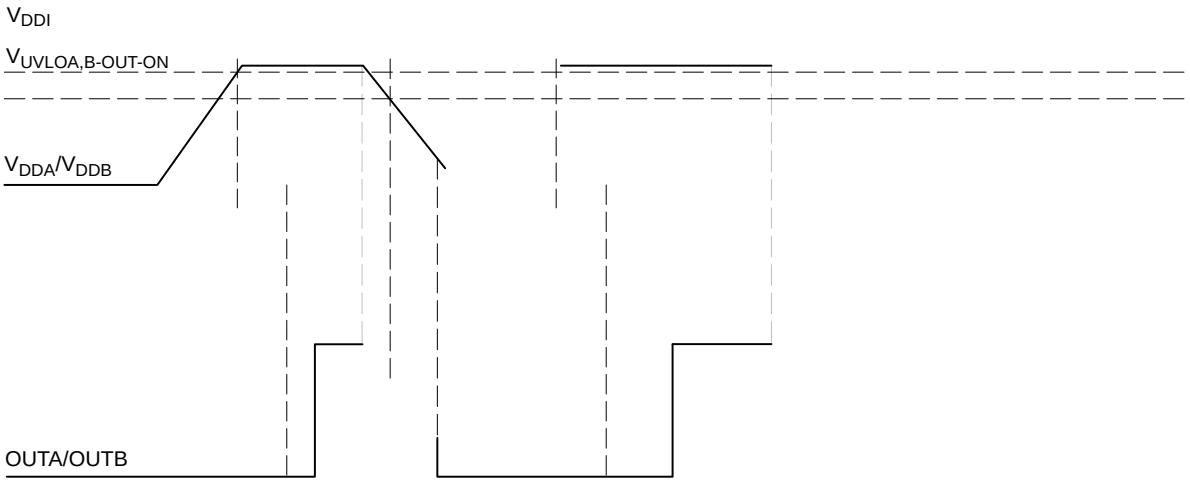
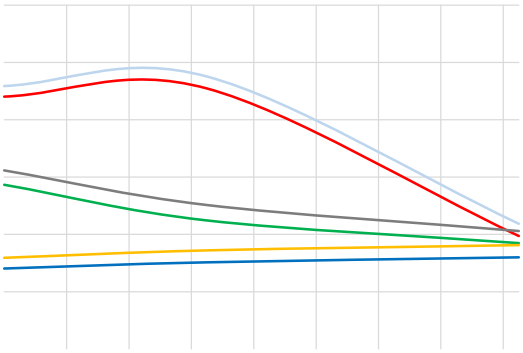


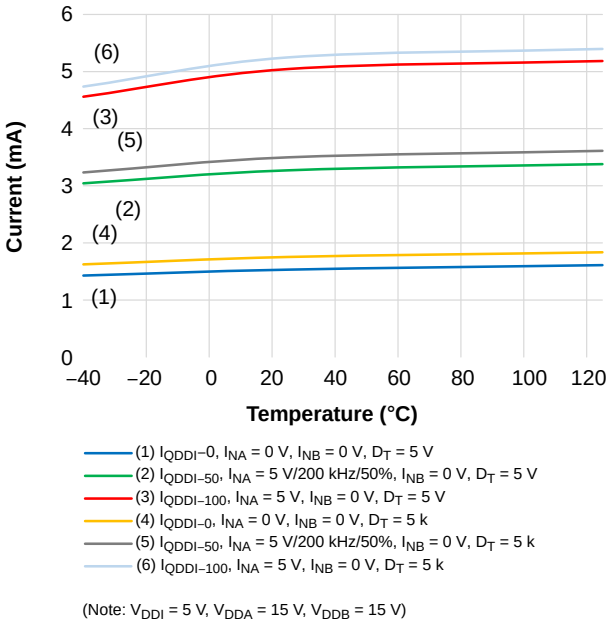
Figure 9. Output Ramp−up and Ramp−down Times during UVLOA, UVLOB

Figure 10. V_{DDA}/V_{DDB} Glitch Filtering

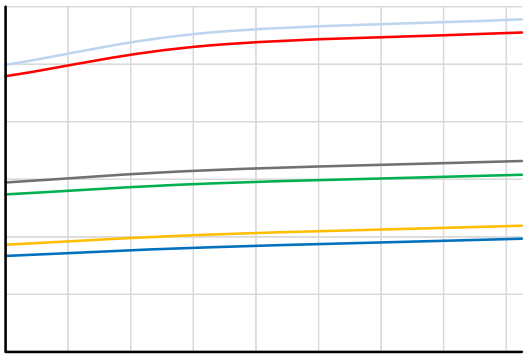
- Low inductance (wide and short) traces from OUTA (OUTB) to R_G

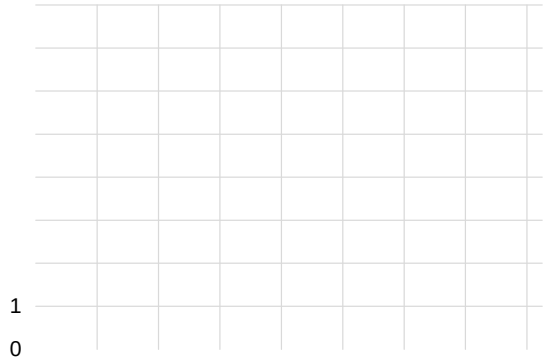
TYPICAL CHARACTERISTICS



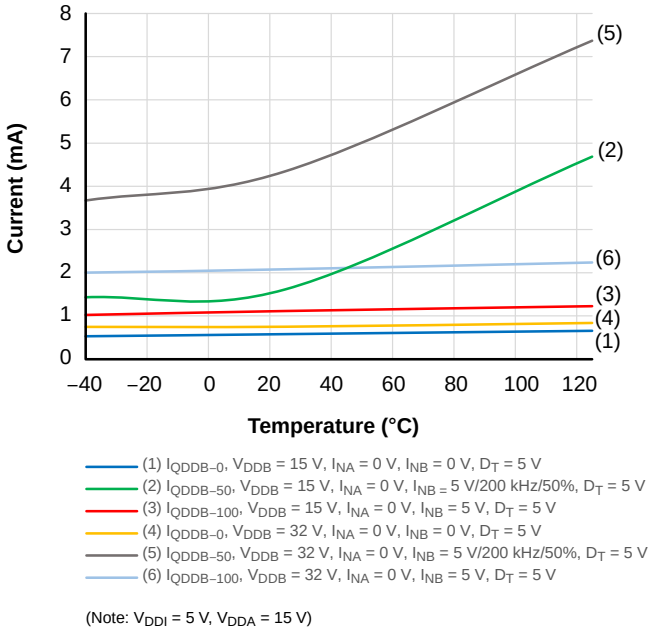


(Note: V_{DDI} = 5 V, V_{DDA} = 15 V, V_{DDB} = 15 V)



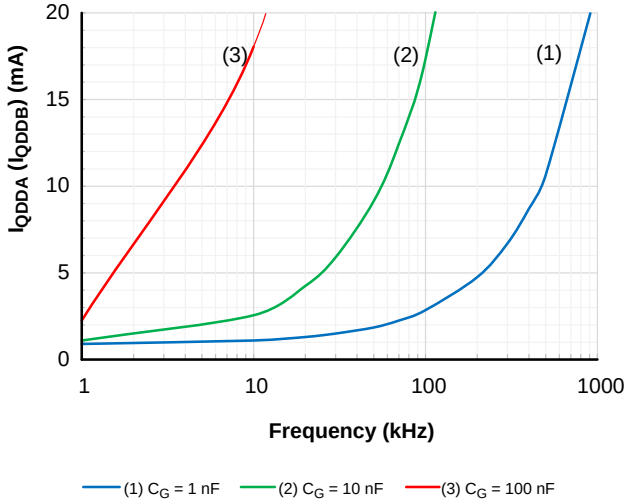


TYPICAL CHARACTERISTICS



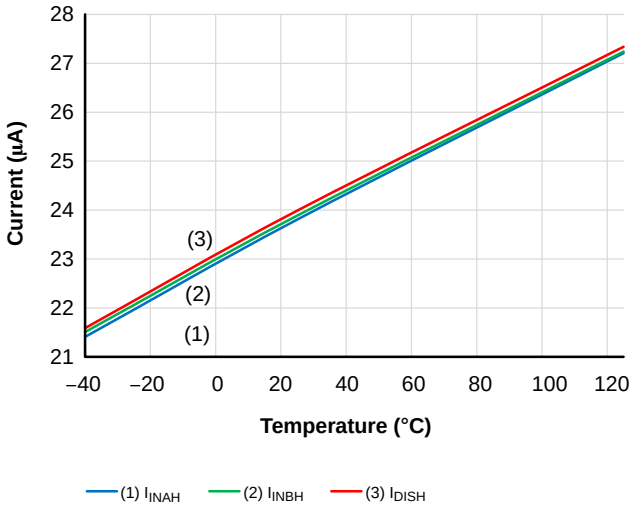
(Note: V_{DDI} = 5 V, V_{DDA} = 15 V)

Figure 17. I_{QDDB} Supply Current



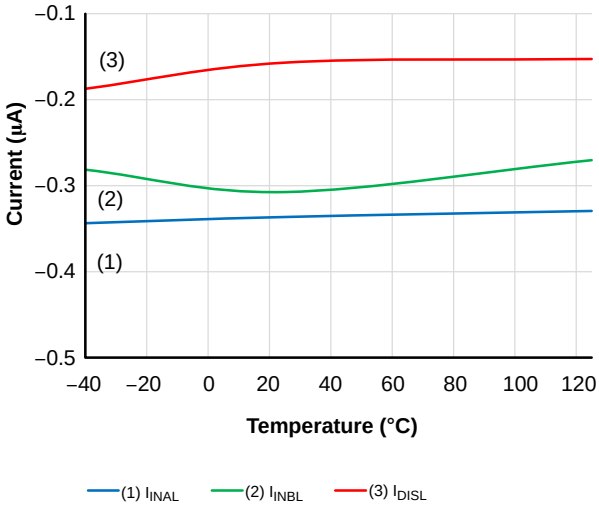
(Note: V_{DDI} = 5 V, V_{DDA} = 15 V, V_{DDB} = 15 V, I_{NA} = 5 V/50%, I_{NB} = 0 V, D_T = V_{DDI}, DIS = GNDI, R_G = 0 Ω)

Figure 18. I_{QDDA} (I_{QDDB}) Supply Current vs. Switching Frequency



(Note: V_{DDI} = V_{INA} = V_{INB} = V_{DIS} = 3.3 V, V_{DDA} = V_{DDB} = 15 V)

Figure 19. Input Bias Current − Logic “1”



(Note: V_{DDI} = 3.3 V, V_{INA} = V_{INB} = V_{DIS} = GNDI, V_{DDA} = V_{DDB} = 15 V)

Figure 20. Input Bias Current − Logic “0”

TYPICAL CHARACTERISTICS

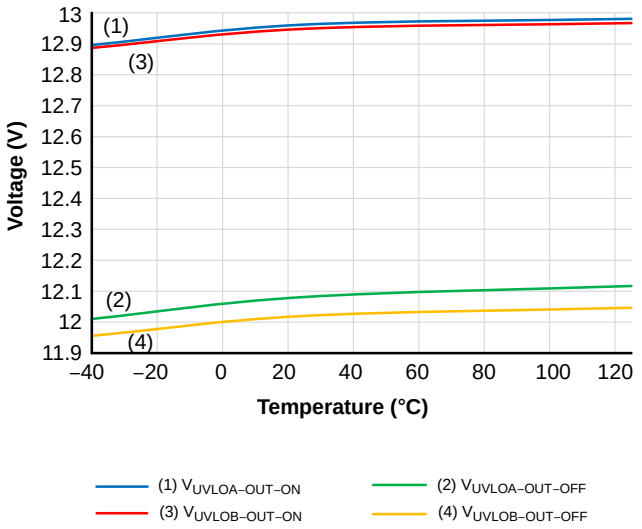


Figure 25. NCx57540 UVLOA and UVLOB Threshold Voltage

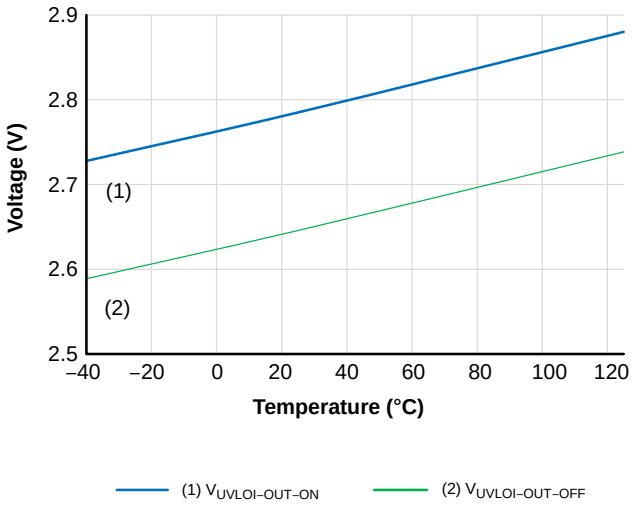


Figure 26. UVLOI Threshold Voltage

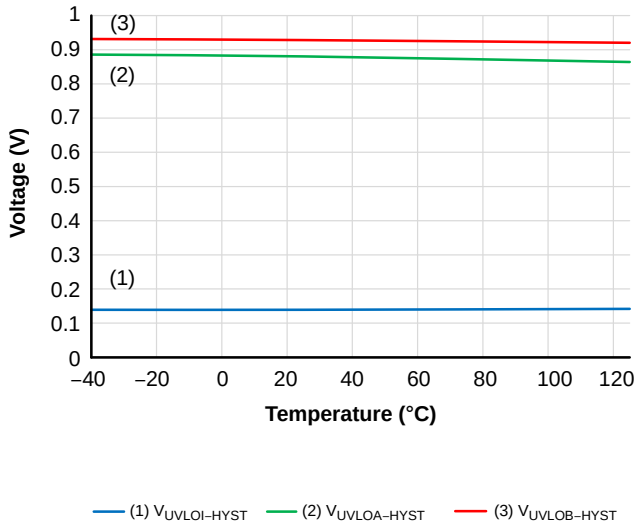


Figure 27. UVLOx Enable/Disable Voltage Hysteresis

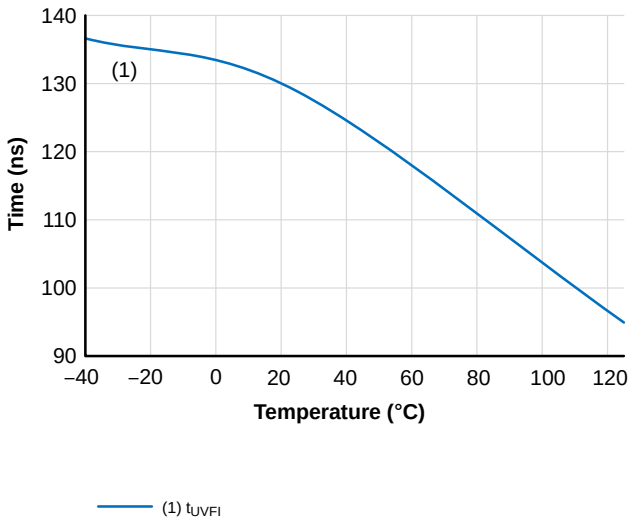


Figure 28. UVLOI Fall Delay

TYPICAL CHARACTERISTICS

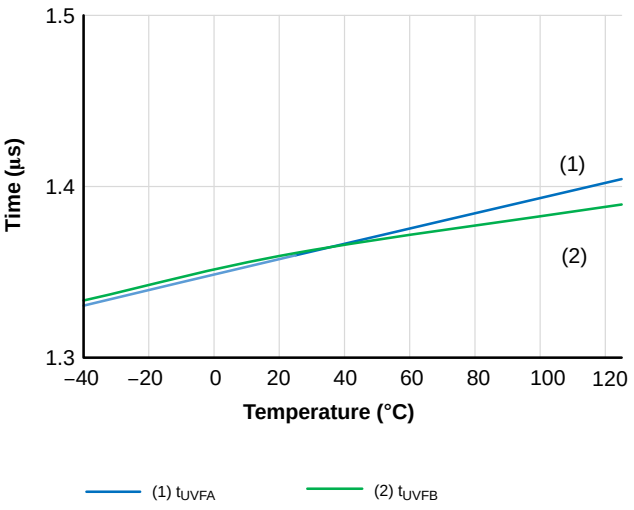


Figure 29. UVLOA and UVLOB Fall Delay

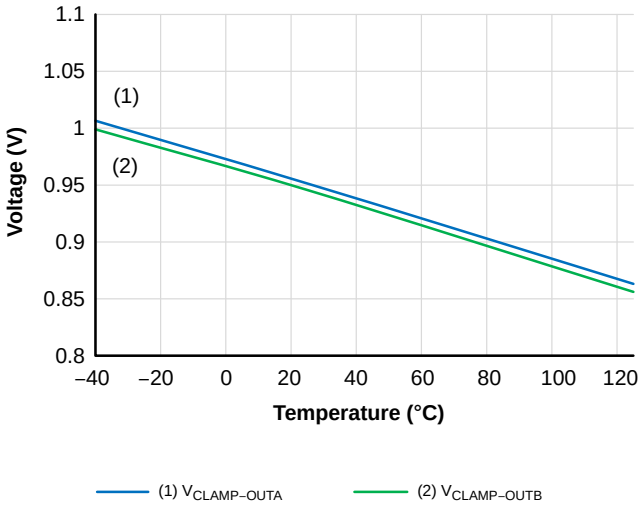


Figure 30. IGBT Short Circuit Clamping Voltage

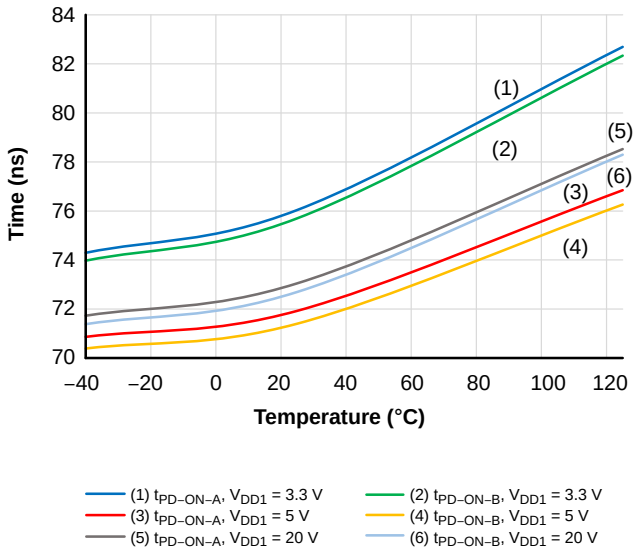


Figure 31. Propagation Delay Turn−on

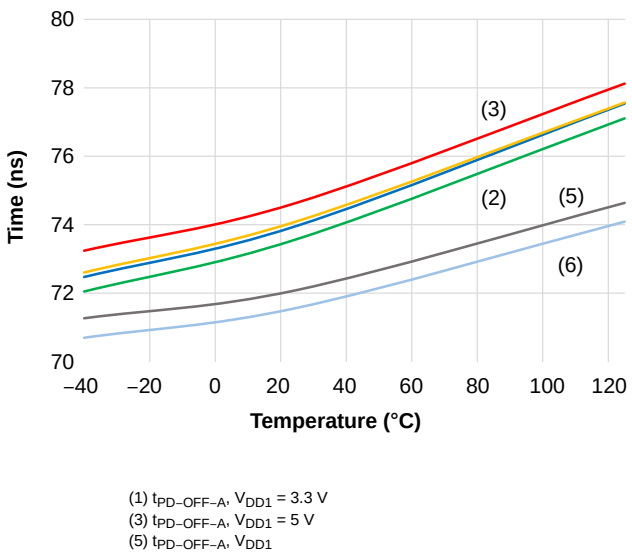
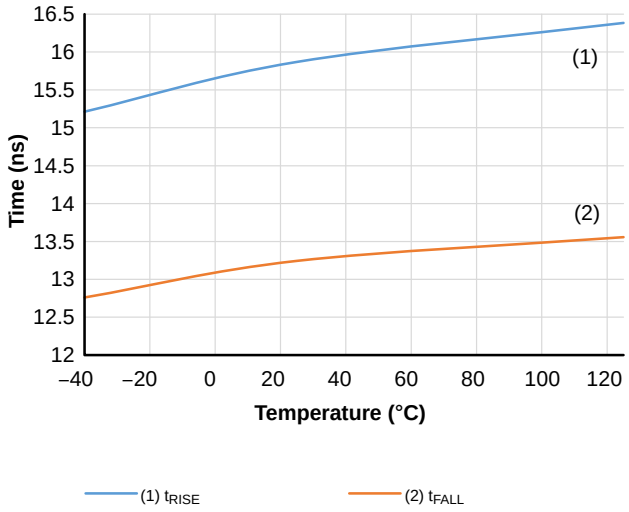
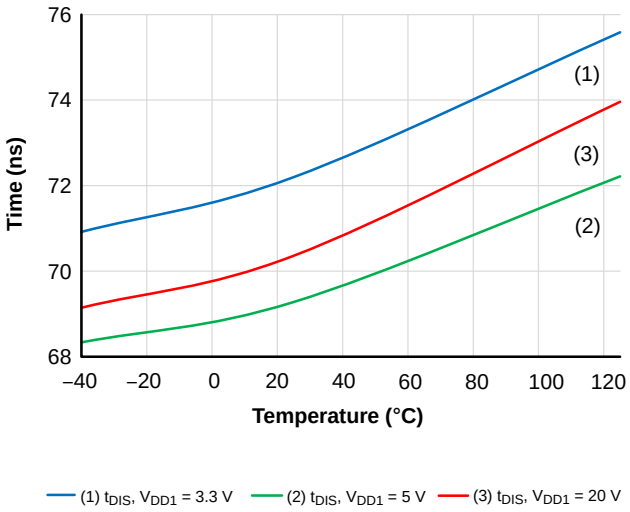
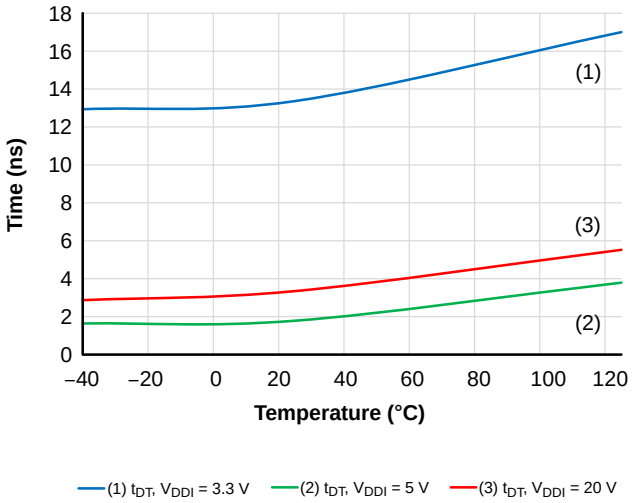


Figure 32. Propagation Delay Turn−off

TYPICAL CHARACTERISTICS







(Note: V_{INA} is inverted from V_{INB}, V_{DDA} = V_{DDB} = 15 V)

SCALE 1:1

SOIC−16 WB LESS PINS 12 & 13
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DATE 17 FEB 2021