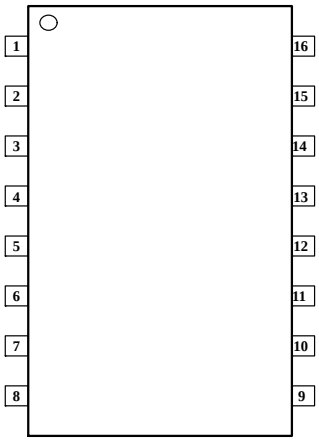
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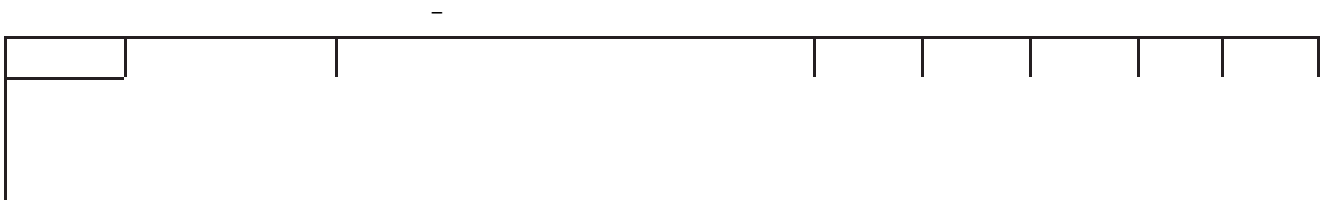
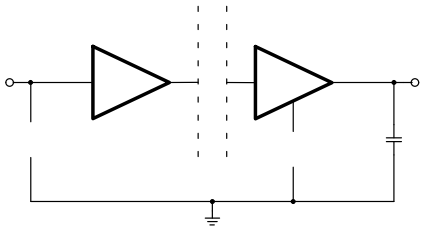
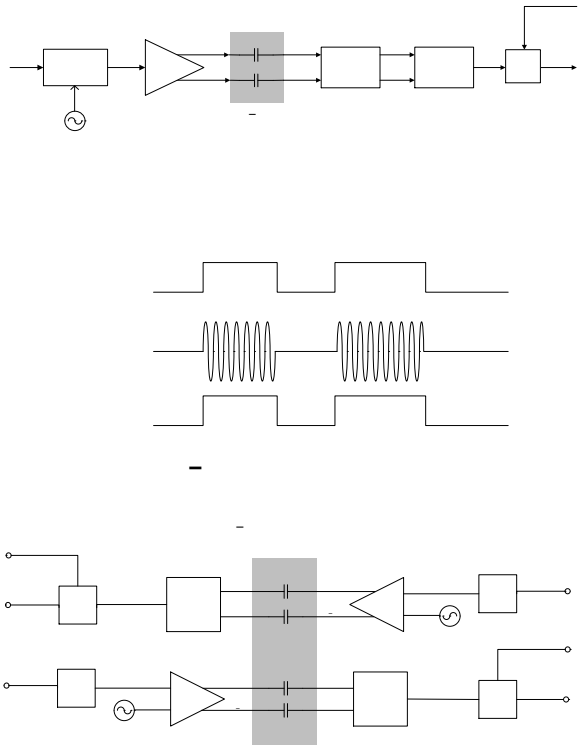




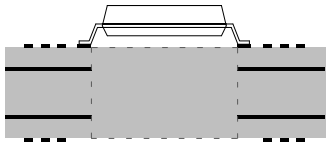
NCID9211 is a dual−channel digital isolator that enables bi−directional communication between two isolated circuits. It uses off−chip ceramic capacitors that serve both as the isolation barrier and as the medium of transmission for signal switching using on−off keying (OOK) technique, illustrated in the single channel operational block diagram in Figure 13.

At the transmitter side, the V_{IN} input logic state is modulated with a high frequency carrier signal. The resulting signal is amplified and transmitted to the isolation barrier. The receiver side detects the barrier signal and demodulates it using an envelope detection technique. The output signal determines the V_O output logic state when the output enable control EN is at high. When EN is at low, output V_O is at high impedance state. V_O is at default state low when the power supply at the transmitter side is turned off or the input V_{IN} is disconnected.



Layout of the digital circuits relies on good suppression of unwanted noise and electromagnetic interference. It is recommended to use 4−layer FR4 PCB, with ground plane below the components, power plane below the ground plane, signal lines and power fill on top, and signal lines and ground fill at the bottom. The alternating polarities of the layers creates interplane capacitances that aids the bypass capacitors required for reliable operation at digital switching rates.

In the layout with digital isolators, it is required that the isolated circuits have separate ground and power planes. The section below the device should be clear with no power, ground or signal traces. Maintain a gap equal to or greater than the specified minimum creepage clearance of the device package.



For NCID9211, it is highly advised to connect at least a pair of low ESR supply bypass capacitors, placed within 2mm from the power supply pins 1 and 16 and ground pins 2 and 15. Recommended values are 1 μF and 0.1 μF, respectively. Place them between the V_{DD} pins of the device and the via to the power planes, with the higher frequency, lower value capacitor closer to the device pins. Directly connect the device ground pins 1, 8, 9 and 15 by via to their corresponding ground planes.

SOIC16 W