Features

- Off Chip Capacitive Isolation to Achieve Reliable High Voltage Insulation
  - DTI (Distance Through Insulation): 0.5 mm
  - Maximum Working Insulation Voltage: 2000 V_{peak}
- Bi directional Communication
- 100 kV/μs Minimum Common Mode Rejection
- 8 mm Creepage and Clearance Distance to Achieve Reliable High Voltage Insulation
- Specifications Guaranteed Over 2.5 V to 5.5 V Supply Voltage and 40 C to 125 C Extended Temperature Range
- Over Temperature Detection
- Output Enable Function (Primary and Secondary side)

capacitors and coreless transformers. The result is a combination of the electrical performance benefits that digital isolators offer with the

PIN CONFIGURATION

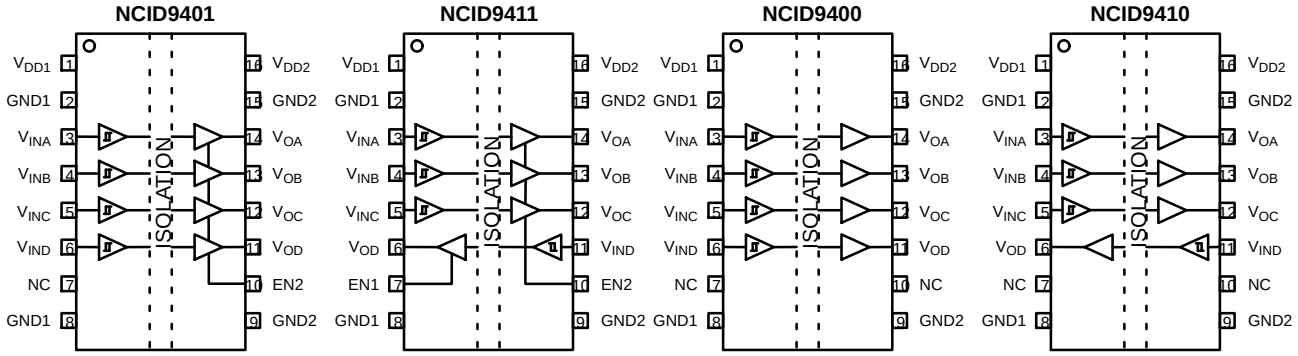


Figure 2. Pin and Channel Configuration

PIN DEFINITION

Name	Pin No. NCID9401	Pin No. NCID9411	Pin No. NCID9400	Pin No. NCID9410	Description
V_{DD1}	1	1	1	1	Power Supply, Side 1
GND1	2	2	2	2	Ground Connection for V_{DD1}
V_{INA}	3	3	3	3	Input, Channel A
V_{INB}	4	4	4	4	Input, Channel B
V_{INC}	5	5	5	5	Input, Channel C
V_{IND}	6	11	6	11	Input, Channel D
EN1	–	7	–	–	Output Enable 1
NC	7	–	7	7	No Connect
GND1	8	8	8	8	Ground Connection for V_{DD1}
GND2	9	9	9	9	Ground Connection for V_{DD2}
NC	–	–	10	10	No Connect
EN2	10	10	–	–	Output Enable 2
V_{OD}	11	6	11	6	Output, Channel D
V_{OC}	12	12	12	12	Output, Channel C
V_{OB}	13	13	13	13	Output, Channel B
V_{OA}	14	14	14	14	Output, Channel A
GND2	15	15	15	15	Ground Connection for V_{DD2}
V_{DD2}	16	16	16	16	Power Supply, Side 2

ABSOLUTE MAXIMUM RATINGS (T_A = 25 C unless otherwise specified)

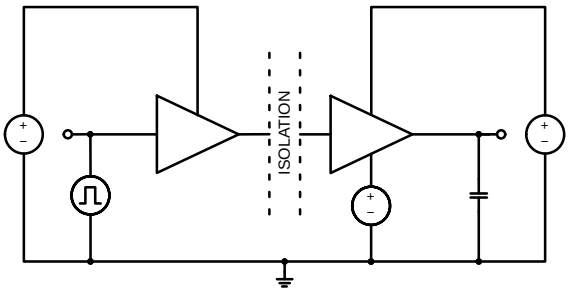
Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−55 to +150	C
T_{OPR}	Operating Temperature	−40 to +125	C
T_J	Junction Temperature	−40 to +150	C
T_{SOL}	Lead Solder Temperature (Refer to Reflow Temperature Profile)	260 for 10 s	C
V_{DD}	Supply Voltage (V_{DDx})	−0.5 to 6	V
V	Voltage (V_{INx}, V_{Ox}, ENx)	−0.5 to 6	V

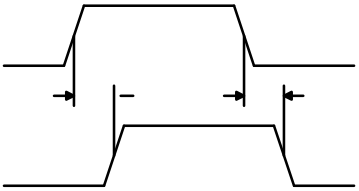
SWITCHING CHARACTERISTICS – NCID9411/NCID9410

Apply over all recommended conditions, T_A =−40 C to +125 C unless otherwise specified. All typical values are measured at T_A = 25 C.

Symbol	Parameter	Ch	Conditions	Min	Typ	Max	Unit	Figure
t_{PHL}	Propagation Delay to Logic Low Output (Note 8)	A, B, C	V_{DD} = 5 V, C_L = 15 pF					

TEST CIRCUITS





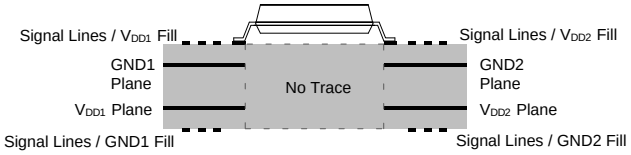


Figure 20. 4−Layer PCB for Digital Isolator

Figure 21. Placement of Bypass Capacitors

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