Safety Features

- Thermal Shutdown
- Non−latching, Over−Voltage Protection (3 Prog Levels)
- Over Current Limitation
- Low Duty−Cycle Operation if the Bypass Diode is Shorted
- Open Ground Pin Fault Monitoring
- Pin CS shorted to GND or open Monitoring
- Pin ZCD open tested before controller starts
- Controller not allowed to start if MULT pin is left open

Typical Applications

- PC Power Supplies
- Lighting Ballasts (LED, Fluorescent)
- Flat TV
- All Off Line Appliances Requiring Power Factor Correction
  Several product configurations coded with three letters (L_1,L_2, L_3) marked on the package will be available

Table 1. NCL2801 1ST LETTER CODING OF PRODUCT VERSIONS

L_1	Soft OVP (% of V_{REF})	Fast OVP (% of V_{REF})

Table 2. NCL2801 2 LETTER CODING OF PRODUCT VERSIONS

L2	VCC Startup Level (V)	DRE (After Startup)	DRE (During Startup)

Table 3. NCL2801 3RD LETTER CODING OF PRODUCT VERSIONS

L3	Brown−in & Brown−out	Line Range Detection w/ 2−level Line Feed−Forward	Failure protection (CS open/short, ZCD open, GND open)

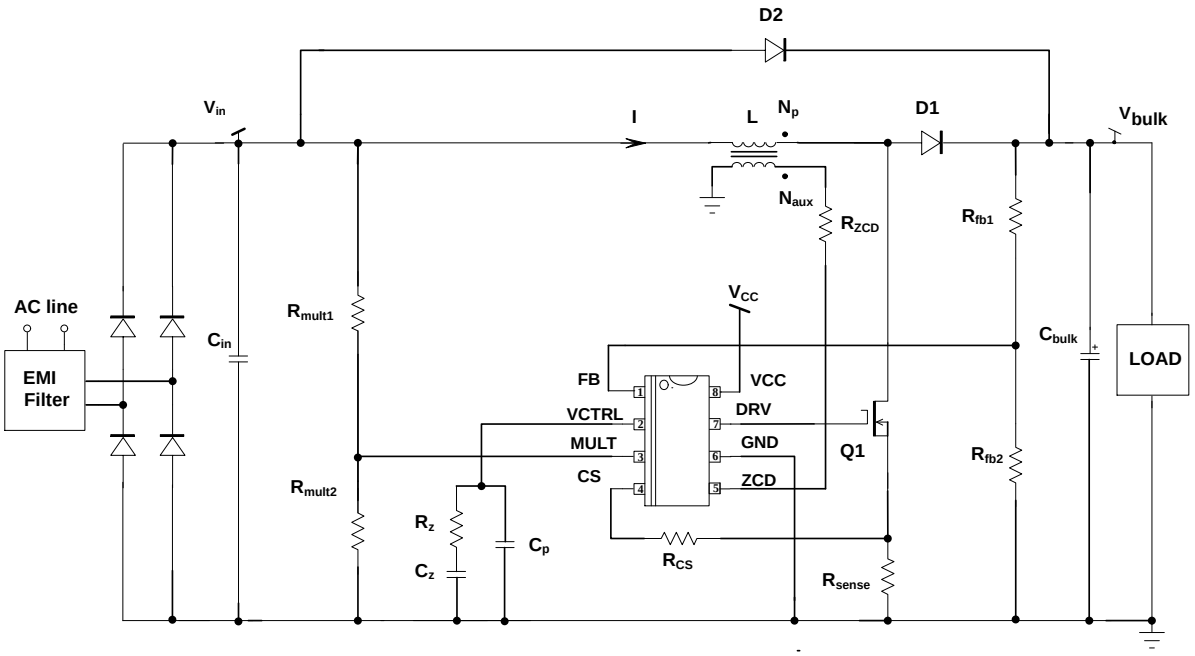


Table 5. MAXIMUM RATINGS TABLE

Symbol	Pin	Rating	Value	Unit
			–	

Table 6. ELECTRICAL CHARACTERISTICS _ ° °

Symbol	Rating	Min	Typ	Max	Unit

Table 6. ELECTRICAL CHARACTERISTICS – ° °

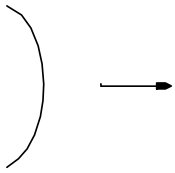
Symbol	Rating	Min	Typ	Max	Unit
	–				
					µ

Table 6. ELECTRICAL CHARACTERISTICS – ° °

Symbol	Rating	Min	Typ	Max	Unit
R_{CS} VALUE IDENTIFICATION REFERENCE VOLTAGES					
	Ω				

Table 6. ELECTRICAL CHARACTERISTICS _ ° °

Symbol	Rating	Min	Typ	Max	Unit
	Ω				
	Ω				
	Ω				
	Ω				
	Ω				



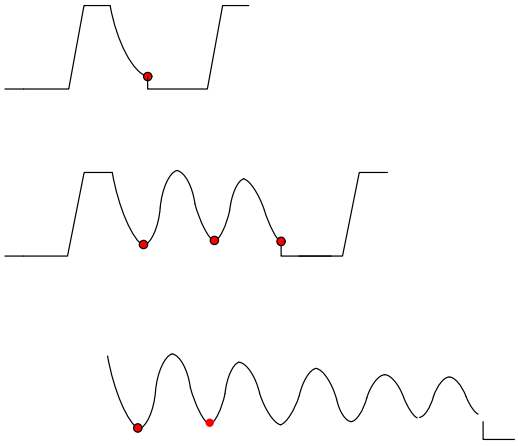
DETAILED OPERATING DESCRIPTION

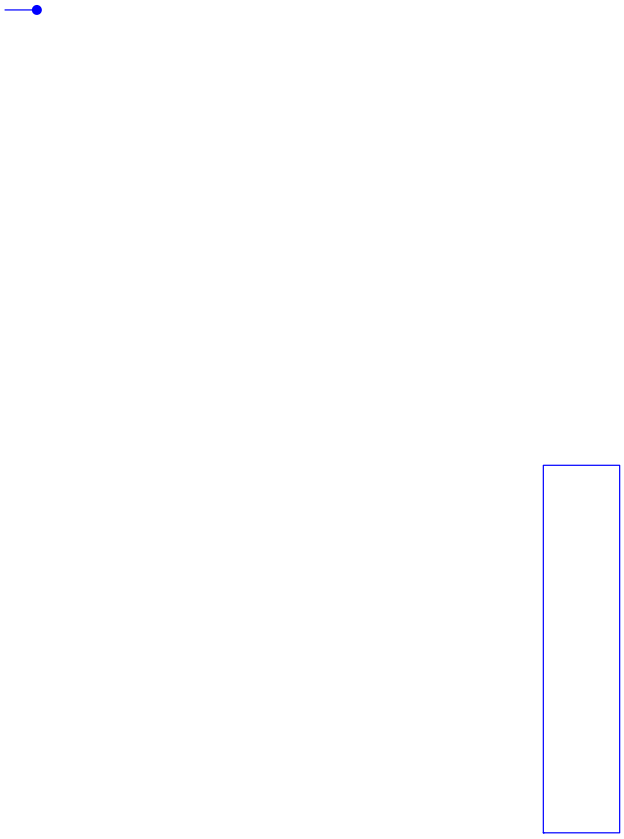
Introduction

NCL2801 is designed for working with LED Lighting applications coping with high ripple voltage on bulk capacitor and providing optimized line current THD and good efficiency. In addition, it incorporates protection features for robust operation. More generally, NCL2801 is ideal in systems where cost−effectiveness, reliability, low line current THD, low stand−by power and high efficiency are key requirements:

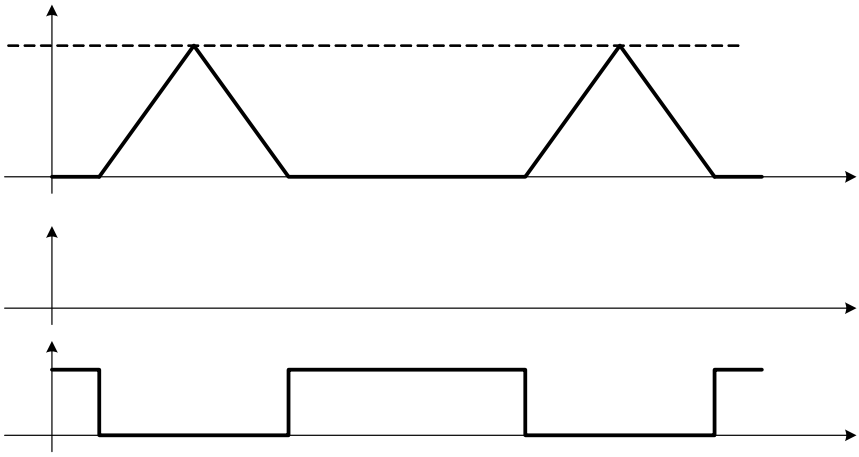
- Valley Count Frequency Fold−back: NCL2801 is designed to drive PFC boost stages in so−called *V*alley *C*ount *F*requency *F*old−back (*VCFF*). In high load current condition, the circuit classically operates in *Cr*itical conduction *M*ode (*CrM*) also called 1st valley

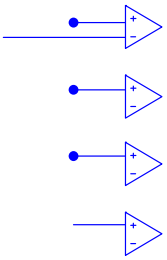
- Safety Protections: Permanently monitoring the input and output voltages, the MOSFET current and the die temperature to protect the system from possible over−stress makes the PFC stage extremely robust and





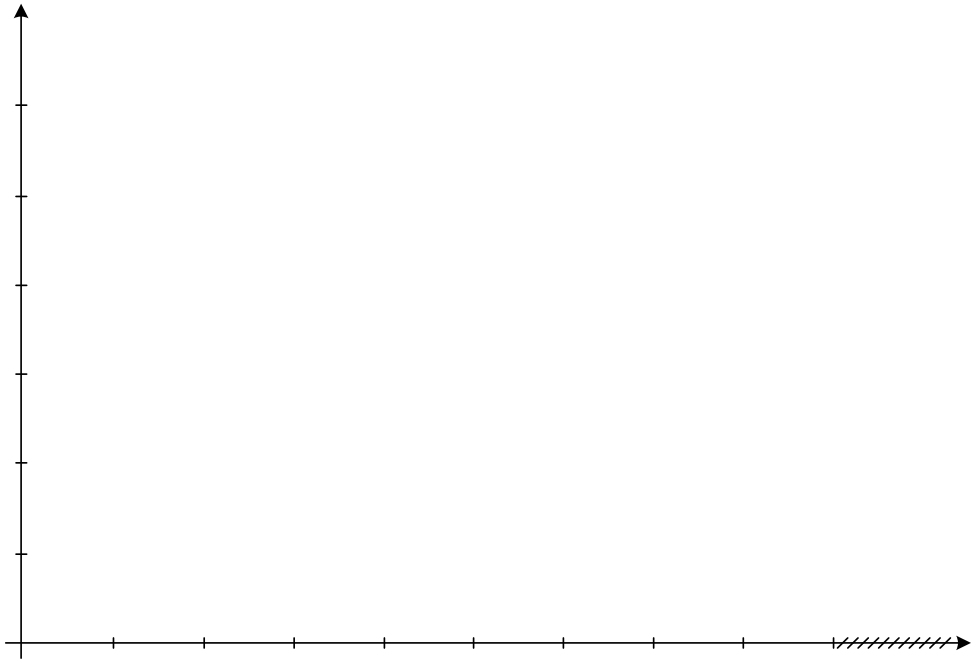
VCTRL pin voltage level, starts adding a dead−time t_{DT}. The system adjusts the on−time t_{ON} (by means of peak current control) versus t_{DT} (see Figure 5) and consequently the output power in order to ensure that the instantaneous mains current remains in phase with the mains instantaneous voltage (creating a unity PF).





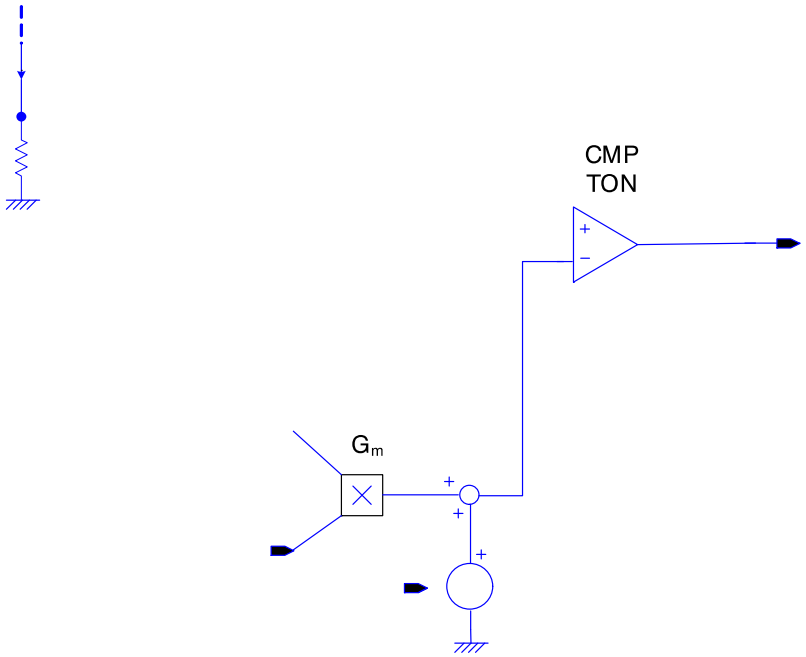
peak−to−peak ripple voltage stays under $V_{CTRL,hyst}$ there will be no valley hopping.

$V_{CTRL,hyst}$ can be calculated for each frequency foldback option determined by R_{CS} value from the thresholds specified in Table 7. While the hysteresis between two adjacent valley numbers is constant for one frequency foldback option, it decreases for options having a lower CrM to DCM V_{CTRL} threshold. This should not be a problem as the two times mains frequency ripple also decreases when VCTRL pin voltage decreases which results from output power decrease. We can also mention looking at Figure 7 and the specified frequency foldback thresholds of Table 7 that $V_{CTRL,th,56}$ which is the V_{CTRL} threshold at which we force counting six valleys, has always the same value. This threshold is also called $V_{CTRL,ADT}$ because when VCTRL pin voltage falls under this threshold, an analog dead−time starts to be added to the dead−time determined by counting six valleys. The lower VCTRL pin voltage goes under $V_{CTRL,ADT}$ threshold, the more analog dead time is added. An example on how the analog dead time can be added is shown in the circuit of Figure 4 and the correspond power MOSFET drain voltage is shown in Figure 3.



NCL2801 On time Modulation and V_{TON} Processing Circuit

Let's analyze the ac line current absorbed by the PFC boost stage. The initial inductor current at the beginning of each switching cycle is always zero. The coil current ramps up when the MOSFET is *on*. The slope is (V_{in}/L) where L is the coil inductance. At the end of the on−time (t_1), the inductor starts to demagnetize. The inductor current ramps down until it reaches zero. The duration of this phase is (t_2). In some cases, the system enters then the dead−


CMP
TON
Gm

level dependent multiplier gain values act as a two−level line feed forward.

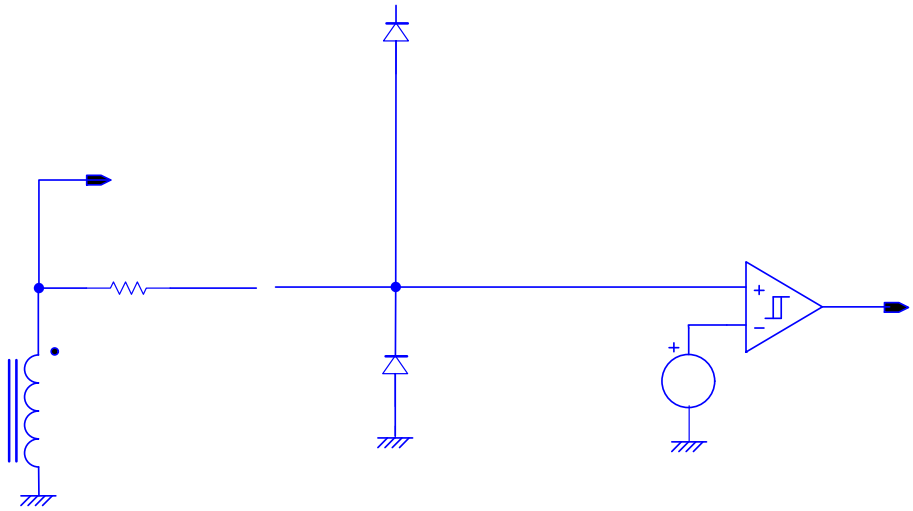
NCL2801 Maximum on time

In order to avoid the on−time to go too high close to line voltage zero crossing, a V_{CTRL} dependent maximum on time circuitry has been added. The on−time limiting values are linearly depending on VCTRL pin voltage as follows:

30 μs @V_{CTRL} = 4.5 V and 5 μs @V_{CTRL} = 0.55 V

NCL2801 Regulation Block and Output Voltage Control

A trans−conductance error amplifier (OTA) with access to its inverting input (FB pin) and to its output pin (VCTRL pin) is provided. It features a typical trans−conductance gain



soldering, an internal pull down current source pulls down the FB voltage under the UVP threshold and the controller is turned off.

- Detection the ZCD pin improper connection
  If the ZCD pin is floating or shorted to GND it is detected by internal circuitry and the circuit stops operating.
- Boost or bypass diode short

The controller addresses the short situations of the boost and bypass diodes (a bypass diode is generally placed between the input and output high−voltage rails to divert this inrush current). Practically, the overstress protection is implemented to detect such conditions and forces a low duty−cycle operation until the fault is gone.

Table 8. NCL2801 ORDERING TABLE

Ordering Part No.	Soft OVP	Fast OVP (%)	V_{CC} Start (V)	DRE (after start)	DRE (during start)	Brown Out	Line Range Detect	Package	Shipping
								– –	

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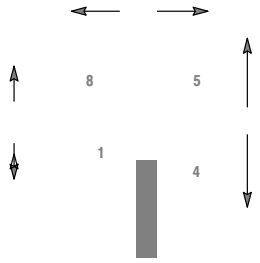
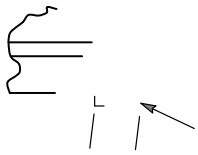
CASE 751−07
ISSUE AK

DATE 16 FEB 2011





SEATING
PLANE