## Safety Features

- Thermal Shutdown
- Non–latching, Over–Voltage Protection (3 Prog Levels)
- Over Current Limitation
- Low Duty–Cycle Operation if the Bypass Diode is Shorted
- Open Ground Pin Fault Monitoring
- Pin CS shorted to GND or open Monitoring
- Pin ZCD open tested before controller starts
- Controller not allowed to start if MULT pin is left open

#### **Typical Applications**

- PC Power Supplies
- Lighting Ballasts (LED, Fluorescent)
- Flat TV
- All Off Line Appliances Requiring Power Factor Correction

Several product configurations coded with three letters  $(L_1, L_2, L_3)$  marked on the package will be available

### Table 1. NCL2801 1<sup>ST</sup> LETTER CODING OF PRODUCT VERSIONS

L <sub>1</sub>	Soft OVP (% of V <sub>REF</sub> )	Fast OVP (% of V <sub>REF</sub> )
А	Disabled	112.5
В	Disabled	110.0
C (default)	105.0	107.0

1. The NCL2801 SO8 package is marked  $L_1L_2L_3$ 

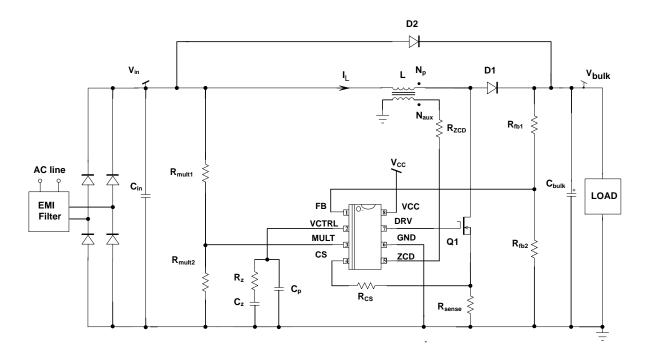
## Table 2. NCL2801 2<sup>ND</sup> LETTER CODING OF PRODUCT VERSIONS

L2	VCC Startup Level (V)	DRE (After Startup)	DRE (During Startup)
А	17.0	NO	YES
В	17.0	YES	YES
С	12.5	NO	YES
D (default)	12.5	YES	YES
E	10.5	NO	YES
F	10.5	YES	YES

2. The NCL2801 SO8 package is marked L<sub>1</sub>L<sub>2</sub>L<sub>3</sub>

## Table 3. NCL2801 3<sup>RD</sup> LETTER CODING OF PRODUCT VERSIONS

L3	Brown-in & Brown-out	Line Range Detection w/ 2-level Line Feed-Forward	Failure protection (CS open/short, ZCD open, GND open)
A (default)	YES	YES	Enabling latch protection
В	YES	NO	Enabling latch protection
С	NO	YES	Enabling latch protection
D	NO	NO	Enabling latch protection
E	YES	YES	Disabling latch protection and MULT OVP
F	YES	YES	Enabling non latch protection





#### Table 5. MAXIMUM RATINGS TABLE

Symbol	Pin	Rating	Value	Unit
FB	1	Feedback Pin	-0.3, +9	

Table 6. ELECTRICAL CHARACTERISTICS (Conditions: VCC = 18 V,  $T_J = -40^{\circ}C$  to +125°C, unless otherwise specified) (Note 6)

Symbol Rating Min Typ Max Unit	
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Symbol	Rating	Min	Тур	Max	Unit
VCS_OCP_HL(th)	Current Sense Voltage Reference when High Line is detected [**A]&[**C] Options At tLEB,OCP**	0.53	0.58	0.66	v
$V_{CS_OVS_HL(th)}$	Current Sense Overstress Voltage Reference when High Line is detected [**A]&[**C] Options At t <sub>LEB,OVS</sub>	0.79	0.87	0.97	v
t <sub>LEB,OCP</sub>	Leading edge Blanking Time for current control	125	200	275	ns
t <sub>LEB,OVS</sub>	Leading edge Blanking Time for Overstress	50	100	150	ns
tocp	Over–Current Protection Delay from $V_{CS}$ > $V_{CS(th)}$ to DRV low Test: $V_{CS}$ > $V_{CS}$ + 100 mV	10	40	200	ns
t <sub>WDG(OS)</sub>	Watch Dog Timer in "OverStress" Situation	400	800	1200	μs

**Table 6. ELECTRICAL CHARACTERISTICS** (Conditions: VCC = 18 V,  $T_J = -40^{\circ}C$  to +125°C, unless otherwise specified) (Note 6)

Table 6. ELECTRICAL CHARACTERISTICS (Conditions: VCC = 18 V,  $T_J = -40^{\circ}C$  to +125°C, unless otherwise specified) (Note 6)

Symbol	Rating	Min	Тур	Max	Unit
R <sub>CS</sub> VALUE IDENTIF	ICATION REFERENCE VOLTAGES				
I <sub>RCS</sub>	Internal current sourced by CS pin into a 1% $\rm R_{CS}$ resistor just before the startup generates a voltage drop $\rm V_{CS}$	0.96	1.0	1.04	mA
V <sub>RCS,REF,1</sub>	Internal voltage reference for identifying the $R_{CS}$ resistor value CS pin is said shorted to GND if $V_{CS} < V_{RCS,REF,1}$	20	50	100	mV
V <sub>RCS,REF,2</sub>	Internal voltage reference for identifying the R <sub>CS</sub> resistor value $R_{CS}$ = 150 $\Omega$ if $_{RCS,REF,1}$ < V <sub>CS</sub> < V <sub>RCS,REF,2</sub>	180	230		

Symbol	Rating	Min	Тур	Max	Unit			
V <sub>CTRL,th,56, 330</sub>	$V_{CTRL}$ threshold for valley5 to valley6 forcing $@R_{CS}$$ = 330 $\Omega$	0.693	0.770	0.847	V			
V <sub>CTRL,th,65, 330</sub>	$V_{CTRL}$ threshold for valley6 to valley5 forcing $@R_{CS}$$ = 330 $\Omega$	0.846	0.940	1.034	V			
V <sub>CTRL,th,54, 330</sub>	$V_{CTRL}$ threshold for valley5 to valley4 forcing $@R_{CS}$$ = 330 $\Omega$	1.008	1.120	1.232	V			
V <sub>CTRL,th,43, 330</sub>	$V_{CTRL}$ threshold for valley4 to valley3 forcing $@R_{CS}$$ = 330 $\Omega$	1.170	1.300	1.430	V			
V <sub>CTRL,th,32, 330</sub>	$V_{CTRL}$ threshold for valley3 to valley2 forcing $@R_{CS}$$ = 330 $\Omega$	1.332	1.480	1.628	V			
V		•	-	-	•			

## Table 6. ELECTRICAL CHARACTERISTICS (Conditions: VCC = 18 V, $T_J = -40^{\circ}C$ to +125°C, unless otherwise specified) (Note 6)

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STOP

VREGUL DT SOFTOVP



#### DETAILED OPERATING DESCRIPTION

#### Introduction

NCL2801 is designed for working with LED Lighting applications coping with high ripple voltage on bulk capacitor and providing optimized line current THD and good efficiency. In addition, it incorporates protection features for robust operation. More generally, NCL2801 is ideal in systems where cost–effectiveness, reliability, low line current THD, low stand–by power and high efficiency are key requirements:

• Valley Count Frequency Fold–back: NCL2801 is designed to drive PFC boost stages in so–called Valley Count Frequency Fold–back (VCFF). In high load current condition, the circuit classically operates in *Cr*itical conduction *M*ode (*CrM*) also called 1<sup>st</sup> valley • Safety Protections: Permanently monitoring the input and output voltages, the MOSFET current and the die temperature to protect the system from possible over-stress makes the PFC stage extremely robust and



High Load Current One valley (CrM) Counting 1 valley Low Load Current More valleys (DCM) Counting 3 valleys

Lower Load Current More valleys (DCM)

Counting 6 valleys

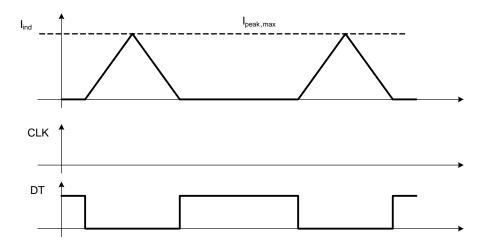


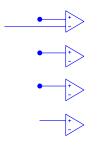
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VCTRL pin voltage level, starts adding a dead-time  $t_{DT}$ . The system adjusts the on-time  $t_{ON}$  (by means of peak current control) versus  $t_{DT}$  (see Figure 5) and consequently the

output power in order to ensure that the instantaneous mains current remains in phase with the mains instantaneous voltage (creating a unity PF).



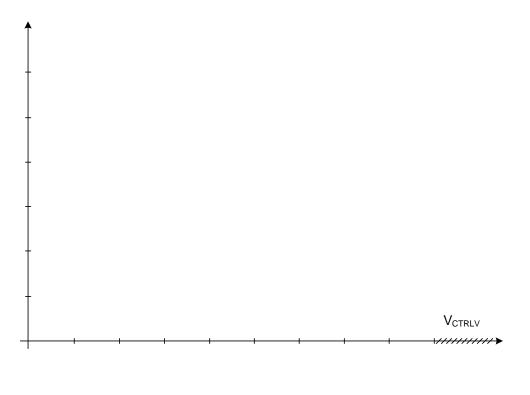




peak-to-peak ripple voltage stays under  $V_{\text{CTRL,hyst}}$  there will be no valley hopping.

 $V_{CTRL,hyst}$  can be calculated for each frequency foldback option determined by  $R_{CS}$  value from the thresholds specified in Table 7. While the hysteresis between two adjacent valley numbers is constant for one frequency foldback option, it decreases for options having a lower CrM to DCM  $V_{CTRL}$  threshold. This should not be a problem as the two times mains frequency ripple also decreases when VCTRL pin voltage decreases which results from output power decrease. We can also mention looking at Figure 7 and the specified frequency foldback thresholds of Table 7 that  $V_{CTRL,th,56}$  which is the  $V_{CTRL}$  threshold at which we force counting six valleys, has always the same value. This threshold is also called  $V_{CTRL,ADT}$  because when VCTRL pin voltage falls under this threshold, an analog dead-time starts to be added to the dead-time determined by counting six valleys. The lower VCTRL pin voltage goes under  $V_{CTRL,ADT}$  threshold, the more analog dead time is added. An example on how the analog dead time can be added is shown in the circuit of Figure 4 and the correspond power MOSFET drain voltage is shown in Figure 3.



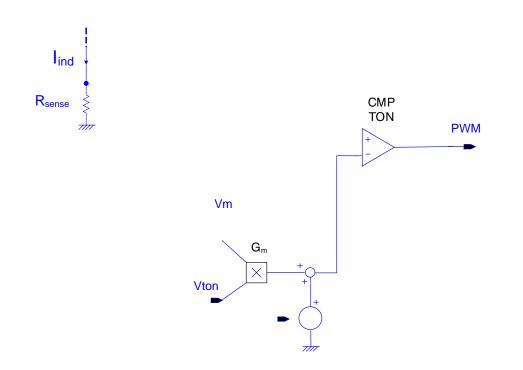


o Entering Forced Valley #

• Exiting Forced Valley #

# NCL2801 On time Modulation and $V_{\text{TON}}$ Processing Circuit

Let's analyze the ac line current absorbed by the PFC boost stage. The initial inductor current at the beginning of each switching cycle is always zero. The coil current ramps up when the MOSFET is *on*. The slope is  $(V_{in}/L)$  where *L* is the coil inductance. At the end of the on–time  $(t_I)$ , the inductor starts to demagnetize. The inductor current ramps down until it reaches zero. The duration of this phase is  $(t_2)$ . In some cases, the system enters then the dead–



level dependent multiplier gain values act as a two-level line feed forward.

#### NCL2801 Maximum on time

In order to avoid the on-time to go too high close to line voltage zero crossing, a  $V_{CTRL}$  dependent maximum on time circuitry has been added. The on-time limiting values are linearly depending on VCTRL pin voltage as follows:

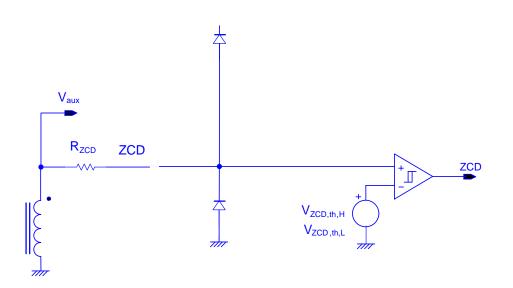
30  $\mu s ~@V_{CTRL}$  = 4.5 V and 5  $\mu s ~@V_{CTRL}$  = 0.55 V

#### NCL2801 Regulation Block and Output Voltage Control

A trans-conductance error amplifier (OTA) with access to its inverting input (FB pin) and to its output pin (VCTRL pin) is provided. It features a typical trans-conductance gain









soldering, an internal pull down current source pulls down the FB voltage under the UVP threshold and the controller is turned off.

- Detection the ZCD pin improper connection If the ZCD pin is floating or shorted to GND it is detected by internal circuitry and the circuit stops operating.
- Boost or bypass diode short

The controller addresses the short situations of the boost and bypass diodes (a bypass diode is generally placed between the input and output high–voltage rails to divert this inrush current). Practically, the overstress protection is implemented to detect such conditions and forces a low duty–cycle operation until the fault is gone.

Ordering Part No.	Soft OVP	Fast OVP (%)	V <sub>CC</sub> Start (V)	DRE (after start)	DRE (during start)	Brown Out	Line Range Detect	Package	Shipping <sup>†</sup>
NCL2801CDADR2G	Х	107	12.5	Х	Х	Х	Х	SOIC-8 (Pb-Free)	2500/Tape & Reel
NCL2801CDBDR2G	Х	107	12.5	Х	Х	Х		(PD-Fiee)	& Reel
NCL2801CFADR2G	Х	107	10.5	Х	Х	Х	Х		

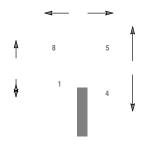
#### Table 8. NCL2801 ORDERING TABLE

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.





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