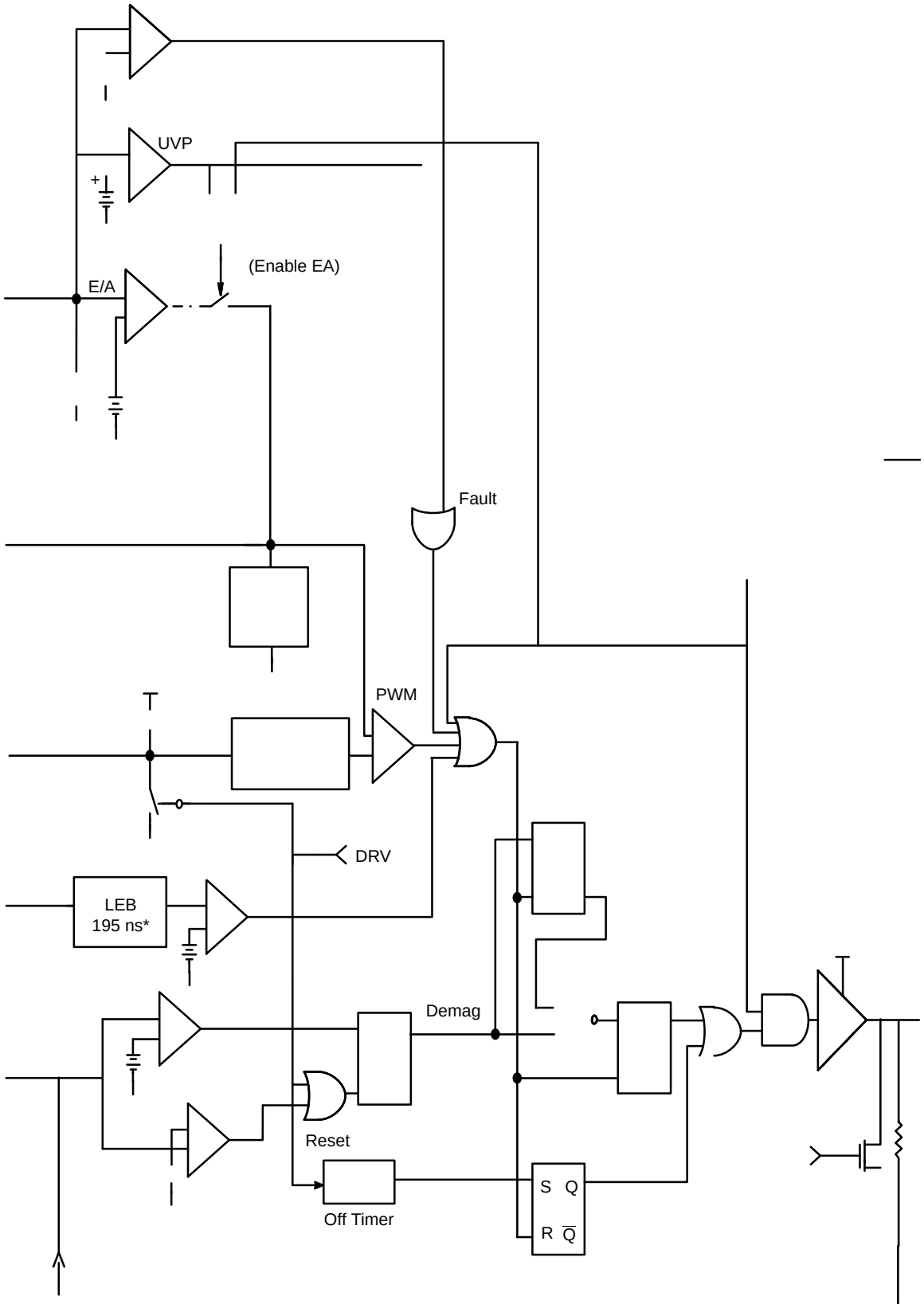
NCL30000

[illegible]d [illegible]

The NCL30000 is a switch mode power supply controller intended for low to medium power single stage power factor (PF) corrected LED Drivers. The device is designed to operate in critical conduction mode (CrM) and is suitable for flyback as well as buck topologies. Constant on time CrM operation is particularly suited for isolated flyback LED applications as the control scheme is straightforward and very high efficiency can be achieved even at low power levels. These are important in LED lighting to comply with regulatory requirements and meet overall system luminous efficacy requirements. In CrM, the switching frequency will vary with line and load and switching losses are low as recovery losses in the output rectifier are negligible since the current goes to zero prior to reactivating the main MOSFET switch.

The device features a programmable on time limiter, zero current detect sense block, gate driver, trans-conductance error amplifier as well as all PWM control circuitry and protection functions required to implement a CrM switch mode power supply. Moreover, for high efficiency, the device features low startup current enabling fast, low loss charging of the V_{CC} capacitor. The current sense protection threshold has been set at 500 mV to minimize power dissipation in the

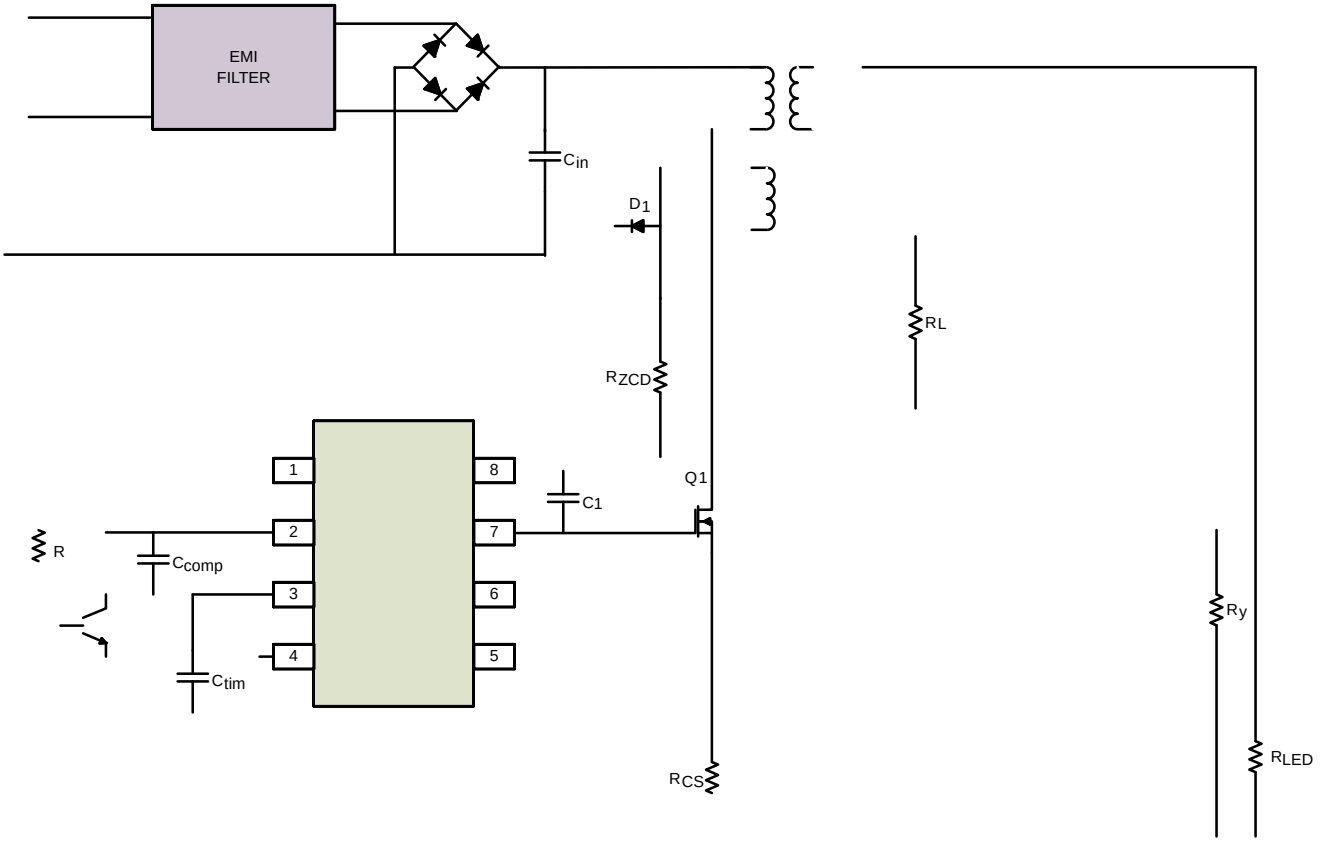


All SR Latches are Reset Dominant

Figure 1. Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Function
1	MFP	The multi-function pin is connected to the internal error amplifier. By pulling this pin below the V_{uvp} threshold, the controller is disabled. In addition, this pin also has an over voltage comparator which will disable the controller in the event of a fault.
2	COMP	The COMP pin is the output of the internal error amplifier. A compensation network is connected between this pin and ground to set the loop bandwidth. Normally this bandwidth is set at a low frequency (typically 10 Hz 20 Hz) to achieve high power factor and low total harmonic distortion (THD).
3	C_t	The C_t pin sources a regulated current to charge an external timing capacitor. The PWM circuit controls the power switch on time by comparing the C_t voltage to an internal voltage derived from $V_{Control}$. The C_T pin discharges the external timing capacitor at the end of the on time cycle.
4	CS	The CS input is used to sense the instantaneous switch current in the external MOSFET. This signal is filtered by an internal leading edge blanking circuit.
5	ZCD	The voltage of an auxiliary zero current detection winding is sensed at this pin. When the ZCD control block circuit detects that the winding has been demagnetized, a control signal is sent to the gate drive block to turn on the external MOSFET.
6	GND	This is the analog ground for the device. All bypassing components should be connected to the GND pin with a short trace length.
7	DRV	The high current capability of the totem pole gate drive (+0.5/ 0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs. The driver stage provides both passive and active pull down circuits that force the output to a voltage less than the turn-on threshold voltage of the power MOSFET when $V_{CC(on)}$ is not reached.
8	V_{CC}	This pin is the positive supply of the controller. The circuit starts to operate when V_{CC} exceeds $V_{CC(on)}$, nominally 12 V and turns off when V_{CC} goes below $V_{CC(off)}$, typically 9.5 V. After startup, the operating range is 10.2 V up to 20 V.



Overview

Figure 2 illustrates how the NCL30000 is configured to implement an isolated power factor corrected flyback switch mode power supply. On the secondary side is the NCS1002, a constant voltage, constant current controller which senses the average LED current and the output voltage and provides a feedback control signal to the primary side through an opto-coupler interface. One of the key benefits of active power factor correction is that it makes the load appear like a linear resistance similar to an incandescent bulb. High power factor requires generally sinusoidal line current and minimal phase displacement between the line current and voltage. The NCL30000 operates in a fixed on-time variable frequency mode where the power switch is on for the same length of time over a half cycle of input power. The current in the primary of the transformer starts at zero each switching cycle and is directly proportional to the applied voltage times the on-time. Therefore with a fixed on-time, the current will follow the applied voltage generating a current of the same shape. Just as in a traditional boost PFC circuit, the control bandwidth is low so that the on-time is constant throughout a single line cycle. The feedback signal from the secondary side is used to modify the average on-time so the current through the LEDs is properly regulated regardless of forward voltage variation of the LED string.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
MFP Voltage	V_{MFP}	0.3 to 10	V
MFP Current	I_{MFP}	10	mA
COMP Voltage	$V_{Control}$	0.3 to 6.5	V
COMP Current	$I_{Control}$	2 to 10	mA
Ct Voltage	V_{Ct}	0.3 to 6	V
Ct Current	I_{Ct}	10	mA
CS Voltage	V_{CS}	0.3 to 6	V
CS Current	I_{CS}	10	mA
ZCD Voltage	V_{ZCD}	0.3 to 10	V
ZCD Current	I_{ZCD}	10	mA
DRV Voltage	V_{DRV}	0.3 to V_{CC}	V
DRV Sink Current	$I_{DRV(sink)}$	800	mA
DRV Source Current	$I_{DRV(source)}$	500	mA
Supply Voltage	V_{CC}	0.3 to 20	V
Supply Current	I_{CC}	20	mA
Power Dissipation (T_A = 70 C, 2.0 Oz Cu, 55 mm^2 Printed Circuit Copper Clad)	P_D	450	mW
Thermal Resistance Junction-to-Ambient (2.0 Oz Cu, 55 mm^2 Printed Circuit Copper Clad)			

Table 3. ELECTRICAL CHARACTERISTICS
V_{MFP} = 2.4 V, $V_{Control}$ = 4 V, Ct = 1 nF, V_{CS} = 0 V, V_{ZCD} = 0 V, C_{DRV} = 1 nF, V_{CC} = 12 V, unless otherwise specified
(For typical values, T_J = 25 C. For min/max values, T_J = 40 C to 125 C, unless otherwise specified)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Startup Voltage Threshold	V_{CC} Increasing	$V_{CC(on)}$	11	12	12.5	V
Minimum Operating Voltage	V_{CC} Decreasing	$V_{CC(off)}$	8.8	9.5	10.2	V
Supply Voltage Hysteresis		H_{UVLO}	2.2	2.5	2.8	V
Startup Current Consumption	0 V < V_{CC} < $V_{CC(on)}$ 200 mV	$I_{cc(startup)}$		24	35	μA
No Load Switching Current Consumption	C_{DRV} = Open, 70 kHz Switching, V_{CS} = 2 V	I_{cc1}		1.4	1.7	mA
Switching Current Consumption	70 kHz Switching, V_{CS} = 2 V	I_{cc2}		2.1	2.6	mA
Fault Condition Current Consumption	No Switching, V_{MFP} = 0 V	$I_{cc(fault)}$		0.75	0.95	mA
OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
Overvoltage Detect Threshold	V_{MFP} = Increasing	V_{OVP}/V_{REF}	105	106	108	%
Overvoltage Hysteresis		$V_{OVP(HYS)}$	20	60	100	mV
Overvoltage Detect Threshold Propagation Delay	V_{MFP} = 2 V to 3 V ramp, C, 613.077 .68036 15.364 ref511 52-94(V)MFP					

Table 3. ELECTRICAL CHARACTERISTICS (Continued)
V_{MFP} = 2.4 V, $V_{Control}$ = 4 V, Ct = 1 nF, V_{CS} = 0 V, V_{ZCD} = 0 V, C_{DRV} = 1 nF, V_{CC} = 12 V, unless otherwise specified
(For typical values, T_J = 25 C. For min/max values, T_J = 40 C to 125 C, unless otherwise specified)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
RAMP CONTROL						
Ct Peak Voltage	V_{COMP} = open	$V_{Ct(MAX)}$	4.775	4.93	5.025	V
On Time Capacitor Charge Current	V_{COMP} = open V_{Ct} = 0 V to $V_{Ct(MAX)}$					

TYPICAL CHARACTERISTICS

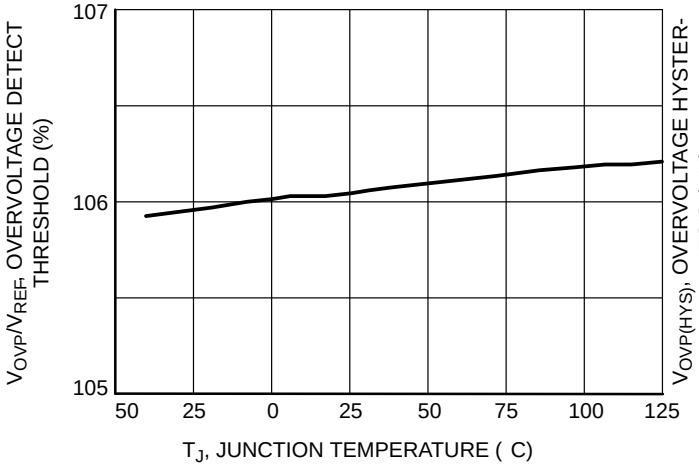


Figure 3. Overvoltage Detect Threshold vs. Junction Temperature

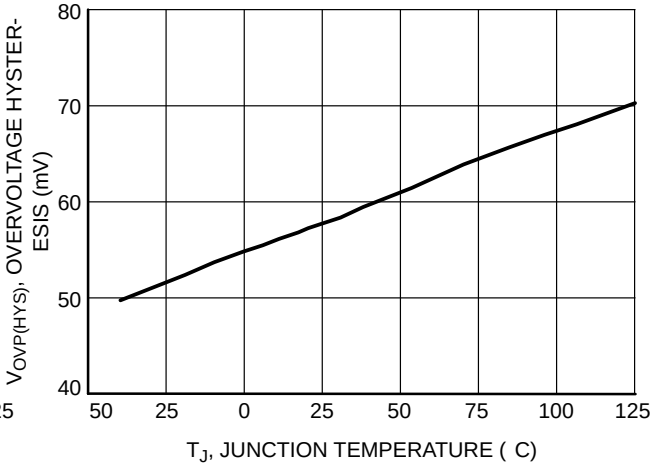


Figure 4. Overvoltage Hysteresis vs. Junction Temperature

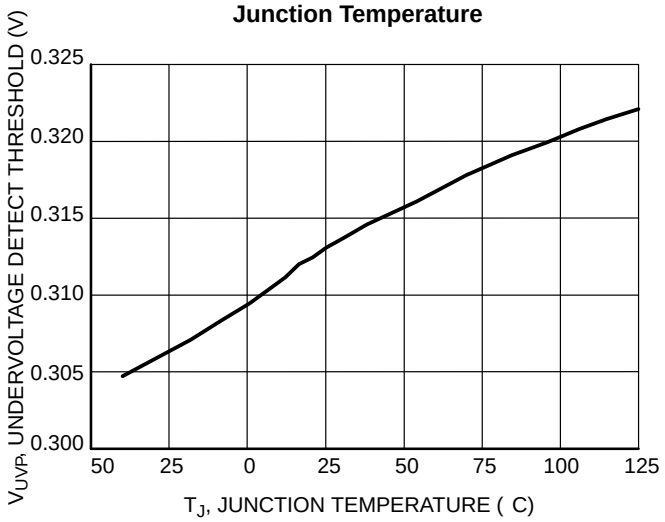


Figure 5. Undervoltage Detect Threshold vs. Junction Temperature

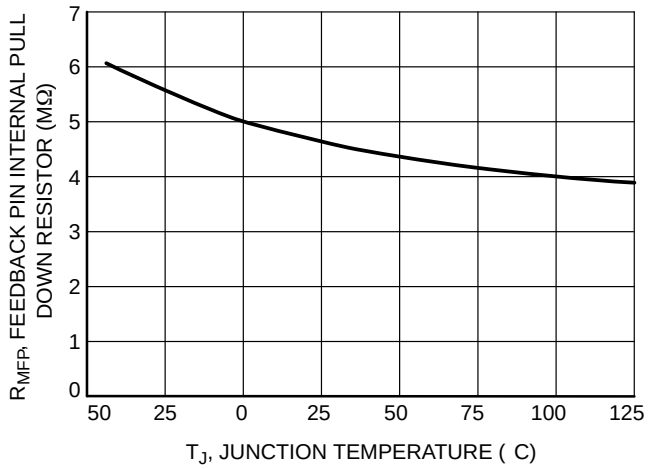


Figure 6. MFP Pin Internal Pull−Down Resistor vs. Junction Temperature

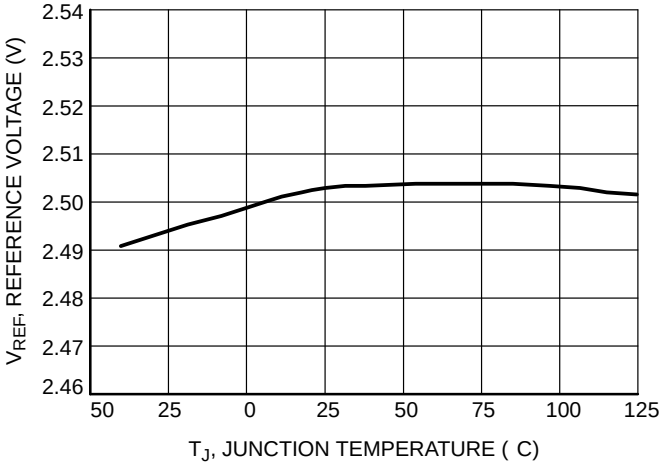


Figure 7. Reference Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS

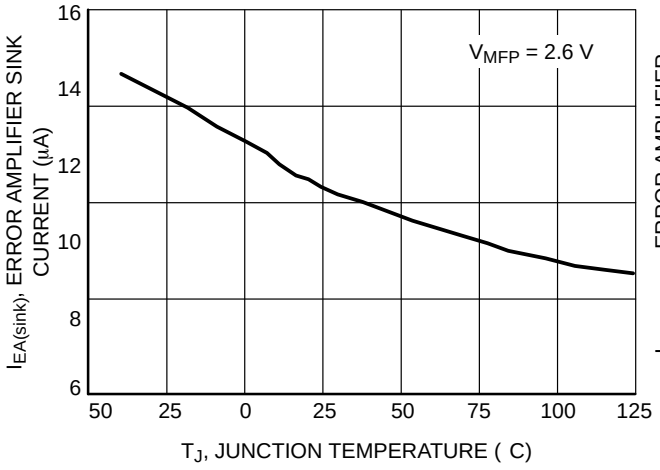


Figure 8. Error Amplifier Sink Current vs. Junction Temperature

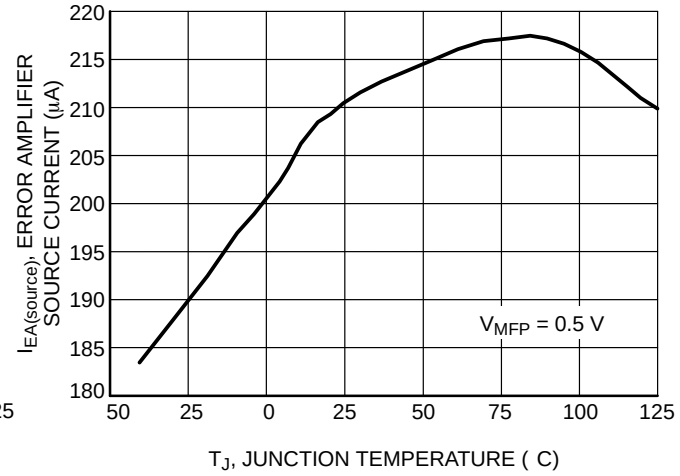


Figure 9. Error Amplifier Source Current vs. Junction Temperature

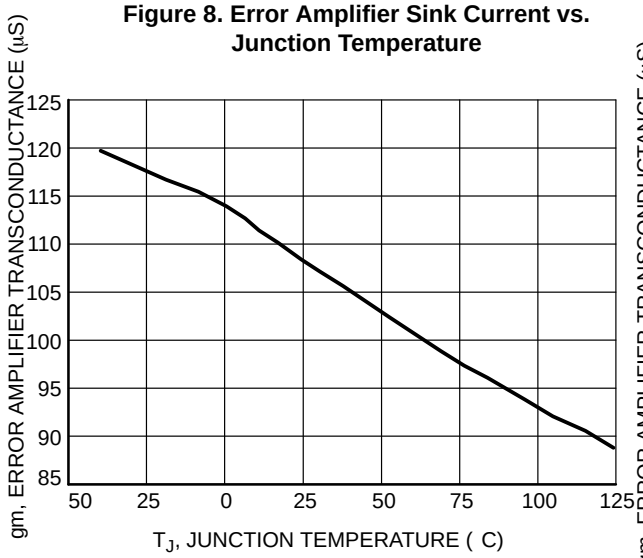


Figure 10. Error Amplifier Transconductance vs. Junction Temperature

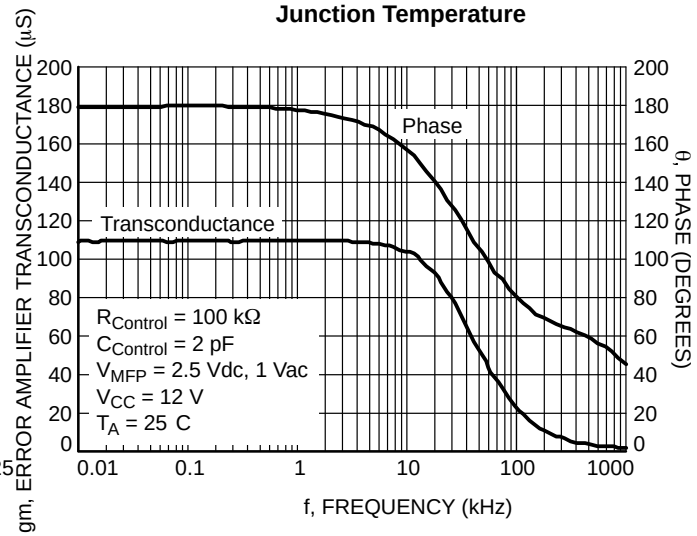


Figure 11. Error Amplifier Transconductance and Phase vs. Frequency

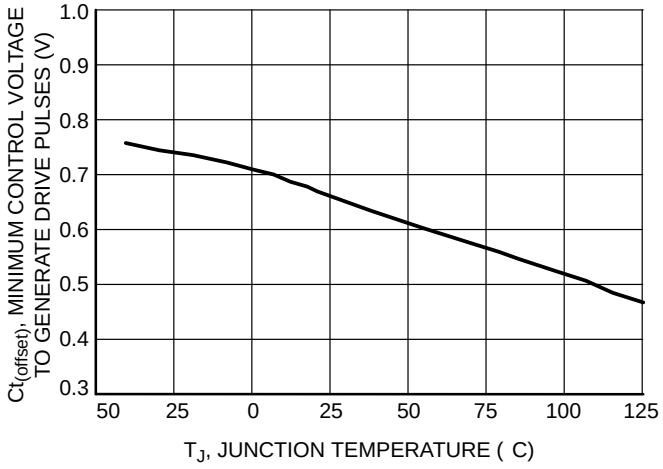


Figure 12. Minimum Control Voltage to Generate Drive Pulses vs. Junction Temperature

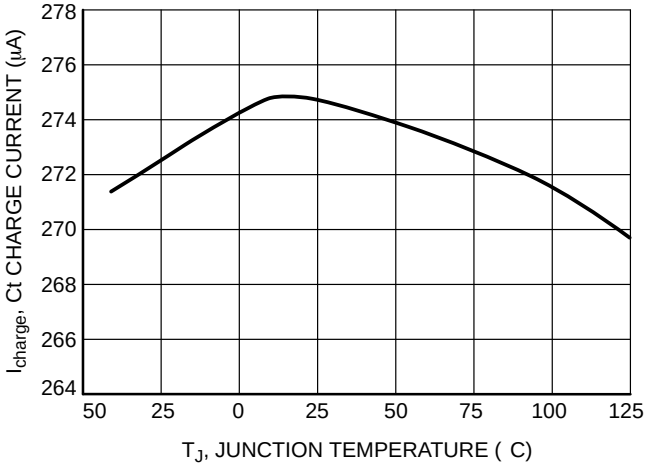


Figure 13. On Time Capacitor Charge Current vs. Junction Temperature

TYPICAL CHARACTERISTICS

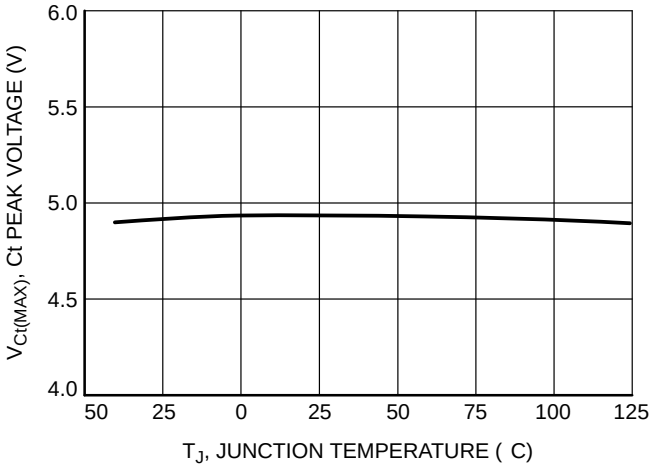


Figure 14. Ct Peak Voltage vs. Junction Temperature

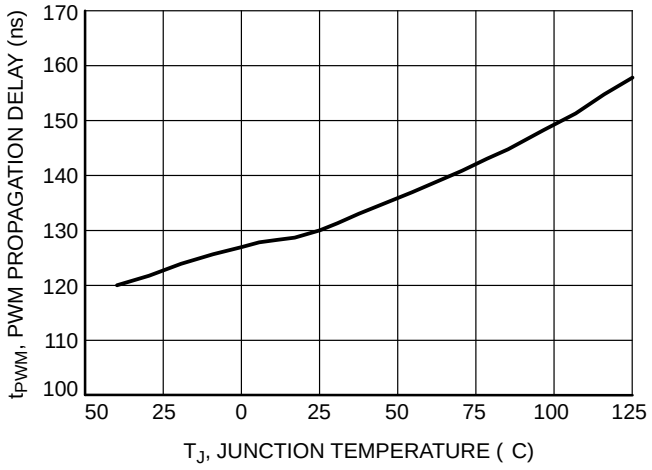


Figure 15. PWM Propagation Delay vs. Junction Temperature

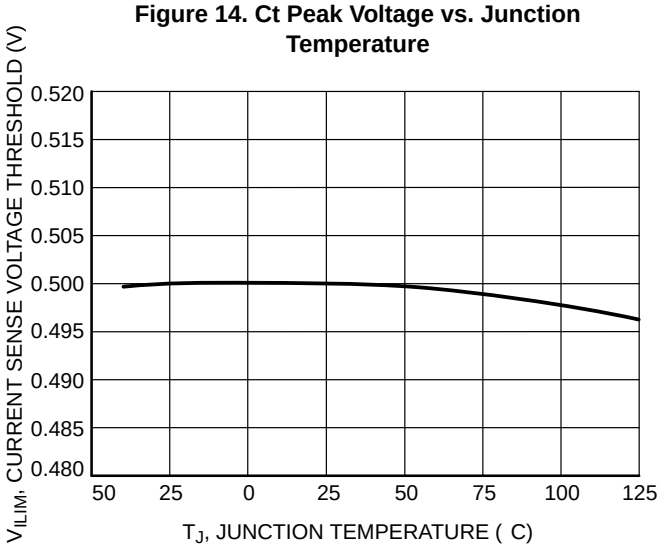


Figure 16. Current Sense Voltage Threshold vs. Junction Temperature

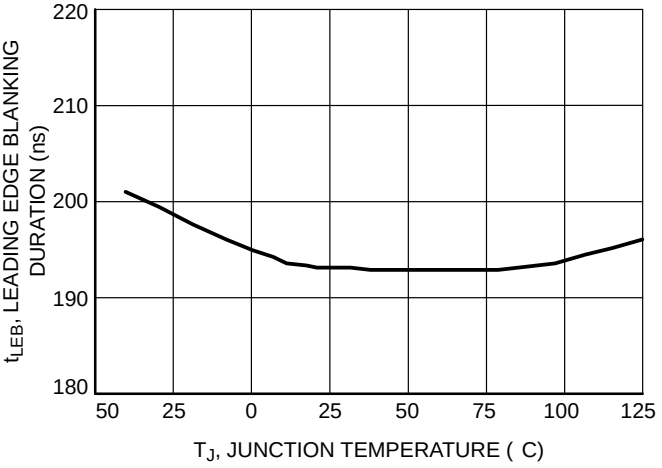


Figure 17. Leading Edge Blanking Duration vs. Junction Temperature

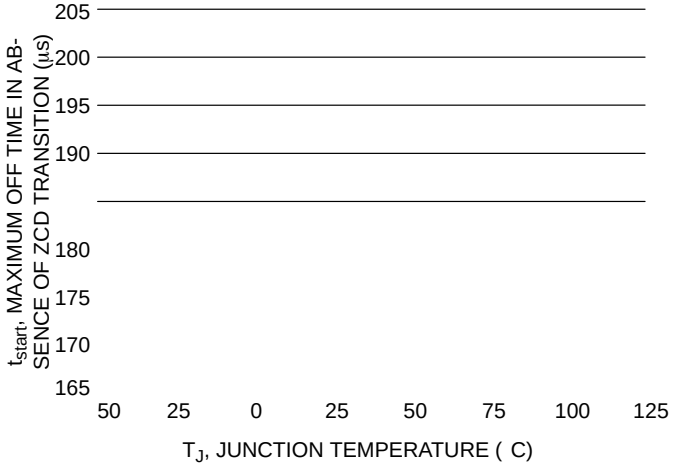


Figure 18. Maximum Off Time in Absence of ZCD Transition vs. Junction Temperature

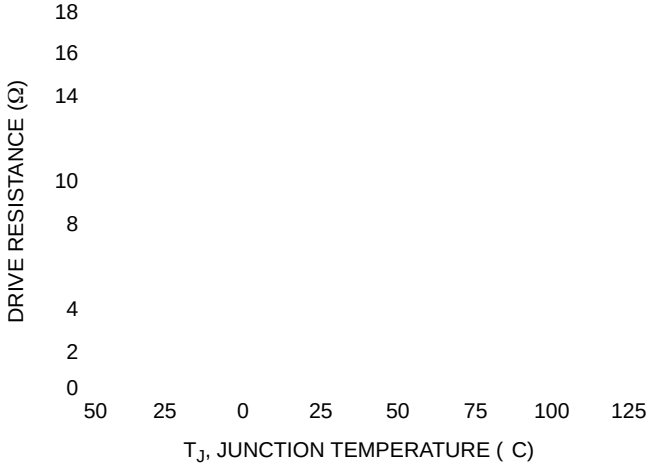


Figure 19. Drive Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS

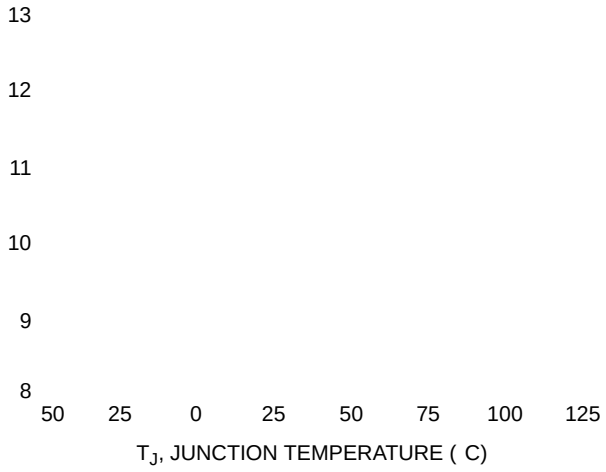


Figure 20. Supply Voltage Thresholds vs. Junction Temperature

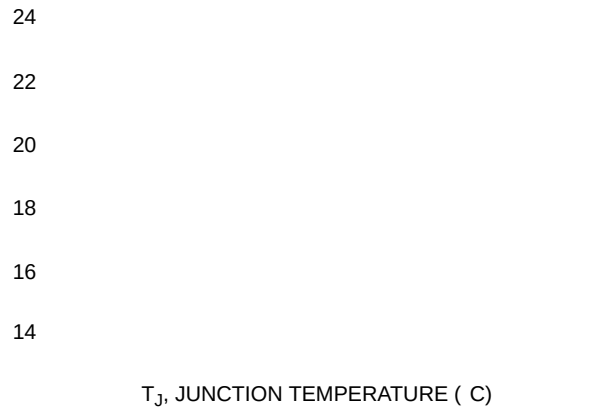
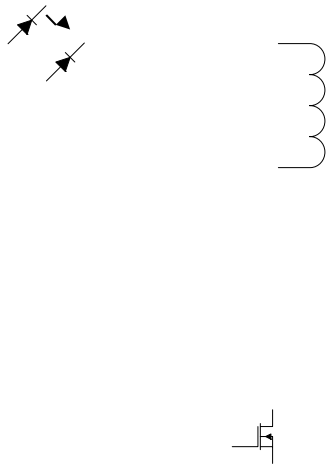


Figure 21. Startup Current Consumption vs. Junction Temperature

THEORY OF OPERATION

High power factor requires generally sinusoidal line current and minimal phase displacement between the line current and voltage. Normally this is not the case with a traditional isolated flyback topology so the first step to achieve high power factor is to have minimal capacitance before the switching stage to allow a more sinusoidal input current. A simplified block diagram is illustrated in Figure 23. Since the input bulk capacitor has virtually been eliminated except for a small capacitor, the voltage to the flyback converter now follows a rectified sine shape at twice the line frequency. By employing a critical conduction mode control technique such that the input current is kept to the same shape, high power factor can be achieved. The NCL30000 is a voltage mode, fixed on-time controller specifically intended for such applications.



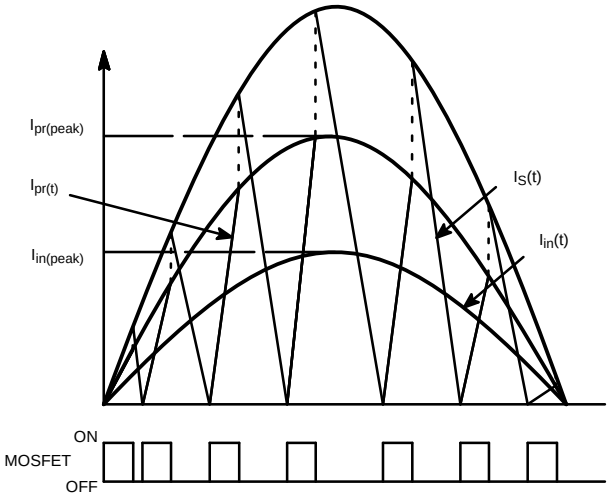


Figure 24. Theoretical Switching Waveform

The LED current is compared to a reference and an error signal is passed to the NCL30000 controller to maintain the desired average level. This error signal adjusts the on-time of the power switch to pass the required energy through the flyback transformer to achieve proper regulation of the LED load. Just like in a traditional PFC boost converter, the loop bandwidth must be low enough to filter out the twice line frequency ripple otherwise the power factor correction element of the circuit will be compromised. In the event of

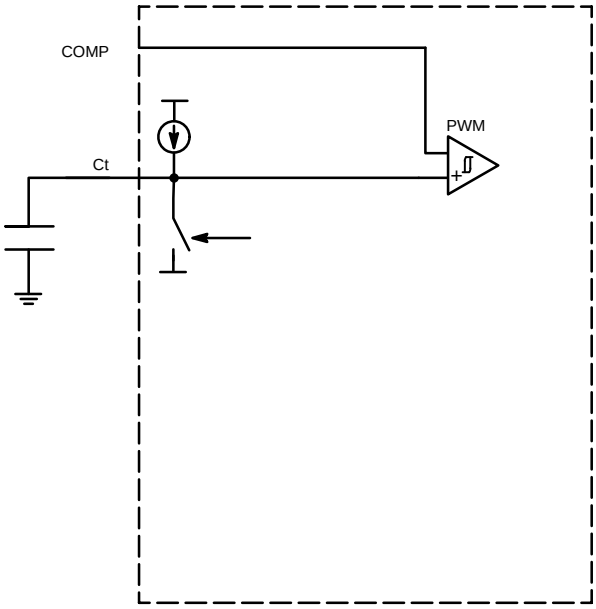


Figure 25. On Time Control

ZCD Detection Block

A dedicated circuit block is necessary to implement the zero current detection**.** The NCL30000 provides a separate input pin to signal the controller to turn the power switch back on just after the flyback transformer discharges all the stored energy to the secondary winding. When the output winding current reaches zero the winding voltage will reverse. Since all windings of the transformer reflect the same voltage characteristic this voltage reversal appears on the primary bias winding. Coupling the winding voltage to the ZCD input of the NCL30000 allows the controller to start the next switching cycle at the precise time. To avoid inadvertent false triggering, the ZCD input has a dual comparator input structure to arm the latch when the ZCD detect voltage rises above 1.4 V (nominal) thus setting the latch. When the voltage on ZCD falls below 0.7 V (nominal) a zero current event is detected and a signal is asserted which initiates the next switching cycle. This is illustrated in Figure 27. The input of the ZCD has an internal circuit which clamps the positive and negative voltage excursions on this pin. The current into or out of the ZCD pin must be limited to 10 mA with an external resistor.

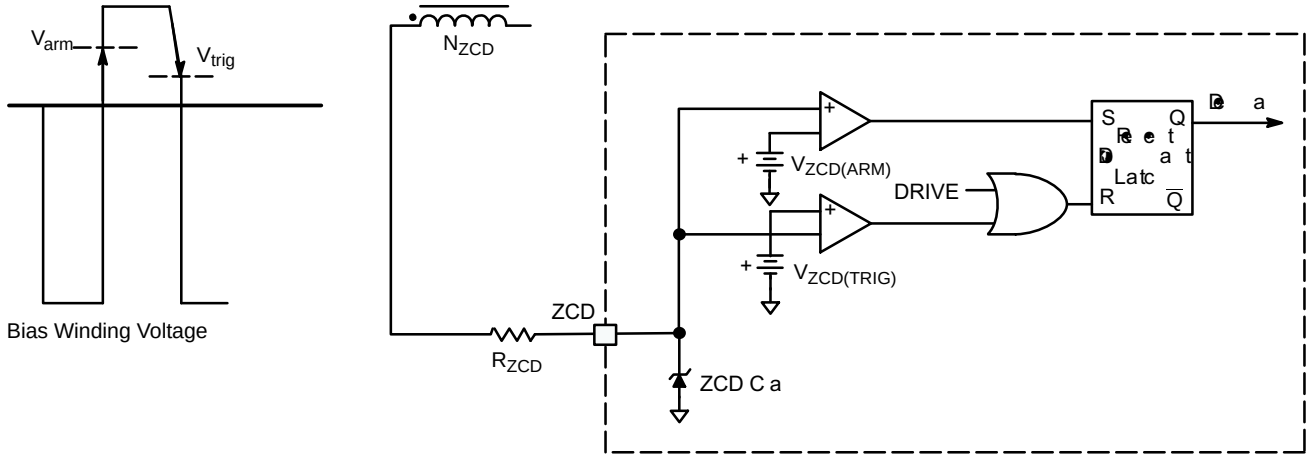


Figure 27. ZCD Operation

At startup, there is no energy in the ZCD winding and no voltage signal to activate the ZCD comparators. To enable the controller to start under these conditions, an internal watchdog timer is provided which initiates a switching cycle in the event that the output drive has been off for more than 180 μs (nominal).

The timer is deactivated only under an OVP or UVP fault condition which will be discussed in the next section.

Overcurrent Protection (OCP)

The dedicated CS pin of the NCL30000 senses the current through the MOSFET switch and the primary side of the transformer. This provides an additional level of protection in the event of a fault. If the voltage of the CS pin exceeds V_{ILIM}, the internal comparator will detect the event and turn off the MOSFET. The peak switch current is calculated using Equation 1:

$$I_{SW(peak)} = \frac{V_{ILIM}}{R_{sense}} \qquad \text{(eq. 1)}$$

To avoid the possibility of false switching, the

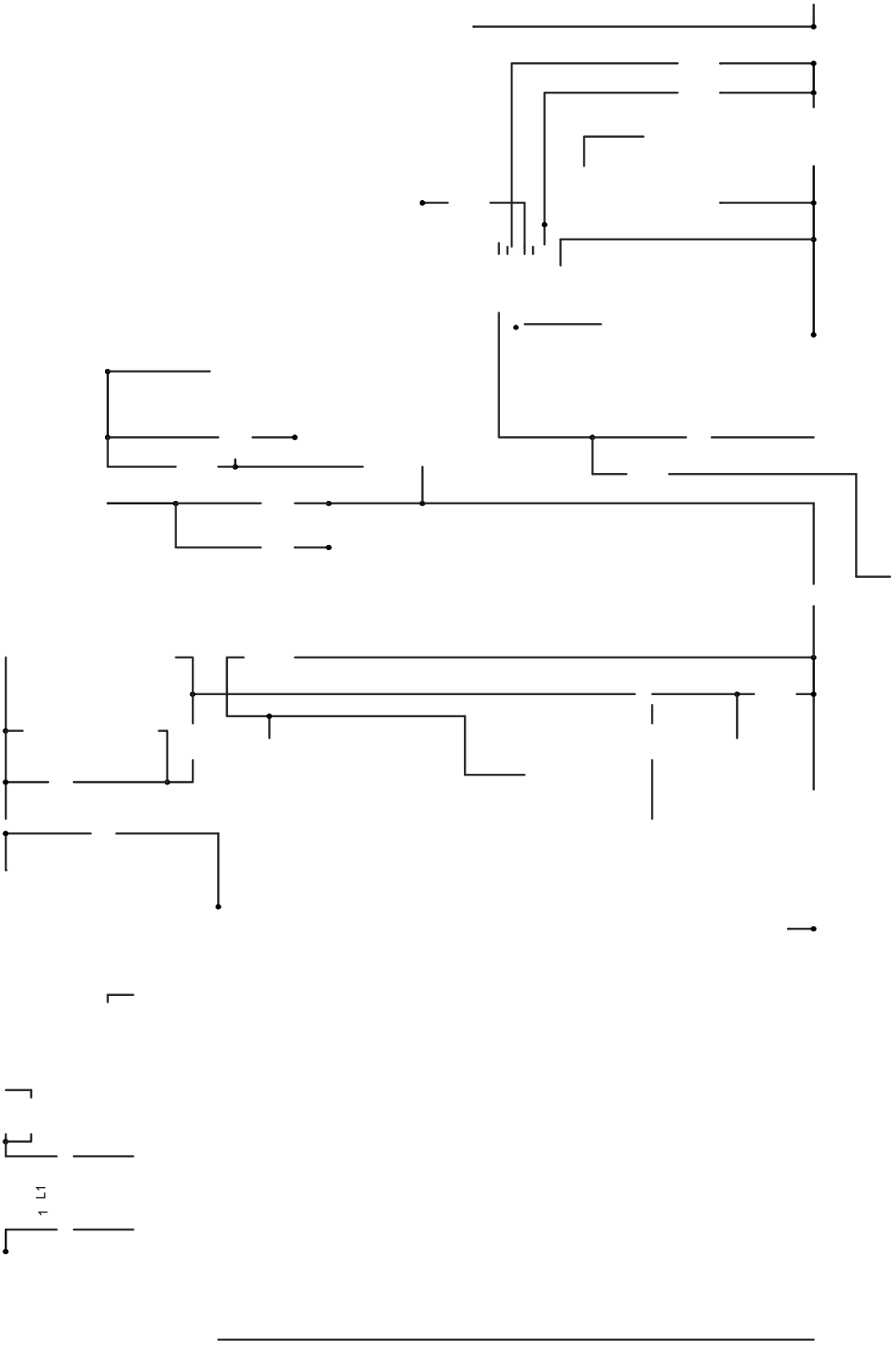


Figure 30. Wide Input Main, 4−15 LED 350 mA Load Schematic

Zero Current Detection (ZCD)

The signal controlling the ZCD function is taken from the primary bias winding. Raising the ZCD pin above 1.4 V arms the zero detection circuit. When the pin voltage subsequently falls below 0.7 V, the controller issues the command to turn the power switch back on. The current in or out of the ZCD pin must be limited to 10 mA by an external resistor. For this reference circuit a resistance of 47 kΩ provides the required voltage thresholds and limits current to less than 10 mA.

Feedback Control

The secondary feedback signal is routed through an optocoupler to the primary side NCL30000 controller. LED current is measured with a 0.2 Ω resistor which for 350 mA has a voltage drop of 70 mV.

The control loop must be designed to filter out the rectified sine wave ripple component to provide an average feedback level to the pulse width controller. In order to maintain high power factor operation, the compensation components around the error amplifier must be set well below 50/60 Hz. The corner frequency typically falls between 10 and 40 Hz. The low frequency response means the control loop will be slow to compensate for rapidly changing situations. In particular, the slow response can introduce overshoot at turn on.

To compensate for the slow steady state loop this circuit utilizes a second current control loop to minimize overshoot. The second loop is set for higher than nominal operating current with a very fast response loop. This error amp takes control of the feedback loop until the main error amp is able to respond. In this way the maximum current is limited to safe established level.

The current set point of the fast control loop should be set above the peak of the ripple current of normal operation. U4 is a 2.5 V reference which in conjunction with

insulated wire is selected for compliance with safety agency isolation requirements.

The primary bias winding must supply 10.2 V to maintain NCL30000 operation. The minimum secondary voltage is 12 V and with 24 turns this means the bias winding needs 20.4 turns. Select 22 turns to meet the minimum.

For maximum primary to secondary coupling, the primary winding will be split in two equal sections with the secondary winding placed in between. The bias winding is wound on top of the second half of the primary winding.

FET Switch

The NCL30000 controller drives an external power FET controlling the current in the flyback transformer primary. The demonstration board was designed to accept the surface mount DPAK or through-hole TOǐ220 power packages. The 17.5 W target application in 50 C ambient works well with a DPAK package. The 800 V 2 A rated SPD02N80C3 was chosen.

Maximum primary current was calculated as 1.11 A. The NCL30000 has a 0.5 V over-current protection threshold. To allow for 25% margin, a minimum sense resistor of 0.348 Ω is required. A standard 0.33 Ω resistor will be selected. The current sense resistor is placed in the source lead of the power FET and coupled to the controller with a 100 Ω resistor. This resistance in conjunction with the inherent capacitance of the pin filters high frequency noise. In addition, a

Load

Figure 35 shows output ripple current for 115 Vac input and 36.9 (12 LED) load operating at 350 mA average. Scale factor is 67 mA per division. The low frequency ripple follows the input twice line frequency rectified sine wave characteristic of single stage converters.

Figure 35. Output Ripple at 115 Vac and 36.9 V, 350 mA Load

Figure 36 shows output ripple current at the main switching frequency. Scale factor is 33 mA per division. This is the signal superimposed over the rectified sine wave ripple component.

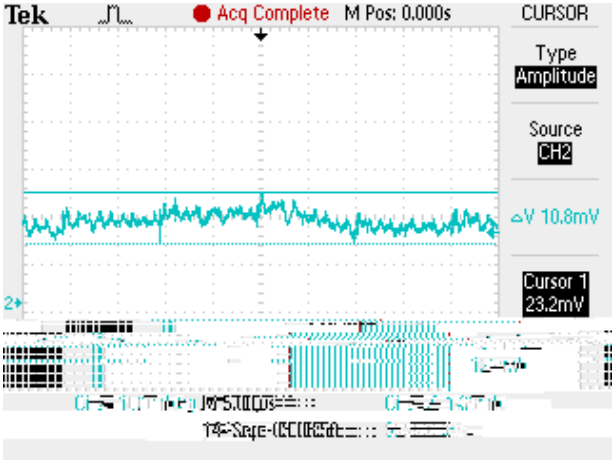


Figure 36. Output Ripple at 115 Vac and 36.9 V, 350 mA Load

Initial start up characteristic is shown in Figure 37 below. Note the higher current limit controlled by the fast feedback loop and the transition to the main average mode feedback control loop. This shows start up at 115 Vac with 36.9 V, 350 mA load. Trace 2 is LED current at 167 mA per division and trace 3 is applied input voltage at 200 V per division.

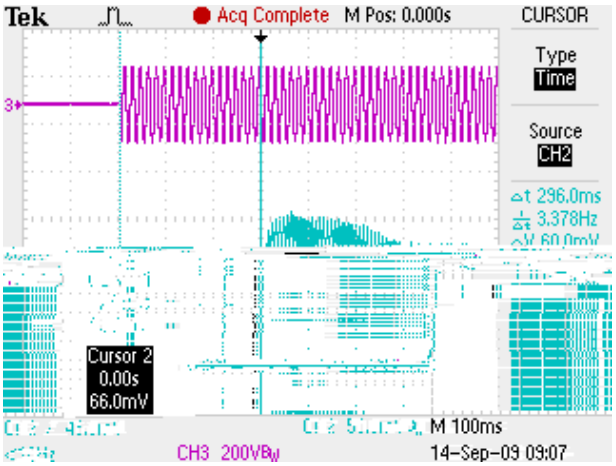


Figure 37. Start up Characteristic with 36.9 V, 350 mA Load

Typical voltage stress on power FET with 36.9 V, 350 mA load and 305 Vac input voltage is shown in Figure 38. Scale factor is 100 V per division.

Figure 38. Drain to Source Voltage with 36.9 V, 350 mA Load at 305 Vac Input

Note that while the power supply was designed to meet agency requirements, it has not been submitted for compliance. Standard safety practices should be used when this circuit is energized and in particular when connecting test equipment. During evaluation, input power should be sourced through an isolation transformer.

Additional Application Information and Tools

An evaluation board is available for this 90 ĭ 305 Vac design example. Moreover, for applications where it is desired to dim the LEDs via a TRIAC dimmer, please refer to Application Note AND8448 which explains the steps necessary to configure the NCL30000 for TRIAC dimming. In addition there are two additional TRIAC dimmable reference designs which illustrate a complete design for 90 ĭ 135 Vac or 180 ĭ 265 Vac operation. There is also an Microsoft EXCEL spreadsheet tool available to aid in the design process and assist in developing target winding requirements for the transformer.

SOIC−8 NB