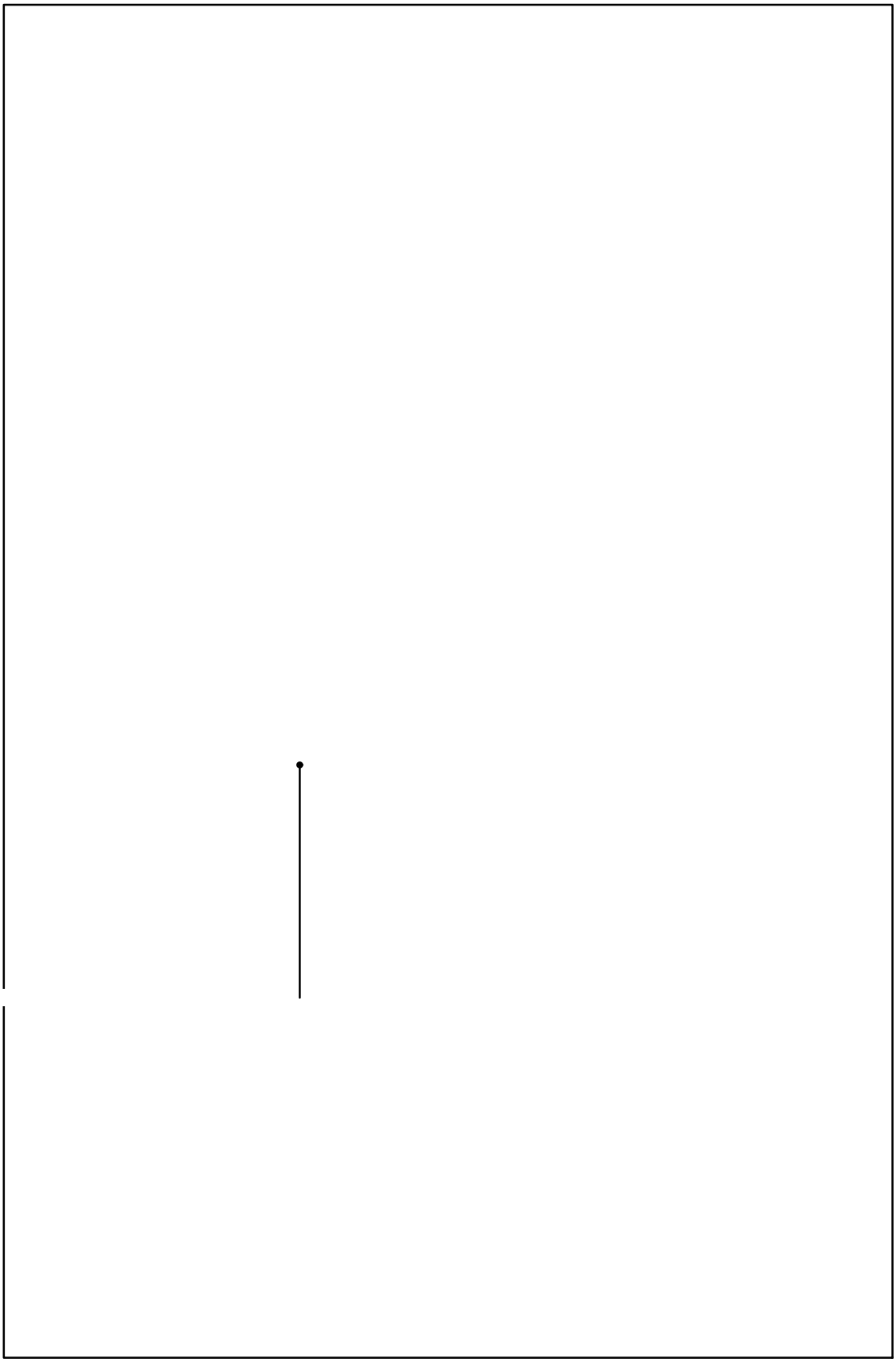


**PIN FUNCTION DESCRIPTION**

| Pin | Symbol | Description |
|---|---|---|
| 1 | $C_T$ | An external timing capacitor ($C_T$) sets the oscillator frequency. A sawtooth between 0.2 V and 4 V sets the oscillator frequency and the gain of the multiplier. |
| 2 | RAMP COMP | A resistor ($R_{RC}$) between this pin and ground adjust the amount of ramp compensation that is added to the current signal. Ramp compensation is required to prevent subharmonic oscillations. This pin should not be left open. |
| 3 | AC IN | The scaled version of the full wave rectified input ac wave is connected to this pin by means of a resistive voltage divider. The line voltage information is used by the multiplier. |
| 4 | FB | An error signal from an external error amplifier circuit is fed to this pin via an optocoupler or other isolation circuit. The FB voltage is a proportional of the load of the converter. If the voltage on the FB pin drops below 0.41 V (typical) the controller enters Soft−Skip to reduce acoustic noise. |
| 5 | VFF | |

**MAXIMUM RATINGS** (Notes 1 and 2)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Start_up Input Voltage<br>Start_up Input Current | $V_{HV}$<br>$I_{HV}$ | −0.3 to 500<br>±100 | V<br>mA |
| Power Supply Input Voltage<br>Power Supply Input Current | $V_{CC}$<br>$I_{CC}$ | −0.3 to 20<br>±100 | V<br>mA |
| Latch Input Voltage<br>Latch Input Current | $V_{Latch}$<br>$I_{Latch}$ | −0.3 to 10<br>±100 | V<br>mA |

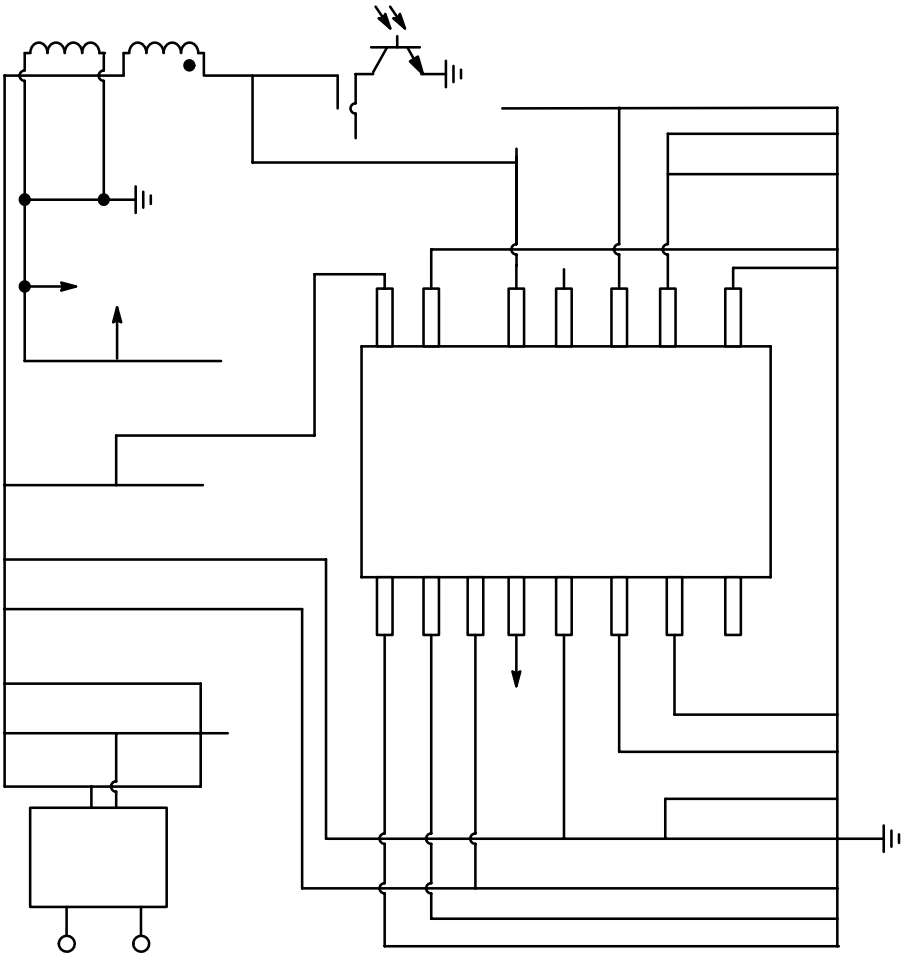


**Figure 2. Typical Application Schematic**

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 15 V, $V_{AC\ IN}$ = 3.8 V, $V_{FB}$ = 2.0 V, $V_{FF}$ = 2.4 V, $V_{Latch}$ = open, $V_{ISPOS}$ = −100 mV, $C_{DRV}$ = 1 nF, $C_T$ = 470 pF, $C_{IAVG}$ = 0.27 nF, $C_{Latch}$ = 0.1 nF, $C_M$ = 10 nF, $R_{IAVG}$ = 76.8 kΩ, $R_{TEST}$ = 50 kΩ, $R_{RC}$ = 43 kΩ, For typical Value $T_J$ = 25 C, for min/max values $T_J$ = −40 C to 125 C, unless otherwise noted)

| Parameter | Test Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | | |
| Frequency | | $f_{osc}$ | 90 | 100 | 110 | kHz |
| Frequency Modulation in Percentage of $f_{OSC}$ | | | – | 6.8 | – | % |
| Frequency Modulation Period | | | – | 6.8 | – | ms |
| Ramp Peak Voltage | | $V_{CT(peak)}$ | – | 4.0 | – | V |
| Ramp Valley Voltage | | $V_{CT(valley)}$ | – | 0.10 | – | V |
| Maximum Duty Ratio | $R_{TEST}$ = open | D | 94 | – | – | % |
| Ramp Compensation Peak Voltage | | $V_{RCOMP(peak)}$ | – | 4 | – | V |
| **AC ERROR AMPLIFIER** | | | | | | |
| Input Offset Voltage (Note 3) | Ramp $I_{AVG}$, $V_{FB}$ = 0 V | $ACV_{IO}$ | | 40 | – | mV |
| Error Amplifier Transconductance | | $g_m$ | – | 100 | – | μS |
| Source Current | $V_{AC\ COMP}$ = 2.0 V, $V_{AC\ IN}$ = 2.0 V, $V_{FF}$ = 1.0 V | $I_{EA(source)}$ | 25 | 70 | – | μA |
| Sink Current | $V_{AC\ COMP}$ = 2.0 V, $V_{A\ C\_IN}$ = 2.0 V, $V_{FF}$ = 5.0 V | $I_{EA(sink)}$ | −25 | −70 | – | μA |
| **CURRENT AMPLIFIER** | | | | | | |
| Input Bias Current | $V_{ISPOS}$ = 0 V | $CAI_{bias}$ | 40 | 53 | 80 | μA |
| Input Offset Voltage | $V_{AC\ COMP}$ = 5.0 V, $V_{ISpos}$ = 0 V | $CAV_{IO}$ | −20 | 0 | 20 | mV |

Current Limit.mcJreshol

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 15 V, $V_{AC\ IN}$ = 3.8 V, $V_{FB}$ = 2.0 V, $V_{FF}$ = 2.4 V, $V_{Latch}$ = open, $V_{ISPOS}$ = −100 mV, $C_{DRV}$ = 1 nF, $C_T$ = 470 pF, $C_{IAVG}$ = 0.27 nF, $C_{Latch}$ = 0.1 nF, $C_M$ = 10 nF, $R_{IAVG}$ = 76.8 kΩ, $R_{TEST}$ = 50 kΩ, $R_{RC}$ = 43 kΩ, For typical Value $T_J$ = 25 C, for min/max values $T_J$ = −40 C to 125

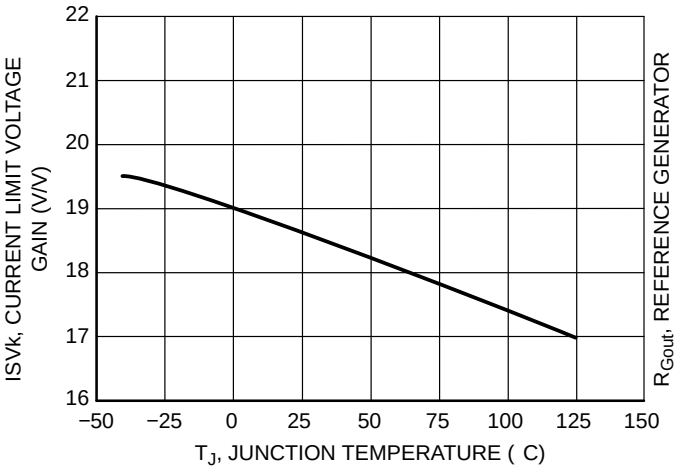



**Figure 14. Oscillator CS Limit Voltage Gain vs. Junction Temperature**

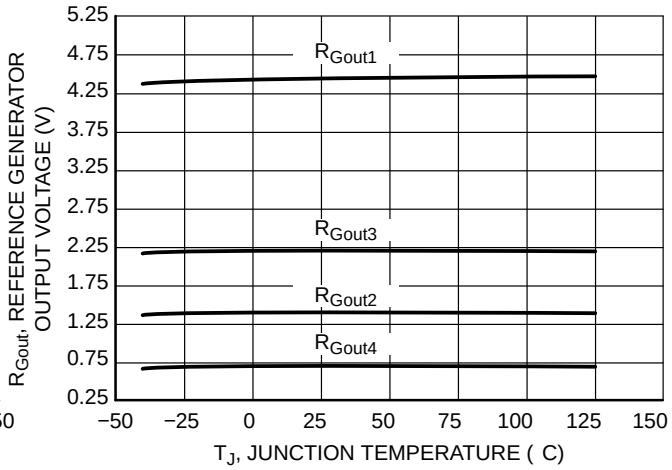
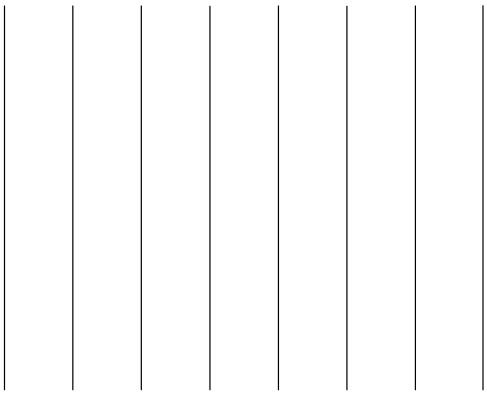



**Figure 15. Oscillator Reference Generator Output Voltage vs. Junction Temperature**



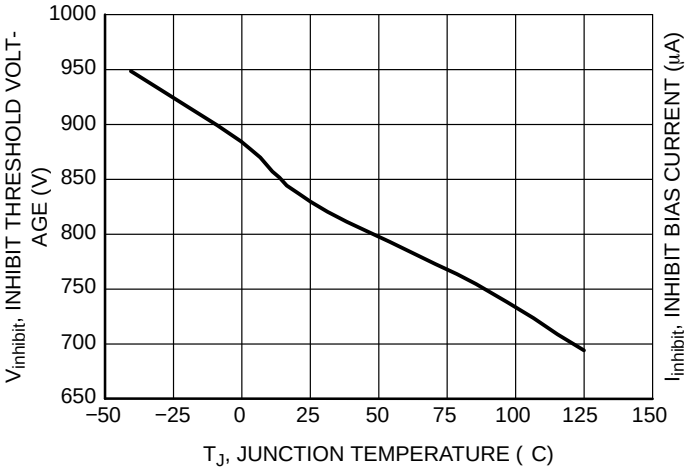



**Figure 26. Inhibit Threshold Voltage vs. Junction Temperature**

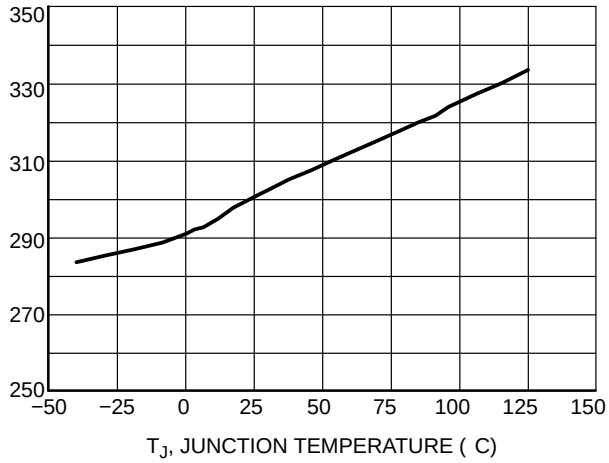
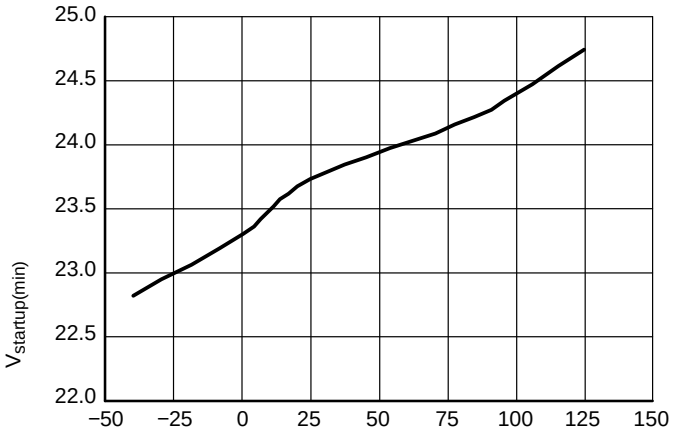



**Figure 27. Inhibit Bias Current vs. Junction Temperature**



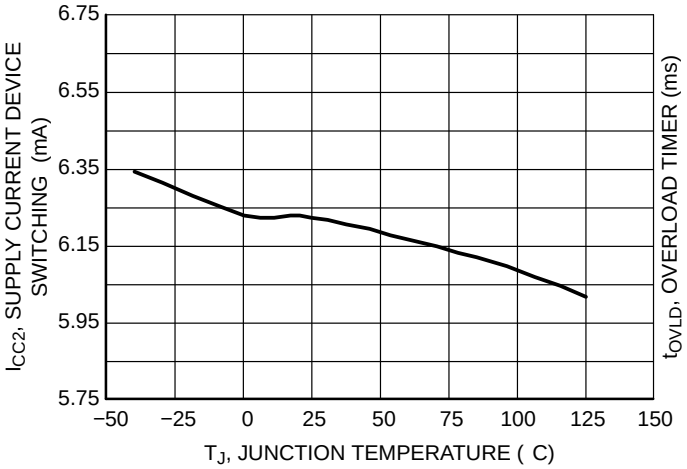



**Figure 32. Supply Current Device Switching vs. Junction Temperature**

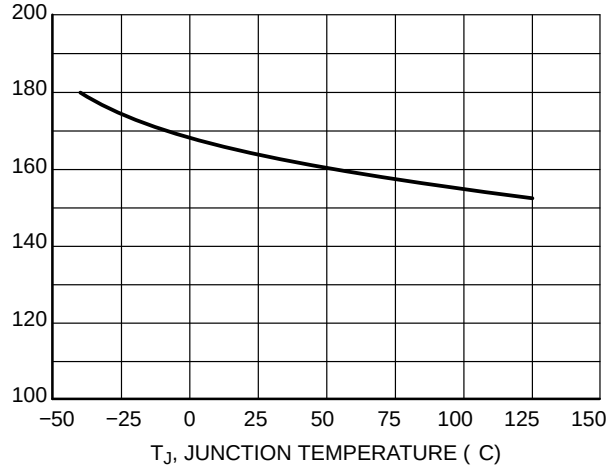



**Figure 33. Overload Timer vs. Junction Temperature**

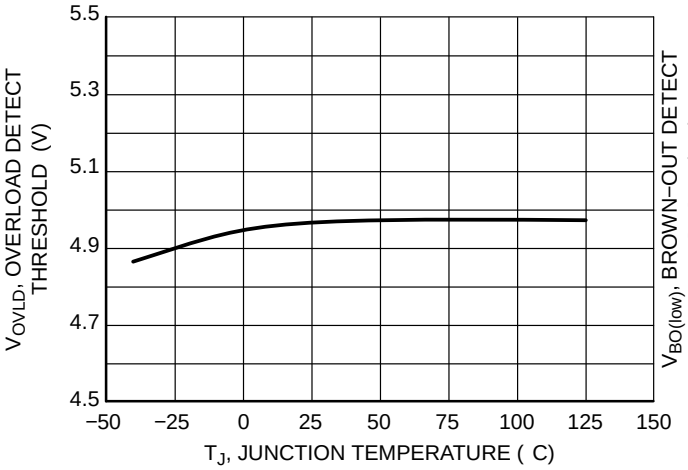



**Figure 34. Overload Detect Threshold vs. Junction Temperature**

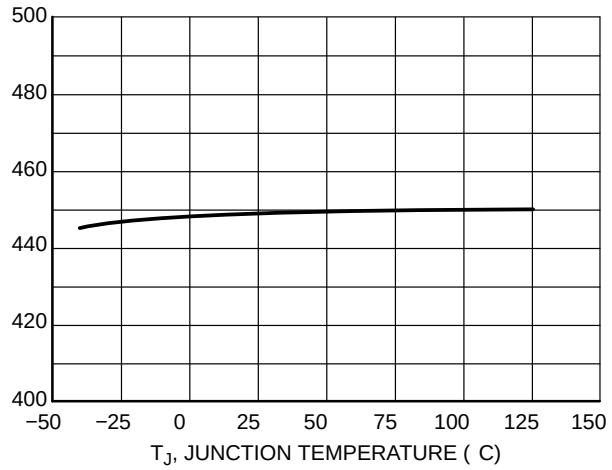



**Figure 35. Brown−Out Detect Threshold vs. Junction Temperature**

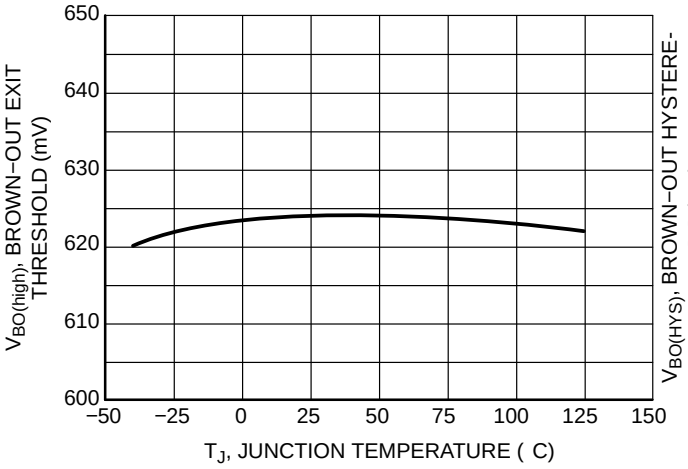



**Figure 36. Brown−Out Exit Threshold vs. Junction Temperature**

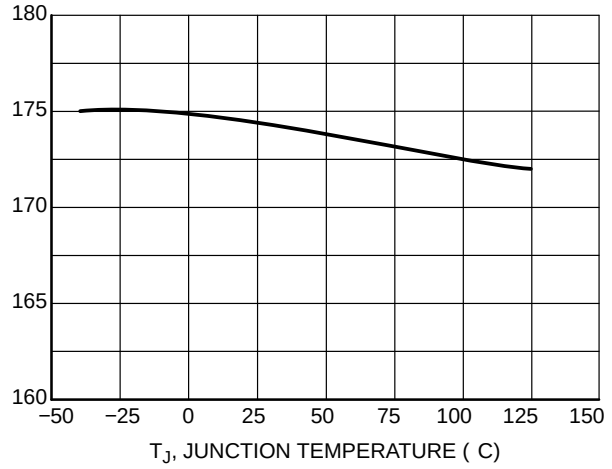



**Figure 37. Brown−Out Hysteresis vs. Junction Temperature**

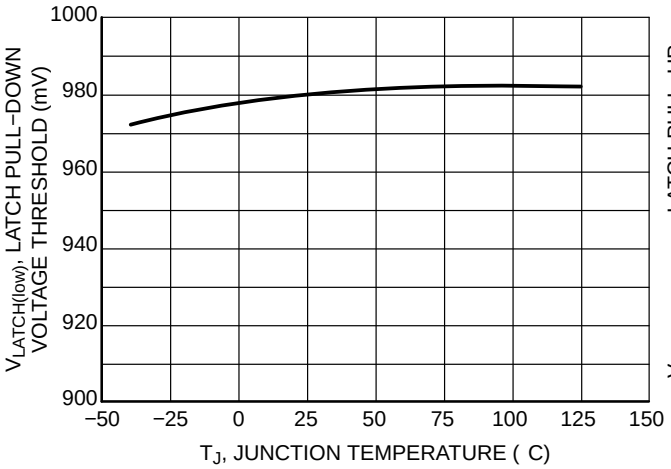



**Figure 38. Latch Pull−Down Voltage Threshold vs. Junction Temperature**

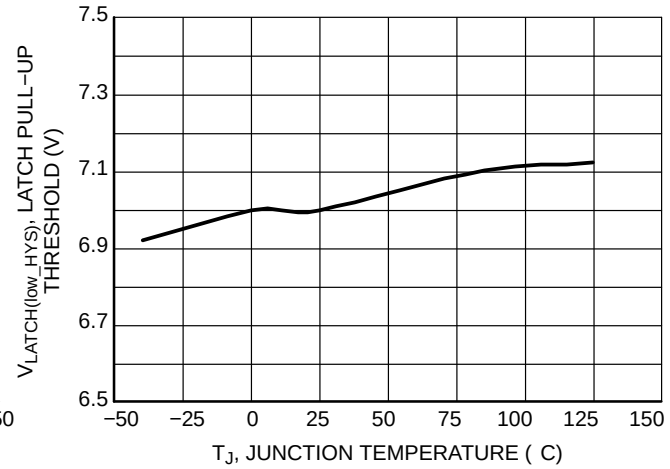



**Figure 39. Latch Pull−Up Threshold vs. Junction Temperature**

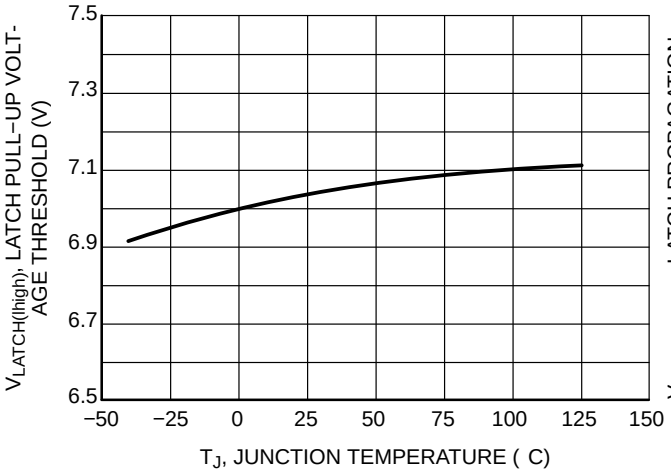



**Figure 40. Latch Pull−Up Voltage Threshold vs. Junction Temperature**

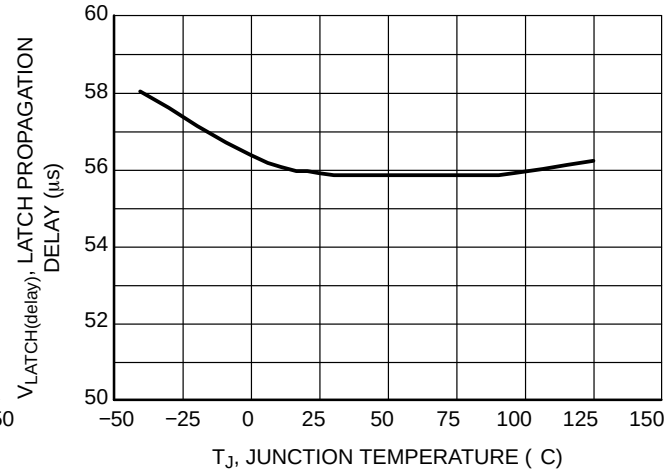



**Figure 41. Latch Propagation Delay vs. Junction Temperature**

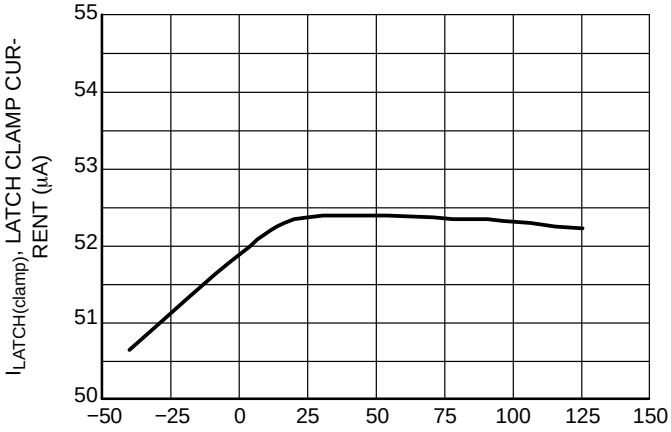



**Figure 42. Latch Clamp Current vs. Junction Temperature**

## DETAILED DEVICE DESCRIPTION

### Introduction

rating compared to similar dc−input flyback applications.

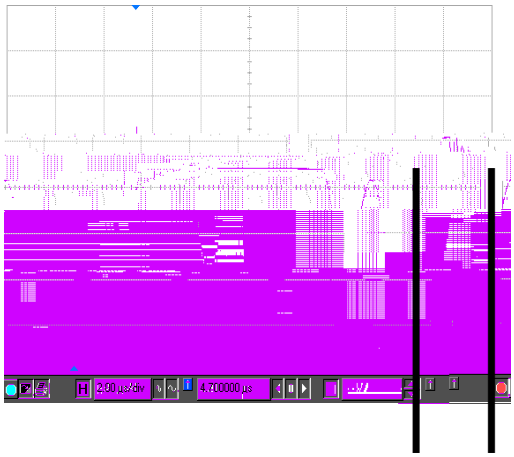


**Figure 47. Typical Drain Voltage Waveform of a Flyback Main Switch**

There are two methods to clamp the voltage spike on the main switch, a resistor−capacitor−diode (RCD) clamp or a transient voltage suppressor (TVS).

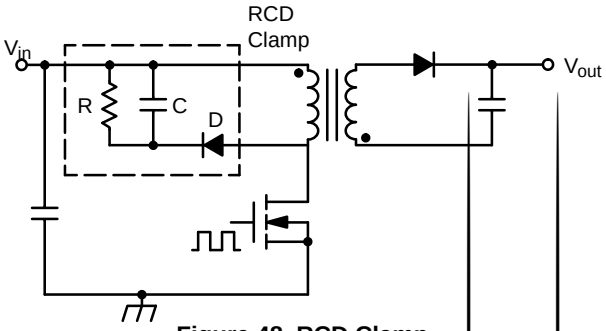



**Figure 48. RCD Clamp**

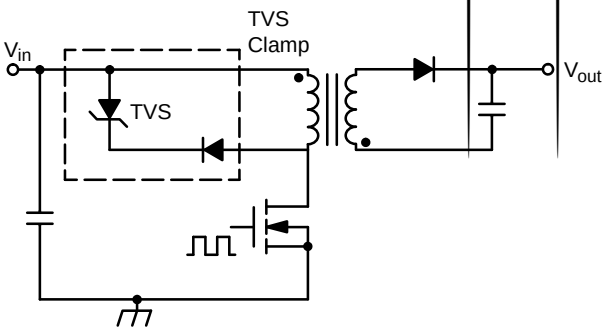



**Figure 49. TVS Clamp**

Both methods result in dissipation of the leakage energy in the clamping circuits – the dissipation is proportional to $LI^2$ where L is the leakage ïravefoer andckcurrent at turn

a fault event. Figure 50 shows double hiccup mode operation. A soft−start sequence is initiated the second time $V_{CC}$ reaches $V_{CC(on)}$. If the controller is latched upon reaching $V_{CC(on)}$, the controller stays in hiccup mode. During this mode, $V_{CC}$ never drops below $V_{CC(reset)}$, the controller logic reset level. This prevents latched faults to be cleared unless power to the controller is completely removed (i.e. unplugging the supply from the AC line).

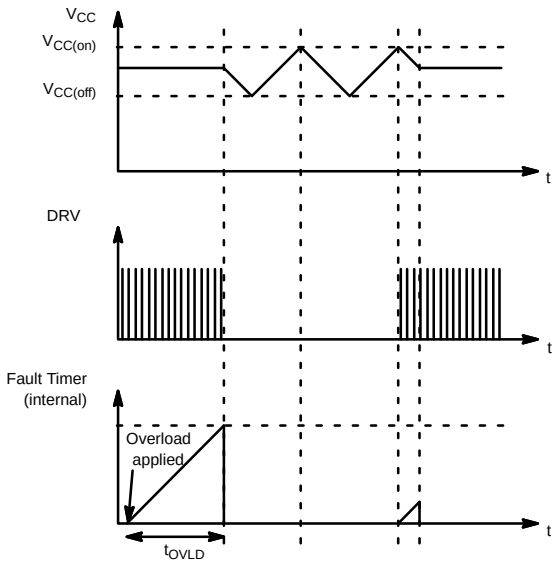



**Figure 50. $V_{CC}$ Double Hiccup Operation with a Fault Occurring while the Startup Circuit is Disabled**

An internal supervisory circuit monitors the $V_{CC}$ voltage to prevent the controller from dissipating excessive power if the $V_{CC}$ pin is accidentally grounded. A lower level current source ($I_{inhibit}$) charges $C_{CC}$ from 0 V to $V_{inhibit}$, typically 0.85 V. Once $V_{CC}$ exceeds $V_{inhibit}$, the startup current source is enabled. This behavior is illustrated in

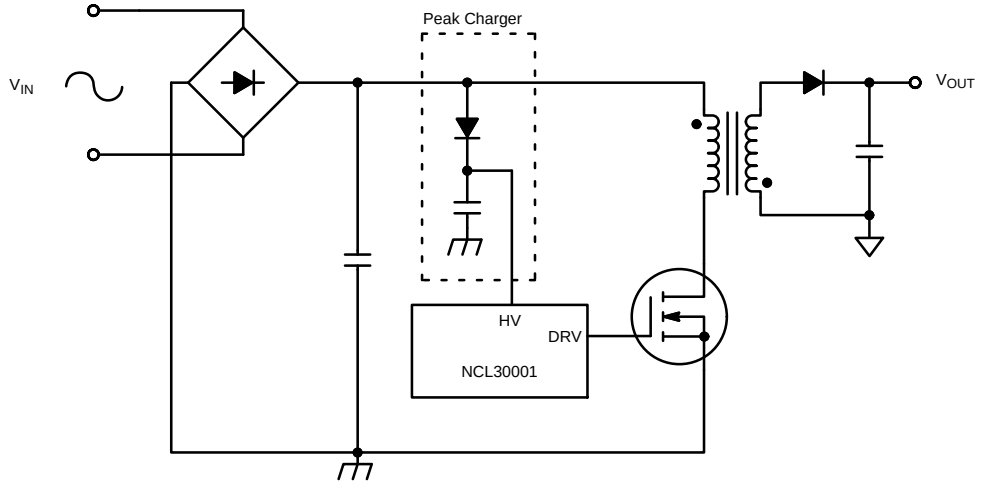



**Figure 52. Peak Charger**

The startup circuit is rated at a maximum voltage of 500 V. Power dissipation should be controlled to avoid exceeding the maximum power dissipation of the controller. If dissipation on the controller is excessive, a resistor can be placed in series with the HV pin. This will reduce power dissipation on the controller and transfer it to the series resistor.

### Drive Output

DRV has a source resistance of 10.8 Ω (typical) and a sink resistance of 8.0 Ω (typical). The driver is enabled once $V_{CC}$ reaches $V_{CC(on)}$ and there are no faults present. They are disabled once $V_{CC}$ discharges to $V_{CC(off)}$. The high current drive capability of DRV may generate voltage spikes during switch transitions due to parasitic board inductance. Shortening the connection length between the driver and the load and using wider connections will reduce inductance−induced spikes.

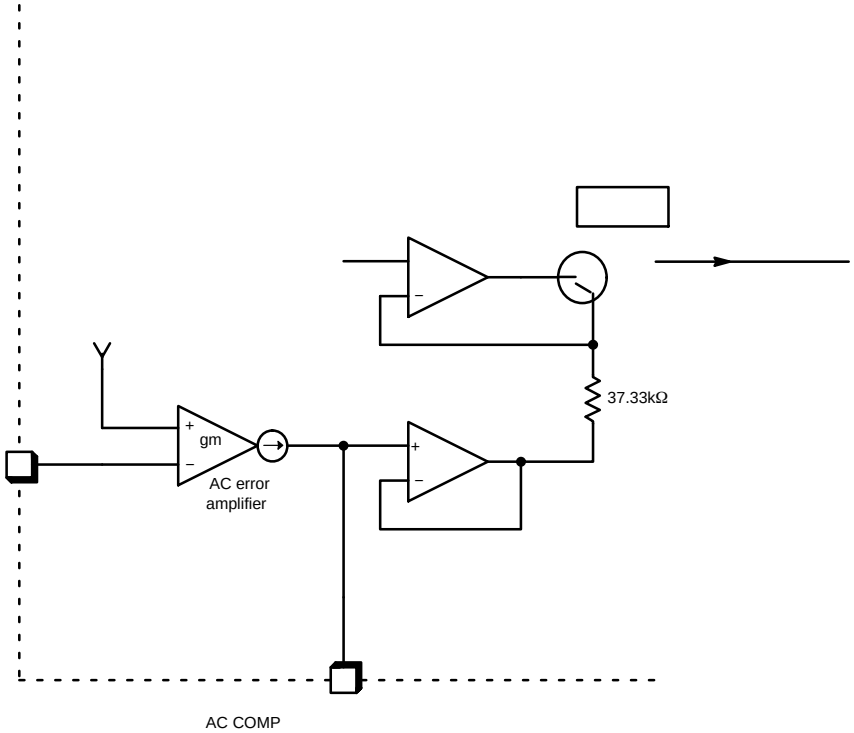
### AC Error Amplifier and Buffer

The AC error amplifier (EA) shapes the input current into a high quality sine wave by forcing the filtered input current to follow the output of the reference generator. The output of the reference generator is a full wave rectified ac signal and it is applied to the non inverting input of the EA. The filtered input current, $I_{in}$, is the current sense signal at the ISpos pin multiplied by the current sense amplifier gain. It is applied to the inverting input of the AC EA.

The AC EA is a transconductance amplifier. A transconductance amplifier generates an output current proportional to its differential input voltage. This amplifier has a nominal gain of 100 μS (or 0.0001 A/V). That is, an input voltage difference of 10 mV causes the output current to change by 1.0 μA. The AC EA has typical source and sink currents of 70 μA.

The filtered input current is a high frequency signal. A low frequency pole forces the average input current to follow the reference generator output. A pole-zero pair is created by placing a ($R_{COMP}$) and capacitor ($C_{COMP}$) series combination at the output of the AC EA. The AC COMP pin provides access to the AC EA output.

The output of the AC EA is inverted and converted into a current using a second transconductance amplifier. The output of the inverting transconductance amplifier is $V_{ACEA(buffer)}$. Figure 53 shows the circuit schematic of the AC EA buffer. The AC EA buffer output current, $I_{ACEA(out)}$, is given by Equation 1.


37.33kΩ
gm
AC error
amplifier
AC COMP

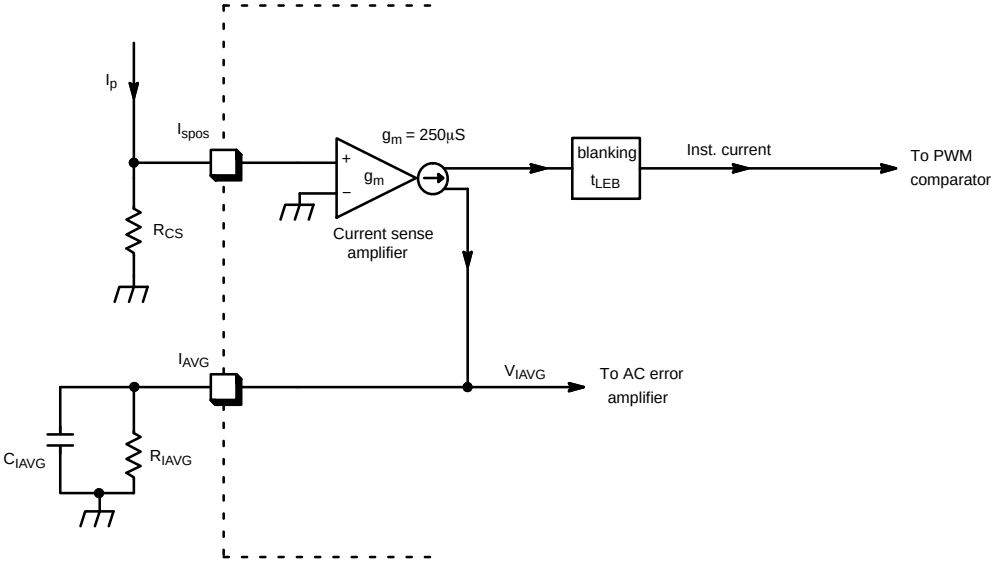



**Figure 54. Current Sense Amplifier**

Caution should be exercised when designing a filter between the current sense resistor and the $IS_{POS}$ input, due to the low impedance of this amplifier. Any series resistance due to a filter creates a voltage offset ($V_{OS}$) due to its input bias current, $CA_{Ibias}$. The input bias current is typically 60 μ

The gain of the low frequency current buffer is set by the resistor at the $I_{AVG}$ pin, $R_{IAVG}$. $R_{IAVG}$ sets the scaling factor betweetih1730(28.7528 Tm-4nary t6.9954 T2)TJ10 -9954 T2 pin, IAVG

### Output Overload

The Feedback Voltage, $V_{FB}$, is directly proportional to the output power of the converter. An internal 6.7 kΩ resistor pulls−up the FB voltage to the internal 6.5 V reference. An external optocoupler pulls down the FB voltage to regulate the output voltage of the system. The optocoupler is off during power up and output overload conditions allowing the FB voltage to reach its maximum level.

The NCL30001 monitors the FB voltage to detect an overload condition. A typical startup time of a single PFC stage converter is around 100 ms. If the converter is out of regulation (FB voltage exceeds 5.0 V) for more that 160 ms (typical) the drivers are disabled and the controller enters the double hiccup mode to reduce the average power dissipation. A new startup sequence is initiated after the double hiccup is complete. This protection feature is critical to reduce power during an output short condition.

### Soft−Skip Cycle Mode

The FB voltage reduces as the output power demand of the converter reduces. Once $V_{FB}$ drops below the skip threshold, $V_{SSKIP}$, 410 mV (typical) the driver is disabled. The skip comparator hysteresis is typically 90 mV.

The converter output voltage starts to decay because no additional output power is delivered. As the output voltage decreases the feedback voltage increases to maintain the output voltage in regulation. This mode of operation is known as skip mode. The skip mode frequency is dependent of load loop gain and output capacitance and can create audible noise due to mechanical resonance in the transformer and snubber capacitor. A proprietary Soft−Skip mode reduces audible noise by slowly increasing the primary peak current until it reaches its maximum value. The minimum skip ramp period, $t_{SSKIP}$, is 2.5 ms. Figure 56 shows the relationship between $V_{FB}$, $V_{SSKIP}$ and the primary current.

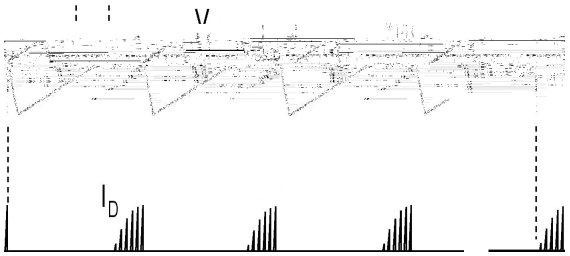



**Figure 56. Soft−Skip Operation**

Skip mode operation is synchronized to the ac line voltage. The NCL30001 disables Soft−Skip when the rectified ac line voltage drops to its valley level. This ensures the primary current always ramp up reducing audible noise. A skip event occurring as the ac line voltage is decreasing, causes the primary peak current to ramp down instead of ramp up. Once the skip period is over the primary current is only determined by the ac line voltage. A Soft−Skip event terminates once the AC−IN pin voltage decreases below/TT6p..34709 Tm0 66.8c.00001 Tc4-.0003 Tw2[outpu26(mV-6(0.4(49 1prop

converter. There is no error in the output signal due to the series rectifier as shown in Figure 58.

The scaled version of the full wave rectified input ac wave is applied to the AC_IN pin by means of a resistive voltage divider. The multiplier ramp is generated by comparing the scaled line voltage to the oscillator ramp with the AC_IN Comparator. The current signal from the V-I converter is factored by the AC_IN comparator output. The resulting signal is filtered by the low pass R-C filter on the CM pin. The low pass filter removes the high frequency content. The gain of the multiplier is determined by the V-I converter, the resistor on the CM pin, and the peak and valley voltages of the oscillator sawtooth ramp.

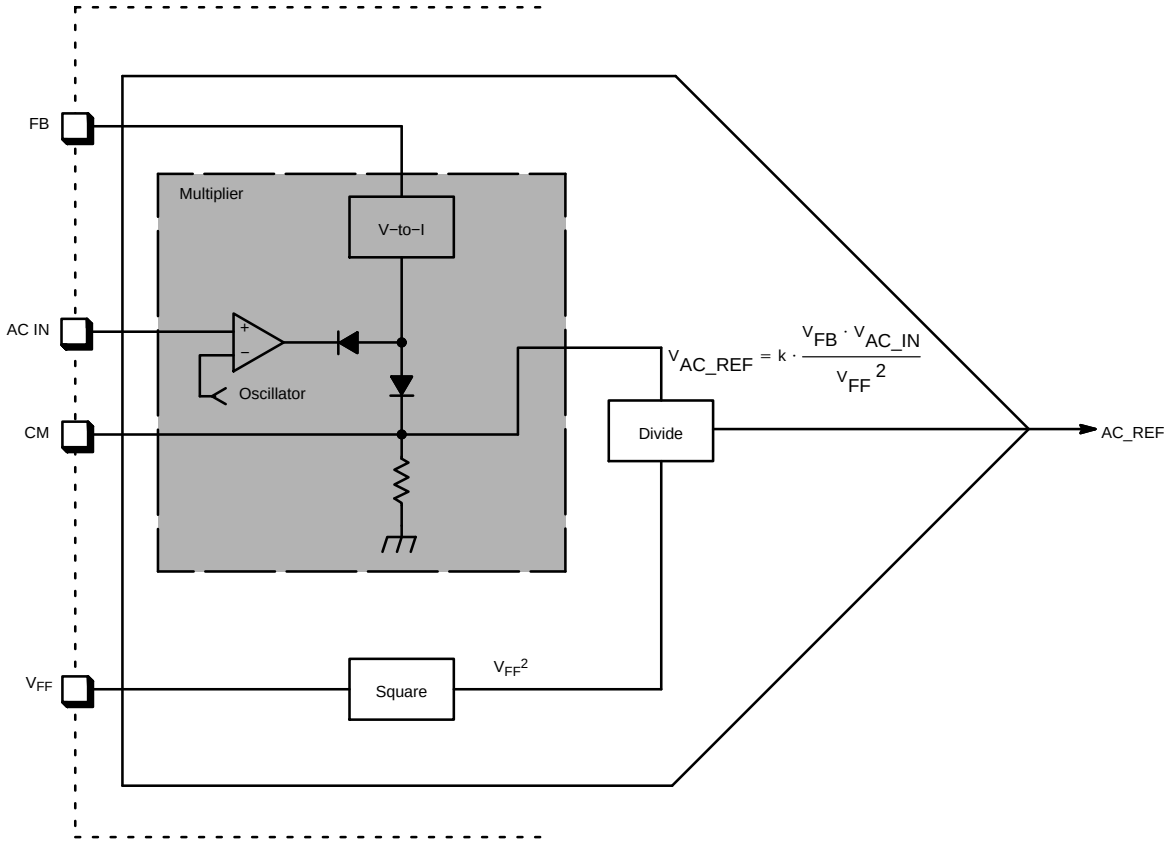



**Figure 58. Reference Generator**

The third input to the reference generator is the $V_{FF}$ signal. The $V_{FF}$ signal is a dc voltage proportional to the ac line voltage. A resistive voltage divider attenuates the full wave rectified line voltage between 0.7 and 5.0 V. The full wave rectified line is then averaged with a capacitor. The ac average voltage must be constant over each half cycle of the line. Line voltage ripple (120 Hz or 100 Hz) ripple on the $V_{FF}$ signal adds ripple to the output of the multiplier. This will distort the ac reference signal and reduce the power factor and increase the line current distortion. Excessive filtering delays the feedforward signal reducing the line transient response. A good starting point is to set the filter time constant to one cycle of the line voltage. The user can then optimize the filter for line transient response versus power factor. The average voltage on the $V_{FF}$ pin is:

$$V_{FF} = \frac{2}{\pi} Vac \sqrt{2\alpha} \qquad \text{(eq. 7)}$$

Where, $\alpha$ is the voltage divider ratio, normally 0.01.

V

$$V_{RCOMP} = \frac{di}{dt_{primary}} \cdot T \cdot R_{CS} \cdot A_{HF} \quad \text{(eq. 20)}$$

$$R_{CS} = \frac{N_S}{N_P} \cdot \frac{L_P \cdot 102.38k}{T \cdot A_{HF} \cdot V_{out} \cdot R_{RCOMP}} \quad \text{(eq. 21)}$$

At low line and full load, the output of the ac error amplifier output is nearly saturated in a low state. While the ac error amplifier output is saturated, $I_{ACEA}$ is zero and does not contribute to the voltage across the internal 21.33 kΩ resistor on the PWM comparator non-inverting input. In this operation mode, the voltage across the 21.33 kΩ resistor is determined solely by the ramp compensation and the instantaneous switch current as given by Equation 22.

$$V_{ref(PWM)} = \left(V_{RCOMP} \cdot \frac{t_{on}}{T}\right) + V_{INST} \quad \text{(eq. 22)}$$

The voltage reference of the PWM Comparator, $V_{REF(PWM)}$, is 4 V. For these calculations, 3.8 V is used to provide some margin. The maximum instantaneous switch current voltage contribution, $V_{INST}$, is given by Equation 23.

$$V_{INST} = I_{PK} \cdot R_{CS} \cdot A_{HF} \quad \text{(eq. 23)}$$

Substituting Equation 23 in Equation 22, setting $V_{REF(PWM)}$ at 3.8 V (provides margin) and solving for $R_{RCOMP}$, Equation 24 is obtained.

$$R_{RCOMP} = \frac{102.38k}{\left(3.8 - 5.333 \cdot I_{PK} \cdot R_{CS}\right)} \cdot \frac{t_{on}}{T} \quad \text{(eq. 24)}$$

Replacing Equation 24 in Equation 21 we obtain:

$$R_{CS} = \frac{3.8}{\left(\frac{N_P}{N_S} \cdot \frac{A_{HF} \cdot V_{out} \cdot t_{on}}{L_P}\right) + 5.333\, I_{PK}} \quad \text{(eq. 25)}$$

### PWM Logic

The PWM and logic circuits are comprised of a PWM comparator, an RS flip-flop (latch) and an OR gate. The latch is Set dominant which means that if both R and S are high the S signal will dominate and Q will be high, which will hold the power switch off.

The NCL30001 uses a pulse width modulation scheme based on a fixed frequency oscillator. The oscillator generates a voltage ramp as well as a pulse in sync with the falling edge of the ramp. The pulse is an input to the PWM Logic and Driver block. While the oscillator pulse is present, the latch is reset, and the output drive is in its low state. On the falling edge of the pulse, the DRV goes high and the power switch begins conduction.

The instantaneous inductor current is summed with a current proportional to the ac error amplifier output voltage. This complex waveform is compared to the 4 V reference signal on the PWM comparator inverting input. When the signal at the non-inverting input to the PWM comparator exceeds 4 V, the output of the PWM comparator toggles to a high state which drives the Set input of the latch and turns the power switch off until the next clock cycle.

### Brown−Out

The NCL30001 incorporates a brown−out detection circuit to prevent the controller operate at low ac line voltages and reduce stress in power components. A scaled version of the rectified line voltage is applied to the VFF Pin by means of a resistor divider. This voltage is used by the brown out detector.

A brown−out condition exists if the feedforward voltage is below the brown−out exit threshold, $V_{BO(high)}$, typically 0.45 V. The brown−out detector has 175 mV hysteresis. The controller is enabled once $V_{FF}$ is above 0.63 V and $V_{CC}$ reaches $V_{CC(on)}$. Figure 59 shows the relationship between the brown−out, $V_{CC}$ and DRV signals.

**SOIC−16 9.90x3.90x1.37 1.27P**
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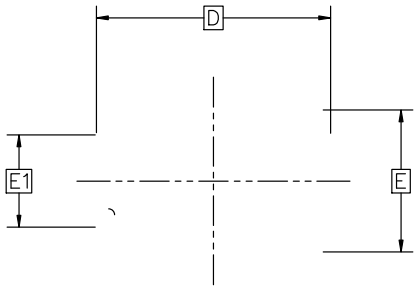
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.1[illegible]

nm TOTAL IN EXCESS OF THE

b DIMENSION AT MAXIMUM MATE




TOP VIEW

**SOIC−16 9.90x3.90x1.37 1.27P**
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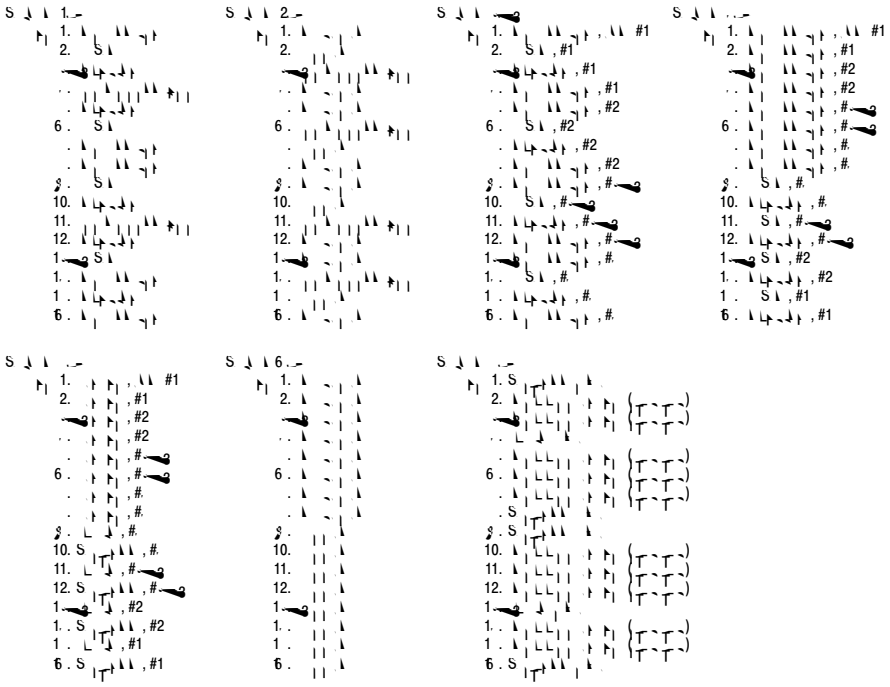
**GENERIC**
**MARKING DIAGRAM***



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb Free indicator