Features

- Voltage Mode CrM Power Factor Correction Controller
- PFC Open Feedback Loop Protection
- PFC Undervoltage Detector
- PFC Overvoltage Detector
- Half−Bridge Stage with 600 V High Side Gate Drive
- State Machine Ensures Proper Turn−on and Turn−off of Half−Bridge Stage
- Controllers are Properly Sequenced for Fault Fr1€

January,
a 600 V startup circuit and an adjustable frequency oscillator with a divide by 2 circuit to assure 50% symmetric duty ratio. The controllers are properly sequenced, simplifying system design.

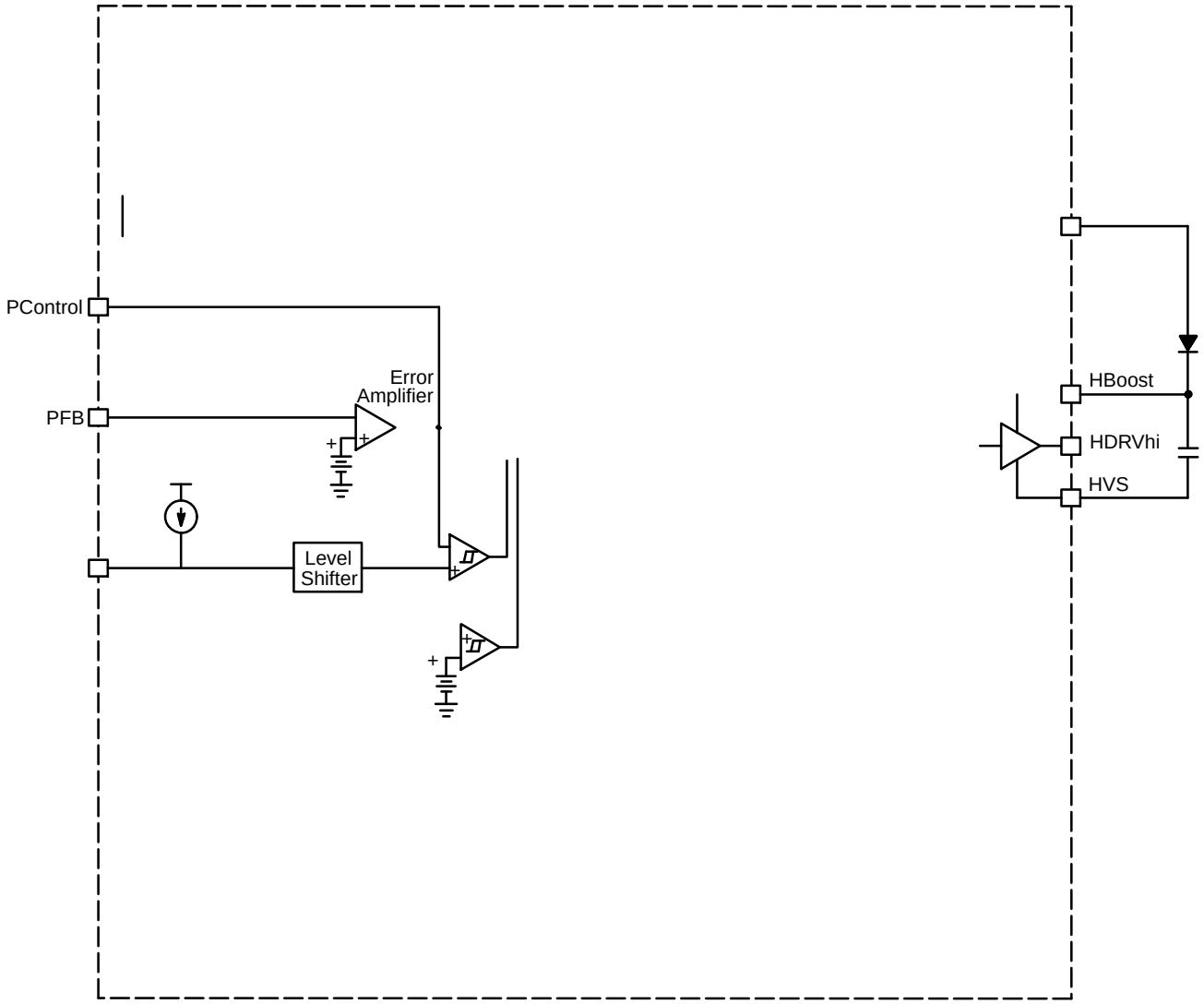


Figure 1. Functional Block Diagram

Table 2. MAXIMUM RATINGS (Notes 1 and 2)

Rating	Symbol	Value	Unit
High Voltage Input Voltage	V_{HV}	−0.3 to 600	V
High Voltage Input Current	I_{HV}	10	mA
Supply Input Voltage	V_{CC}	−0.3 to 20	V
Supply Input Current	I_{CC}	10	mA
Oscillator Input Voltage	V_{OSC}	−0.3 to V_{REF}	V
Oscillator Input Current	I_{OSC}	10	mA
Bandgap Reference Decoupling Output Voltage	V_{REF}	−0.3 to 9	V
Bandgap Reference Decoupling Output Current	I_{REF}	10	mA
PFC Feedback Voltage Input Voltage	V_{PFB}	−0.3 to 10	V
PFC Feedback Voltage Input Current	I_{PFB}	10	mA
PFC Current Sense Input Voltage	V_{PCS}	−0.3 to 10	V
PFC Current Sense Input Current	I_{PCS}	10	mA
PFC Zero Current Detection Input Voltage	V_{PZCD}	−0.3 to 10	V
PFC Zero Current Detection Input Current	I_{PZCD}	10	mA
PFC Control Input Voltage	$V_{PControl}$	−0.3 to V_{REF}	V
PFC Control Input Current	$I_{PControl}$	1.2	mA
PFC On Time Control Input Voltage	V_{PCT}	−0.3 to V_{REF}	V
PFC On Time Control Input Current	I_{PCT}	9	mA
PFC Drive Signal Voltage	V_{PDRV}	−0.3 to V_{CC}	V
PFC Drive Signal Current	I_{PDRV}	100	mA
Half−Bridge Low Side Driver Input Voltage	V_{HDRVlo}	−0.3 to V_{CC}	V
Half−Bridge Low Side Driver Input Current	I_{HDRVlo}	100	mA
Half−Bridge High Side Driver Source Connection Input Voltage	V_{HVS}	−1.0 to 600	V
Half−Bridge High Side Driver Source Connection Input Current	I_{HVS}	100	mA
Half−Bridge High Side Driver Input Voltage	V_{HDRVhi}	−1.3 to V_{HVS}+V_{CC}	V
Half−Bridge High Side Driver Input Current	I_{HDRVhi}	100	mA
Half−Bridge High Side Driver Charge Pump Input Voltage	V_{HBoost}	−0.3 to V_{HVS}+V_{CC}	V
Half−Bridge High Side Driver Charge Pump Input Current	I_{HBoost}	100	mA
High Side Boost Circuit Supply Voltage (between HBoost and HVS pins)	$V_{HBoost(supply)}$	−0.3 to V_{CC}	V
High Side Boost Circuit Supply Voltage (between HBoost and HVS pins)	$I_{HBoost(supply)}$	100	mA
Half−Bridge High Side Driver Source Connection Slew Rate	dV_{HVS}/dt	50	V/ns
Junction Temperature (Biased)	T_J	150	°C
Storage Temperature Range	T_{stg}	–60 to 150	°C
Power Dissipation (T_A = 25°C, 1 Oz Cu, 0.155 Sq Inch, Printed Circuit Copper Clad) D Suffix, Plastic Package Case 751B−05 (SOIC−16)	P_D	0.95	W
Thermal Resistance, Junction to Ambient (1 Oz Cu, 0.155 Sq Inch, Printed Circuit Copper Clad) D Suffix, Plastic Package Case 751B−05 (SOIC−16)	$R_{\theta JA}$	130	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device(s) contains ESD protection and exceeds the following tests:
   Pins 1, 14, 15 and 16 rated to the maximum voltage of the respective pins based on the maximum ratings table.
   All Other Pins: Human Body Model 1500 V per JEDEC Standard JESD22−A114E.
   Machine Model 150 V per JEDEC Standard JESD22−A115−A.
2. This device contains Latch−Up protection and exceeds ± 100 mA per JEDEC Standard JESD78.

Table 3. ELECTRICAL CHARACTERISTICS (V_{HV} = open, V_{PFB} = 2.4 V, V_{PCS} = 0 V, V_{PZCD} = 5 V, $V_{PControl}$ = open, V_{CC} = 15 V, V_{PDRV} = open, V_{HDRVlo} = open, V_{HVS} = 0 V, V_{HDRVhi} = open, V_{HBoost} = 15 V, C_{OSC} = 2200 pF, C_{VREF} = 0.1 μF, C_{PCT} = 1000 pF, for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

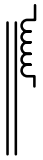
Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Supply Voltage						V
Startup Threshold	V_{CC} Increasing	$V_{CC(on)}$	14.3	15.3	16.3	
Minimum Enable Threshold	V_{CC} Decreasing	$V_{CC(enable)}$	13.6	14.6	15.6	
Minimum Operating Voltage	V_{CC} Decreasing	$V_{CC(off)}$	8.5	9.3	10.0	
Supply Current						mA
Device Disabled/Fault	$V_{PFB} = V_{PUVP(low)}$	I_{CC1}	0.8	1.4	1.8	
Device Switching	(Note 3)	I_{CC2}	1.8	2.4	3.0	
Startup Current	$V_{CC} = V_{CC\ (on)} - 0.2$ V, V_{HV} = 50 V	I_{start}	3.0	7.5	10.5	mA
Startup Circuit Off−State Leakage Current	V_{HV} = 600 V, $V_{CC} = V_{CC\ (on)} + 0.2$ V	$I_{HV(off)}$	–	15	50	μA
BANDGAP REFERENCE						
Reference Voltage	C_{REF} = 0.1 μF	V_{REF}	6.605	7.000	7.295	V
OSCILLATOR						
Half−Bridge Clock Frequency	V_{HVS} = 50 V	f_{clock}	13.5	15.5	16.5	kHz
Maximum Half−Bridge Clock Frequency	C_{OSC} = open	$f_{clock(MAX)}$	75	–	–	kHz
PFC ERROR AMPLIFIER						
PFC Feedback Voltage Reference		V_{PREF}				V
	0°C < T_J < 125°C		2.42	2.50	2.58	
	−40°C < T_J < 125°C		2.40	–	2.60	
PFC Feedback Voltage Reference Regulation with Line	$V_{CC(on)} + 0.2\ V < V_{CC} < 20$ V	$V_{PREF(line)}$	−15	–	15	mV
Error Amplifier Drive Capability						μA
Sink	$V_{PControl}$ = 4 V, V_{PFB} = 5 V	$I_{EA(SNK)}$	60	80	–	
Source	$V_{PControl}$ = 4 V, V_{PFB} = 0.5 V	$I_{EA(SRC)}$	−60	−80	–	

Open Loop Error Amplifier

30.72 .8 409.68 Tm0 Tc43 ref55[(T 2 T72 15T72 1Tm0 Tc(80)Tj-.2s[(CC()-19.8(o)-18.3(n .72 refBT8

Table 5. ELECTRICAL CHARACTERISTICS

DETAILED OPERATING DESCRIPTION



- Low pin-count of controller combines strong feature set
- Low external component count
- ZVS of the second stage FETs without any tuning requirements
- High efficiency facilitates improved thermal performance
- Low EMI and easy filtering due to fixed frequency
- Facilitation of synchronous rectification control design
- Easier design of magnetic components (esp. Resonant transformer and inductor)

While the above listed benefits make this approach a very interesting proposition for many isolated applications

PFC Output Capacitor - Cbulk

The bulk capacitor is one of the most critical components

High Voltage Startup Circuit

The NCL30051 internal startup regulator eliminates the need for external startup components. In addition, this regulator increases the efficiency of the supply as it uses no power when in the normal mode of operation, but instead uses power supplied by an auxiliary winding. The startup regulator consists of a constant current source that supplies current from the high voltage line (V_{in}) to the supply capacitor on the V_{CC} pin (C_{CC}). The startup current (I_{start}) is typically 7.5 mA. The startup circuit is rated at a maximum voltage of 600 V.

Once C_{CC} is charged to 15.3 V ($V_{CC(on)}$), the startup regulator is disabled and the PFC controller is enabled if the PFB voltage exceeds $V_{PUVP(high)}$. The startup regulator remains disabled until the lower supply threshold, $V_{CC(off)}$, (typically 9.3 V) is reached. Once reached, the drive outputs are disabled and the startup current source is enabled. Once the outputs are disabled, the bias current of the NCL30051 is reduced, allowing V_{CC} to charge back up.

The supply capacitor provides power to the controller while operating in the power up or self−bias mode. During the converter power up, C_{CC} must be sized such that a V_{CC} voltage greater than $V_{CC(off)}$ is maintained while the auxiliary supply voltage is building up. Otherwise, V_{CC} will collapse and the controller will turn off. The IC bias current and gate charge load at the drive outputs must be considered to correctly size C_{CC}. The increase in current consumption due to external gate charge is calculated using Equation 1.

$$I_{CC(gate\ charge)} = f \cdot Q_G \qquad \text{(eq. 1)}$$

where, f is the operating frequency and Q_G is the gate charge of the external MOSFETs.

Main Oscillator

The oscillator frequency is set by the oscillator capacitor, C_{OSC}, on the OSC pin. The oscillator operates at a fixed 80% duty ratio. A current source charges C_{OSC} to its peak voltage, typically 5 V. Once the peak voltage is reached, the charge current is disabled and C_{OSC} is discharged down to 3 V by another current source. The charge and discharge currents are typically 173 and 692 μA, respectively. The oscillator frequency vs oscillator capacitance graph is shown in Figure 3.

CC

Figure 3. Oscillator Frequency vs. Oscillator Capacitor

PFC Regulator

The PFC inductor current, $I_{L(t)}$, reaches zero at the end of the switch cycle as shown in Figure 4 and the average input current, $I_{in(t)}$, is in phase with the ac line voltage, $V_{in(t)}$.

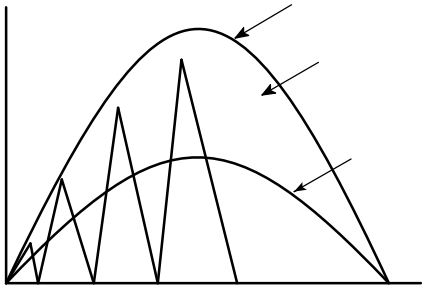


Figure 4. Inductor Current in CrM

PFC Startup

The output of the error amplifier is pulled low with an internal pull down transistor when the supply voltage has not reached $V_{CC(on)}$ or if there is a PFC undervoltage fault. This ensures a soft−start sequence once the PFC is enabled and eliminates output voltage overshoot during on/off tests. Once the error amplifier is enabled the output of the error amplifier charges quickly to the minimum clamp voltage.

Off Time Control

The PFC off time varies with the instantaneous line voltage and it is adjusted every cycle to allow the inductor current to reach zero before the next switch cycle begins. The inductor is demagnetized once its current reaches zero. Once the inductor is demagnetized the drain voltage of the PFC switch begins to drop. The inductor demagnetization is detected by sensing the voltage across the inductor using an auxiliary winding. This winding is commonly known as a zero crossing detector (ZCD) winding. This winding provides a scaled version of the inductor voltage. Figure 6 shows the ZCD winding arrangement.

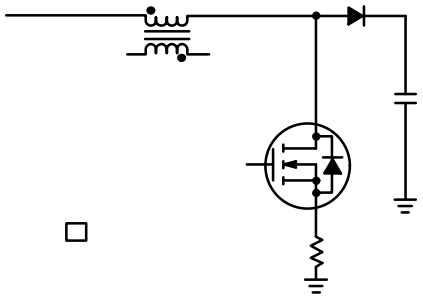


Figure 6. ZCD Winding Implementation

$$V_{PFC} = V_{PREF} \cdot \frac{R_1 + R_2}{R_2} + I_{PFB} \cdot$$

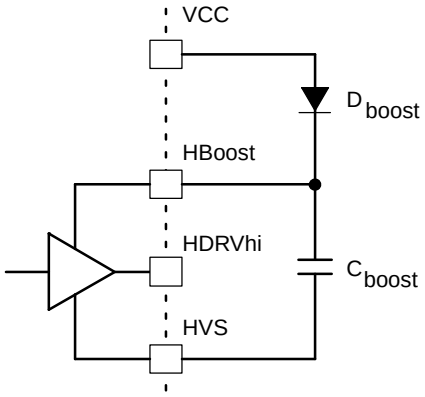


Figure 10. Half−bridge High Side Driver

A boost circuit comprised of D_{boost} and C_{boost} generates the supply voltage for the high side driver. Once HDRVlo turns on, the HVS pin is effectively grounded through the external power switch. This allows C_{boost} to charge to V_{CC}. Once HDRVlo turns off, HVS floats high and D_{boost} is reversed biased. An undervoltage detector monitors the HBoost voltage. Once the HBoost voltage is greater than $V_{Boost(UV)}$, typically, 6.1 V, the high side driver is enabled. The low side driver generally starts before the high side driver because the boost voltage is generated by the low side driver switch transitions.

The half−bridge low side driver source and sink impedances are typically 75 and 15 Ω, respectively. The half−bridge high side driver source and sink impedances are typically 75 and 15 Ω, respectively. Depending on the external MOSFETs gate charge requirements, an external driver may be needed to drive the low and high side power switches.

Analog and Power Ground

The NCL30051 has an analog ground, GND, and a power ground, PGND, terminal. GND is used for analog connections such as VREF and OSC. PGND is used for high current connections such as the gate drivers. It is recommended to have independent analog and power ground planes and connect them at a single point, preferably at the ground terminal of the system. This will prevent high current flowing on PGND from injecting noise in GND. The PGND connection should be as short and wide as possible to reduce inductance−induced spikes.

SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.1[illegible]

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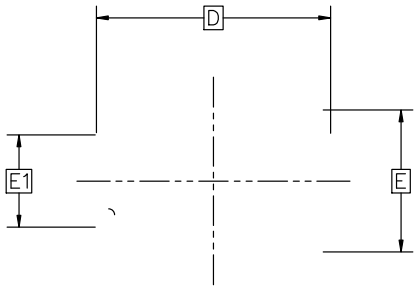

TOP VIEW

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CASE 751B
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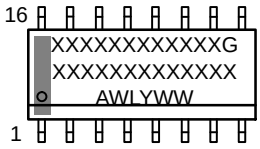
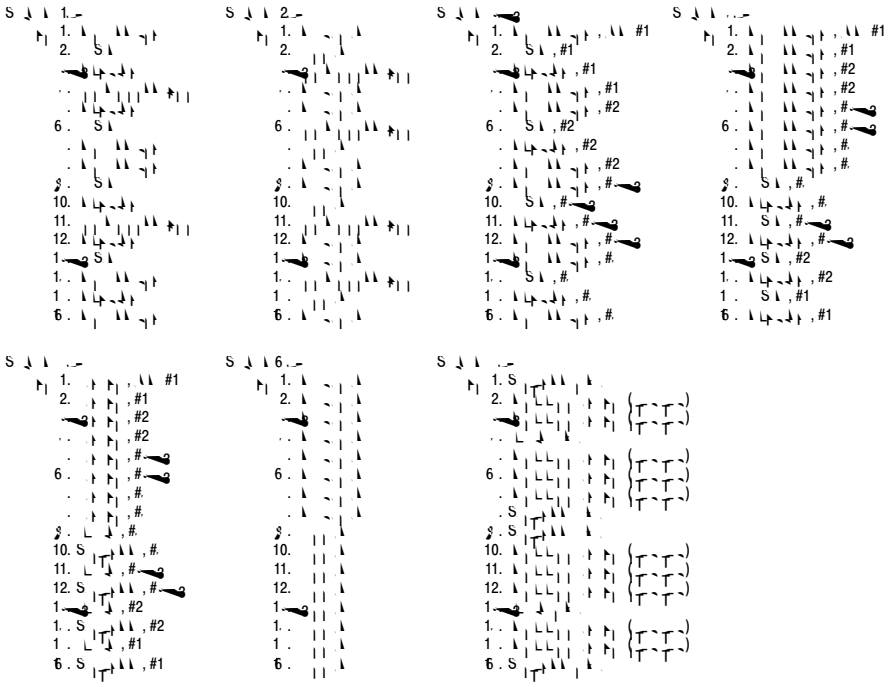
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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