CL30060

H F LED D H Vt Vt V

The NCL30060 is a switch mode power supply controller intended for low to medium power single stage power factor (PF) corrected LED Drivers. It employs a constant on−time control method to ensure near unity power factor across a wide range of input voltages and output power. It can be used for isolated flyback as well as buck topologies. The device offers a suite of robust protection features to ensure safe operation under a range of fault conditions.

Version NCL30060B2 is intended for constant voltage (CV) regulated output drivers where a DC−DC converter or linear regulator in the second stage controls the current to the LEDs so the output short circuit protection detector function has been disabled. Version NCL30060B3 is intended for applications not requiring Brown Out protection or output short circuit protection as typical with low standby operation. The NCL30060B4 removes on−time modulation for solutions not needing this feature.

Features

- Built−In High Voltage Start−up Circuit
- Direct Opto−coupler Feedback Connection
- Constant On−Time PWM Control
- Quasi−Resonant Switching
- Low Operating Current (1.6 mA typical)
- Source 250 mA / Sink 400 mA Totem Pole Gate Driver
- Integrated 12 V (typ) Gate Drive Clamp
- Frequency Dithering for Reduced EMI Profile
- Enable/Disable Function
- Dynamic Self−Supply (DSS) Operation
- Operating T_J from −40°C to 105°C
- Maximum On Time Protection
- Integrated Brown−out
- Overvoltage Protection
- Cycle−by−Cycle Overcurrent Protection
- Output Winding Short−Circuit Protection
- Thermal Shutdown
- These Devices are Pb−

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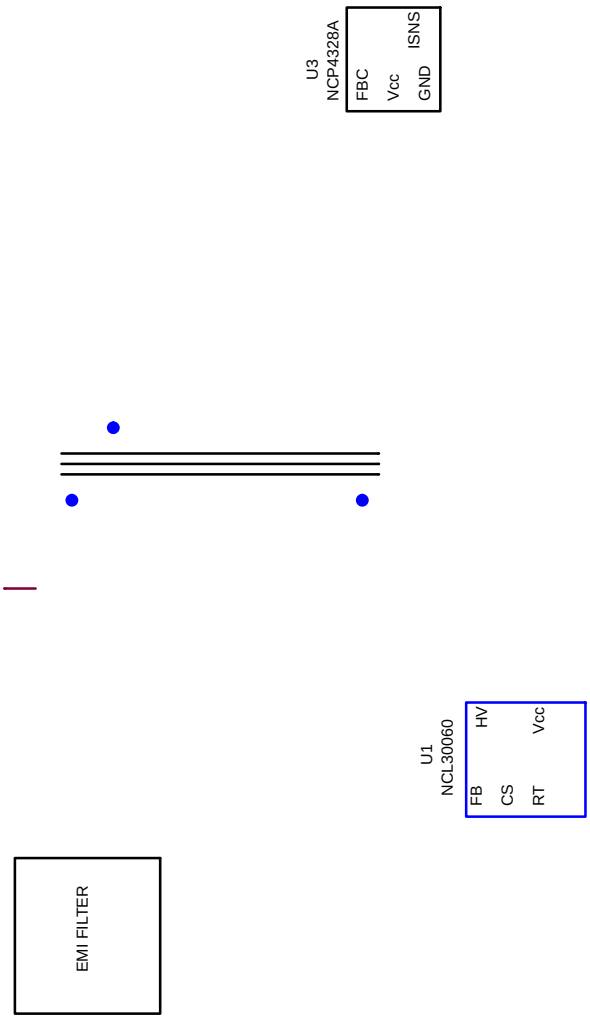

Figure 1. NCL30060 Typical Application Diagram

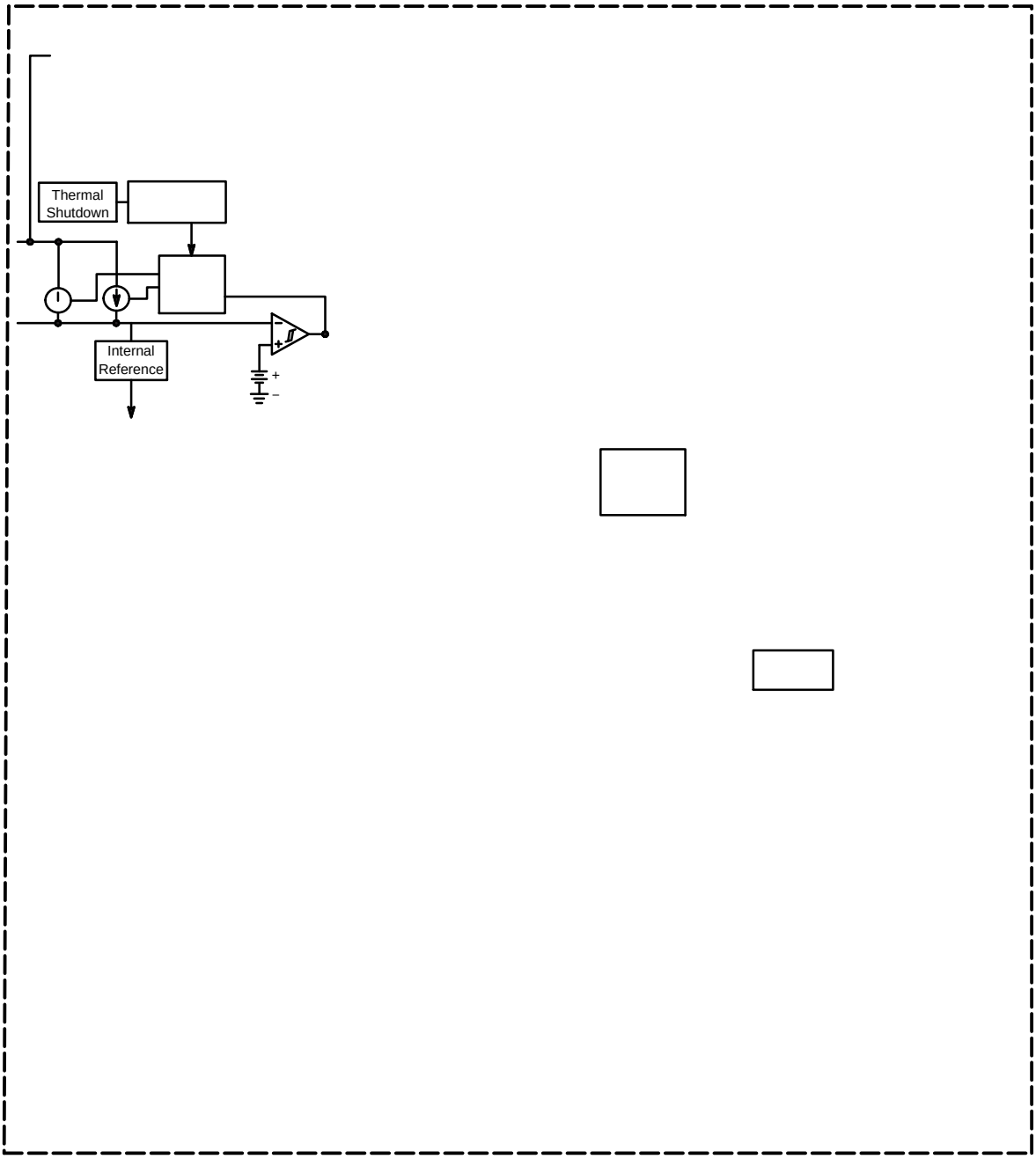

Figure 2. NCL30060 Internal Functional Block Diagram

Table 1. NCL30060 PIN FUNCTION DESCRIPTION

Pin No	Pin Name	Pin Description
1	FB	Feedback Input. The FB pin is the control input to the PWM comparator. A voltage level controlled by the feedback loop on this pin is compared to the internal ramp establishing power switch on time.
2	CS/ZCD	Current sense and zero current detection. The CS input is used to sense the instantaneous switch current in the external power switch during switch on time. A fast−responding high threshold level for short circuit detection is provided along with a longer blanking time at lower level for overload conditions. During switch off time, this pin monitors the bias winding to detect transformer demagnetization. When stored energy is depleted the gate drive turns on the power switch initiating the next cycle. This pin also detects overvoltage conditions through the bias winding. A blanking time prevents false overvoltage triggering due to noise.
3	RT	Maximum on−time adjust. The RT pin establishes the ramp charging current. The PWM comparator establishes the switch on time from the ramp and FB signal. Pulling the RT pin below the disable threshold forces the controller in the Armed mode where all switching functions cease.
4	GND	Ground. This is the ground reference for the controller. All bypassing and control components should be connected to the GND pin with a short trace length to minimize noise.
5	DRV	Drive. The high current capability of the totem pole gate drive makes it suitable to directly control high gate charge power MOSFETs. The driver stage provides both passive and active pull−down circuits which force the MOSFET gate off when VCC is below normal operating levels.
6	VCC	IC Supply. This is the positive supply of the controller and source for powering external circuits. Internal bias will be disabled when external power is sufficient to maintain operation.
7	NC	No−connect. This missing pin provides creepage distance.
8	HV	High−voltage input. Monitors input voltage for brown−out detection and power to operate controller.

Table 2. MAXIMUM RATINGS (Notes 1, 2, 3 and 4)

Rating	Symbol	Value	Unit
FB Voltage	V_{FB}	−0.3 to 10	V
FB Current	I_{FB}	±10	mA
CS/ZCD Voltage	$V_{CS/ZCD}$	−0.9 to 12.4	V
CS/ZCD Current	$I_{CS/ZCD}$	−2 / +5	mA
RT Voltage	V_{RT}	−0.3 to 5	V
RT Current	I_{RT}	±10	

ELECTRICAL CHARACTERISTICS (V_{CC} = 14 V, V_{HV} = 120 V, V_{FB} = 4 V, $V_{CS/ZCD}$ = 0 V, C_{DRV} = 1 nF, R_T = 20 kΩ, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 105°C, unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
CONSTANT ON TIME GENERATOR						
Maximum On−Time Feedback Voltage		V_{FB}				

ELECTRICAL CHARACTERISTICS (V_{CC} = 14 V, V_{HV} = 120 V, V_{FB} = 4 V, $V_{CS/ZCD}$ = 0 V, C_{DRV} = 1 nF, R_T = 20 kΩ, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 105°C, unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
OUTPUT SHORT CIRCUIT AND OVERVOLTAGE PROTECTION						
Output Short Off−Time Detector Threshold (Note 7)	Detected during DRV low	$t_{off(OS)}$	43	50	55	μs
Output Short Detection Integration Weighting Ratio (Note 7)	$N_{INTratio(OS)}$= Charging speed(Output Short detected) / Discharging speed (normal operation)	$N_{INTratio(OS)}$		20		
Output Short Detection Integration Time for Continuous Integration pulses (Note 7)		$t_{INTCON(OS)}$	36.7	40	45.7	ms
Overvoltage Threshold	DRV is low	V_{OVP}	5.8	6.0	6.2	V
Overvoltage Propagation Delay	$V_{CS/ZCD}$ = 0 V to 7 V ramp, dV/dt = 1 V/μs, $V_{CS/ZCD}$ = V_{OVP} to DRV low	$t_{OVP(PROP)}$	–	–	2.5	μs
Overvoltage Blanking		$t_{OVP(blank)}$	1.5	2.0	2.5	μs
Number of Consecutive Overvoltage Events to Enter Fault Mode Mode (Latch mode available on customer request)		n_{OVP}	–	4	–	
Auto−recovery Timer Duration		$t_{autorecovery}$	0.8	1.0	1.2	s
BROWN−OUT PROTECTION (does not apply to B1 and B3 options)						
System Startup Threshold		$V_{BO(start)}$	102	111	120	V
System Shutdown Threshold		$V_{BO(stop)}$	88	96	104	V
Brown−out Detection Blanking Time	V_{HV} decreasing, delay from $V_{BO(stop)}$ to drive disable	$t_{BO(stop)}$	43	54	65	ms
THERMAL PROTECTION						
Thermal Shutdown	Temperature increasing	T_{SHDN}				

−16Tm(1.0)TjET458.526 366.009 .90707 15.307TjE

DETAILED OPERATING DESCRIPTION

HIGH VOLTAGE STARTUP CIRCUIT

The NCL30060 integrates a 700 V startup regulator eliminating the need of external startup components. The startup regulator consists of a constant current source that supplies current from the high voltage input terminal (HV) to the supply capacitor on the VCC pin (C_{CC}). The startup circuit current (I_{start2}) and (I_{start3}) are disabled if the VCC pin is below $V_{CC(inhibit)}$. In this condition, the startup current is reduced to I_{start1}, typically 0.77 mA. In addition, this regulator reduces no load power and increases the system efficiency as it uses negligible power in the normal operation mode.

After VCC pin is higher than $V_{CC(inhibit)}$ threshold, the

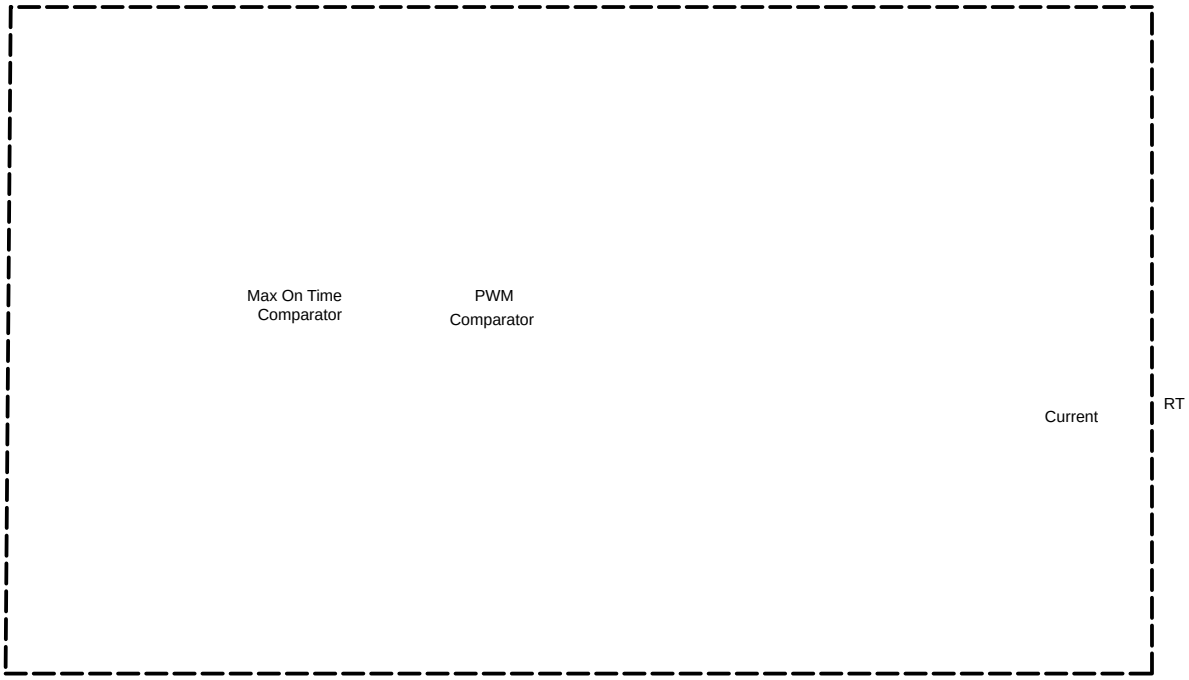

Figure 4. On−Time Control Architecture

Figure 7. Secondary Side Winding Short−Circuit Waveforms

Figure 7 shows simulation results for an output winding short. The simulation waveforms are described below:

- DRV/V is gate drive signal for the PFC switch.
- VCS/V is the signal on the CS/ZCD pin.
- ZCDW/V is the voltage across the ZCD winding.
- VHV1/V is the voltage on the HV pin.

The converter is operating normally and a momentary fault is applied at 24 ms. Once the fault is applied, the watchdog timer duration increases to t_{off2}. The fault is removed after two faults overcurrent events are detected. The fault is re−applied at 35 ms. After four consecutive overcurrent conditions are detected, the fault signal goes high.

ZERO CURRENT DETECTION

The off−time in a CrM topology varies with the instantaneous line voltage and it is adjusted every cycle to allow the inductor current to reach zero before the next switch cycle begins. The inductor is demagnetized once its current reaches zero. Once the inductor is demagnetized the drain voltage of the switch begins to fall. The inductor

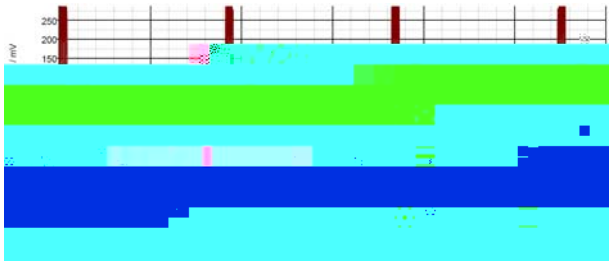

Figure 12. Output Short Detection and Protection Waveform

Versions NCL30060B2 and NCL30060B4 are intended for constant voltage (CV) regulated output drivers where a DC−DC converter or linear regulator in the second stage controls the current to the LEDs so the output short circuit protection detector function has been disabled. Version NCL30060B3 is useful in applications where the Brown Out function is not required and light load operation may trigger the output short circuit protection function. Ensure proper operation in fault modes.

BROWN OUT DETECTION

The NCL30060 includes brown out protection providing a defined shutdown for low input voltage. This feature is enabled after a V_{CC} reset event and does not allow the controller to enter Active mode until the input voltage is above the startup threshold, typically 111 V.

If the input voltage remains below the system shutdown threshold, typically 96 V, longer than the brown out detection blanking time, typically 54 ms, a shutdown flag is set. Gate drive pulses will continue to be issued until the input voltage is near the ac line voltage zero crossing. When a zero crossing is detected and the flag is set, gate drive pulses cease thereby stopping power delivery to the LED load. The brown out flag remains set and switching is suspended until the input voltage rises above the startup threshold.

Delaying termination of gate drive pulses until the zero crossing ensures the system is at a low power state before shutting down. This approach avoids a situation where energy stored in the input filter may artificially force the sensed voltage to cross the startup threshold if switching is abruptly terminated. A false startup level would be followed by crossing the shutdown threshold again. Such cycling on and off near the brown out threshold would result in LED

SOIC−7
CASE 751U
ISSUE E

SCALE 1:1

DATE 20 OCT 2009

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STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6.
7. NOT USED
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. NOT USED
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. NOT USED
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. NOT USED
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5.
6.
7. NOT USED
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6.
7. NOT USED
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. NOT USED
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR (DIE 1)
2. BASE (DIE 1)
3. BASE (DIE 2)
4. COLLECTOR (DIE 2)
5. COLLECTOR (DIE 2)
6. EMITTER (DIE 2)
7. NOT USED
8. COLLECTOR (DIE 1)

STYLE 9:
PIN 1. EMITTER (COMMON)
2. COLLECTOR (DIE 1)
3. COLLECTOR (DIE 2)
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE (DIE 2)
7. NOT USED
8. EMITTER (COMMON)

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. NOT USED
8. GROUND

STYLE 11:
PIN 1. SOURCE (DIE 1)
2. GATE (DIE 1)
3. SOURCE (DIE 2)
4. GATE (DIE 2)
5. DRAIN (DIE 2)
6. DRAIN (DIE 2)
7. NOT USED
8. DRAIN (DIE 1)