NCL30073

Current-Mode PWM Controller for LED Application

The NCL30073 is a highly integrated PWM controller capable of delivering a rugged and high performance LED converter in a tiny TSOP−6 package. With a supply range up to 24 V, the controller hosts a 65 kHz switching circuitry operated in peak current mode control. When the voltage on FB pin decreases, the controller enters skip cycle while limiting the peak current.

Over Power Protection (OPP) is a difficult exercise especially when no−load standby requirements drive the converter specifications. The ON proprietary integrated OPP lets you harness the maximum delivered power without affecting your standby performance simply via two external resistors. An Over Voltage Protection is also combined on the same pin but also on the V_{CC} line. They offer an efficient protection in case of adverse open loop operation.

Finally, a timer−based short−circuit protection offers the best protection scheme, letting you precisely select the protection trip point without caring of a loose coupling between the auxiliary and the power windings.

Features

- Fixed−frequency 65 kHz Current−mode Control Operation
- Internal and Adjustable Over Power Protection (OPP) Circuit
- Internal Ramp Compensation
- Internally Fixed 4 ms Soft−start
- 115 ms Timer−based Auto−recovery Short−circuit Protection
- Protection − Autorecovery
  - OVP by V_{CC}
  - OIP
  - OTP − Foldback
  - Short Circuit
- Up to 24 V V_{CC} Operation
- Extremely Low No−load Standby Power
- Isolated and Non−isolated Outputs
- Good Regulation – 5%
- High Power Factor > 0.9
- Single Winding Inductor
- Low Parts Count
- EPS 2.0 Compliant
- Pb−Free Devices
- +300 mA/ −500 mA Source/Sink Drive Capability

Typical Application

TYPICAL APPLICATION SCHEMATIC

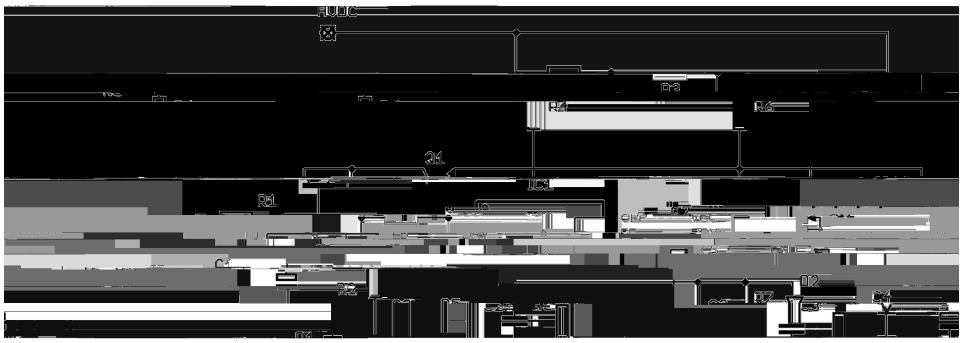


Figure 1. Typical Non−isolated (Buck−Boost) Application

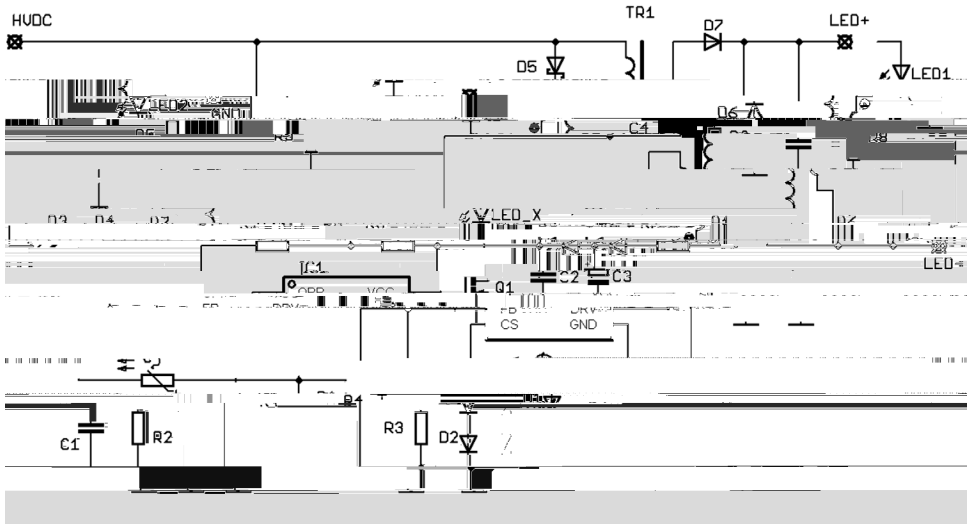


Figure 2. Typical Isolated (Flyback) Application Example

Table 1. PIN FUNCTION DESCRIPTION

Pin #	Pin Name	Function	Pin Description
1	OPP	Adjust the Over Power Protection	A resistive divider from the auxiliary winding to this pin sets the OPP compensation level. When brought above 3 V, the part enters auto−recovery mode.
2	FB	Feedback pin	A voltage variation on this pin will allow regulation.
3	CS	Current Sense + Slope Compensation	This pin monitors the primary peak current but also offers a means to introduce slope compensation.
4	GND		The controller ground.
5			

INTERNAL CIRCUIT ARCHITECTURE

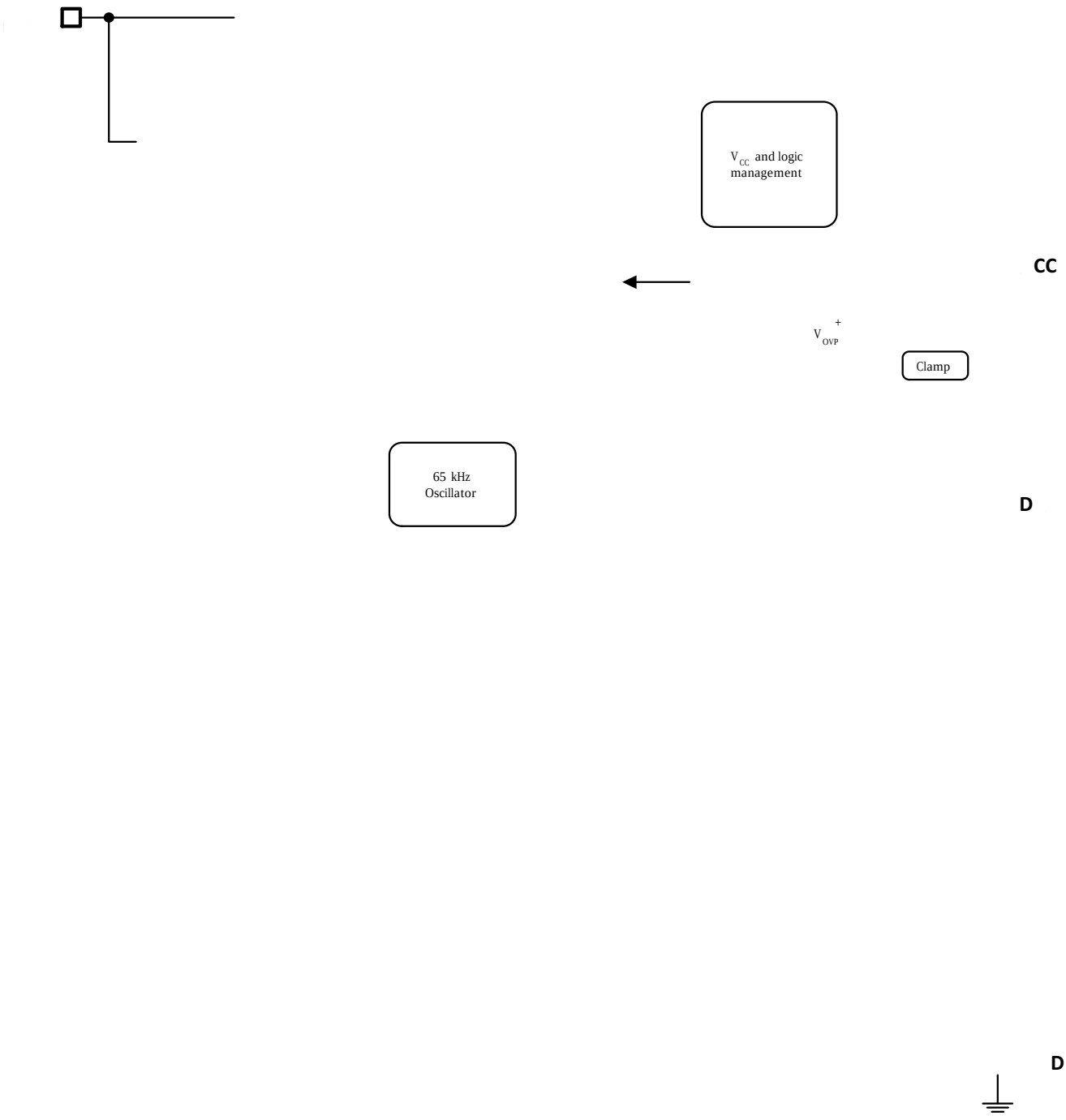


Figure 3. Internal Circuit Architecture

Table 3. ELECTRICAL CHARACTERISTICS

For typical values T_J = 25 C, for min/max values T_J = −40 C to +125 C, V_{CC} = 12 V unless otherwise noted.

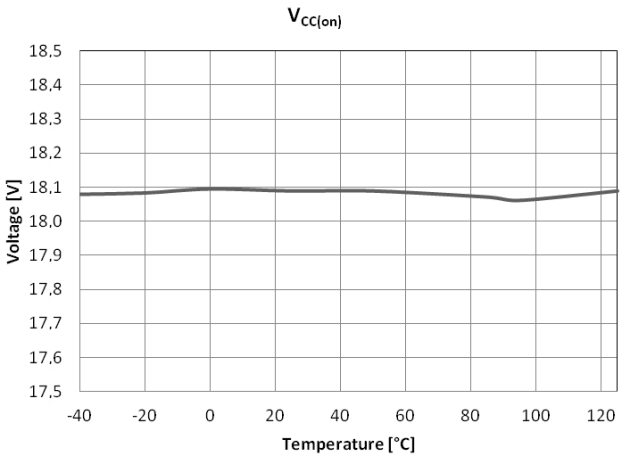
Symbol	Rating	Pin	Min	Typ	Max	Units
SUPPLY SECTION						
$V_{CC(on)}$	V_{CC} increasing level at which driving pulses are authorized	6	16	18	20	V
$V_{CC(min)}$	V_{CC} decreasing level at which driving pulses are stopped	6	8.3	8.9	9.5	V
$V_{CC(hyst)}$	Hysteresis $V_{CC(on)} – V_{CC(min)}$	6	7.7	–	–	V
$V_{CC(reset)}$	Auto−recovery state reset voltage	6	–	8.6	–	V
$V_{CC(reset\_hyst)}$	Defined hysteresis between minimum and reset voltage $V_{CC(min)} – V_{CC(reset)}$	6	0.15	0.30	0.45	V
I_{CC1}	Start−up current ($V_{CC(on)}$ – 100 mV)	6	–	6	10	μA
I_{CC2}	Internal IC consumption with V_{FB} = 3.2 V, f_{SW} = 65 kHz and C_L = 0 nF	6	–	1.0	1.4	mA
I_{CC3}	Internal IC consumption with V_{FB} = 3.2 V, f_{SW} = 65 kHz and C_L = 1 nF	6	–	1.8	2.7	mA
$I_{CC(no-load)}$	Internal consumption in skip mode – non switching, V_{FB} = 0 V	6	–	300		

Table 3. ELECTRICAL CHARACTERISTICS

For typical values T_J = 25 C, for min/max values T_J = −40 C to +125 C, V_{CC} = 12 V unless otherwise noted.

Symbol	Rating	Pin	Min	Typ	Max	Units
FEEDBACK SECTION						
R_{eq}	Internal equivalent feedback resistance	2	−	29	−	kΩ
K_{ratio}	FB pin to current set point division ratio	−	−	4	−	−
$V_{FB(freeze)}$	Feedback voltage below which the peak current is frozen	2	−	1	−	V
$V_{FB(limit)}$	Feedback voltage corresponding with maximum internal current set point	2	−	3.2	−	V
$V_{FB(open)}$	Internal pull−up voltage on FB pin	2	−	4	−	V
SKIP SECTION						
V_{skip}	Skip−cycle level voltage on the feedback pin	−	−	0.8	−	V
$V_{skip(hyst)}$	Hysteresis on the skip comparator (Note 4)	−	−	50	−	mV
INTERNAL SLOPE COMPENSATION						
V_{ramp}	Internal ramp level @ 25 C (Note 6)	3	−	2.5	−	V
R_{ramp}	Internal ramp resistance to CS pin	3	−	20	−	kΩ
PROTECTIONS						
$V_{(latch)}$	Fault level input on OPP pin	1	2.85	3.0	3.15	V
$t_{latch\ (blank)}$	Blanking time after Drive output turn off	1	−	1	−	μs
$t_{latch\ (count)}$	Number of clock cycles before fault is confirmed	1	−	4	−	
$t_{latch\ (del)}$	OVP/OTP delay time constant before fault is confirmed	1	−	600	−	ns
t_{fault}	Internal auto−recovery fault timer duration	−	100	115	130	ms
V_{OVP}	Over voltage protection on the VCC pin	6	24.0	25.5	27.0	V
$t_{OVP(del)}$	Delay time constant before OVP on VCC is confirmed	6	−	20	−	μs

4. Guaranteed by design.
5. Application parameter for information only.
6. 1 MΩ resistor is connected from pin 3 to the ground for the measurement.



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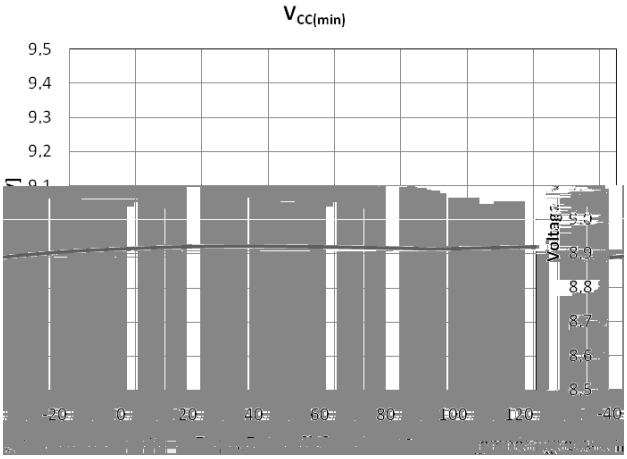

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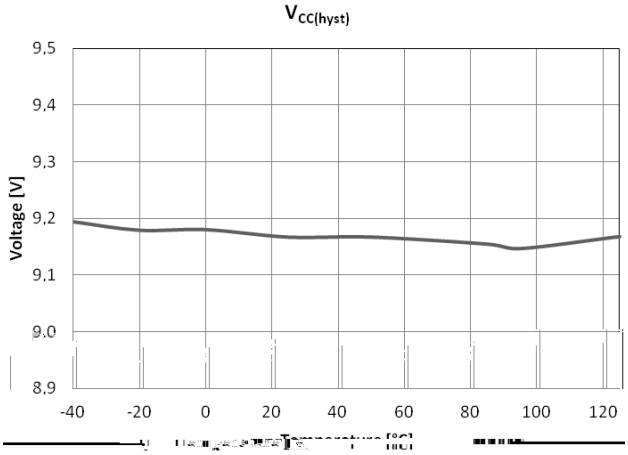

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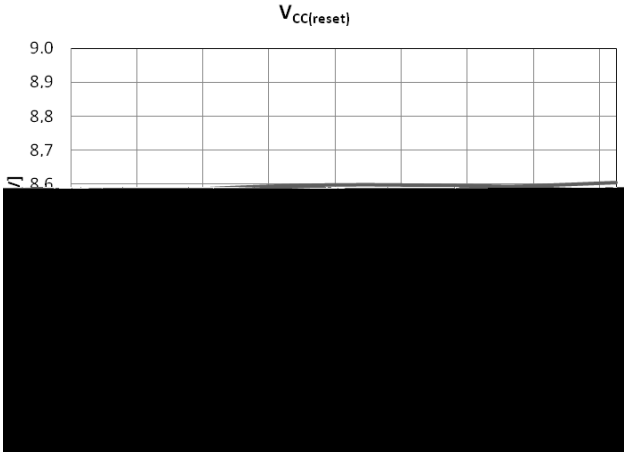

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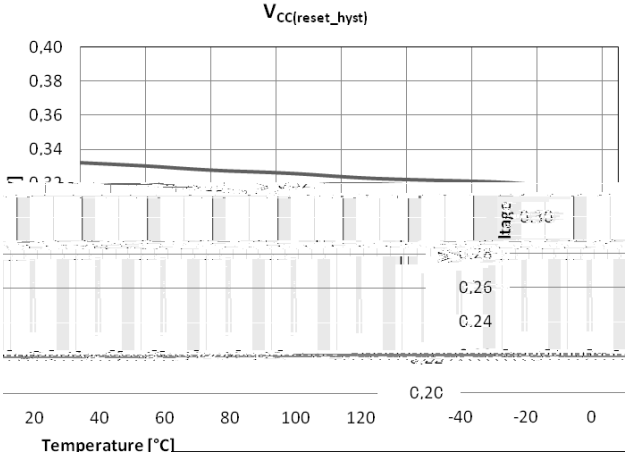

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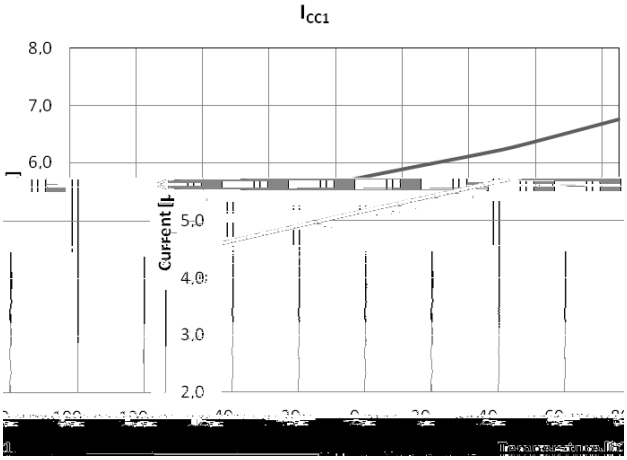

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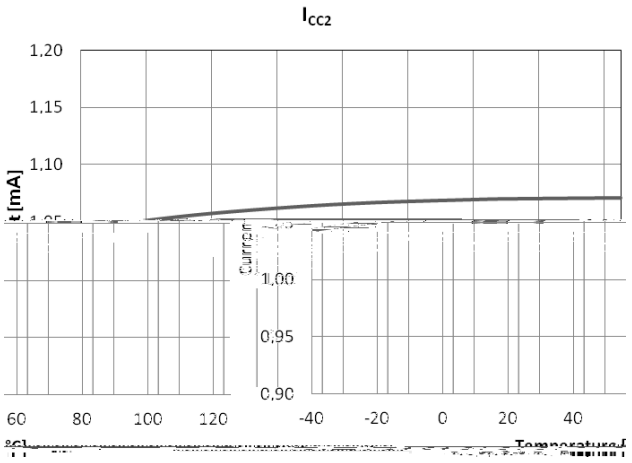

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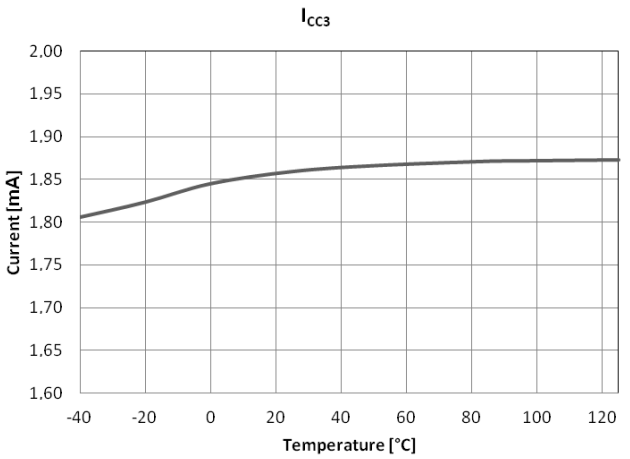

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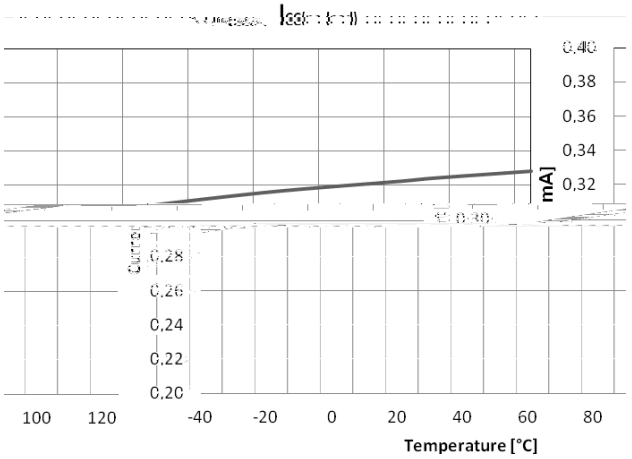

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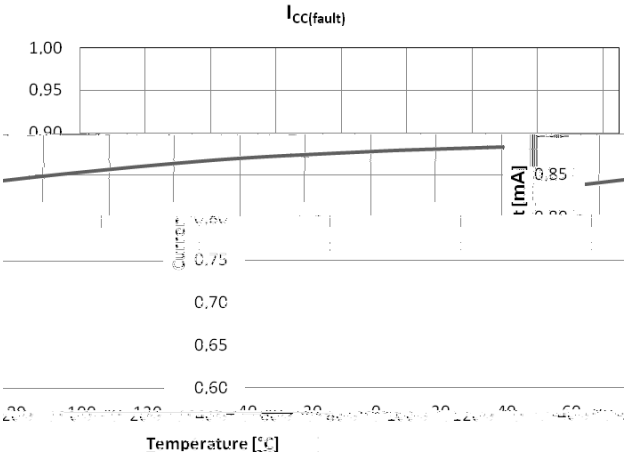

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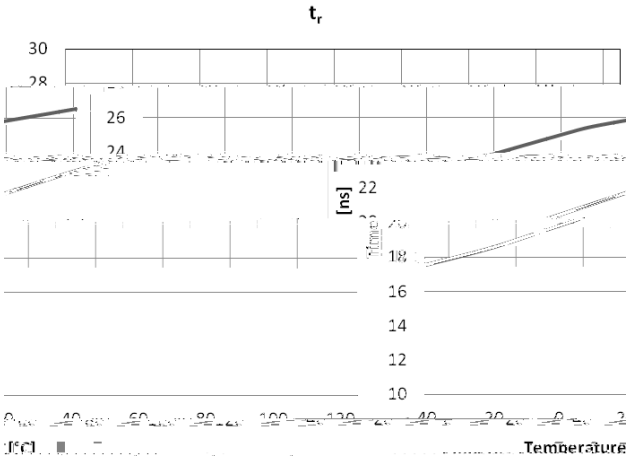

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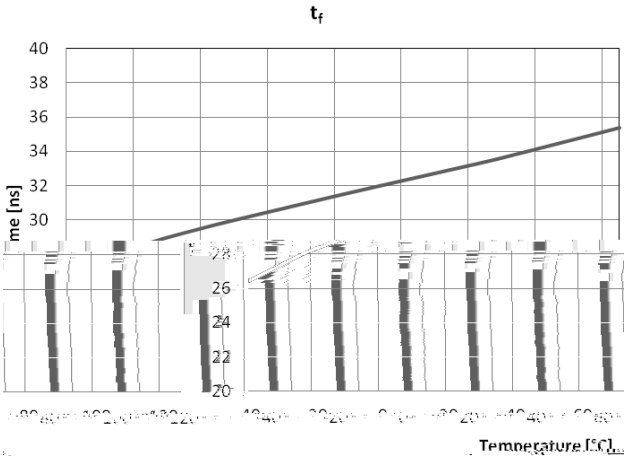

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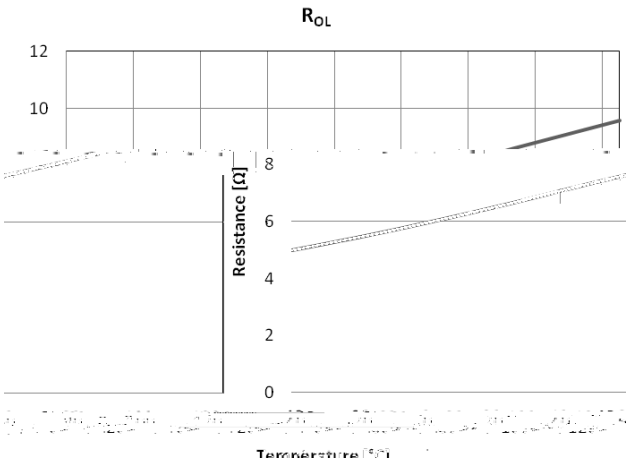

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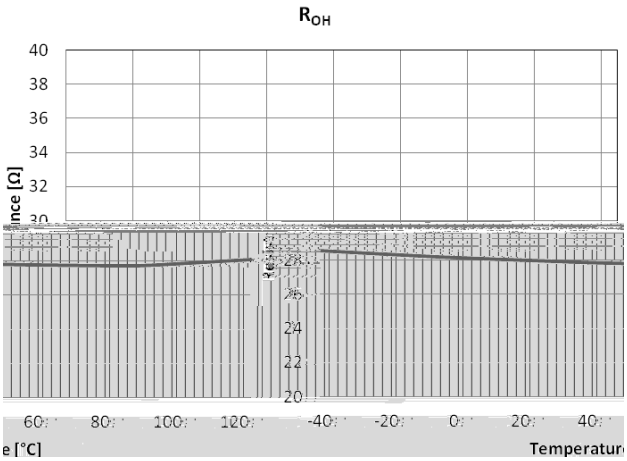

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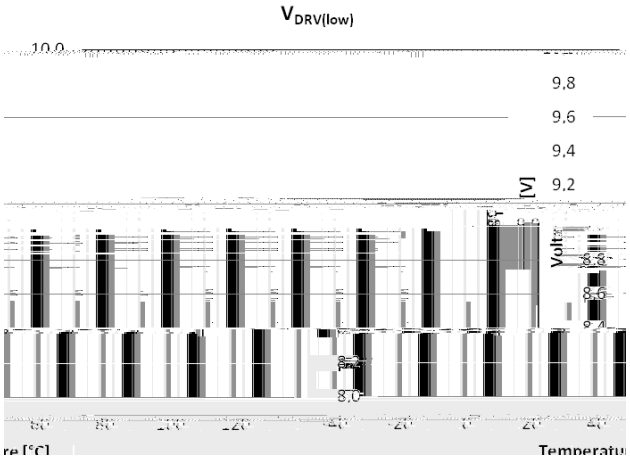

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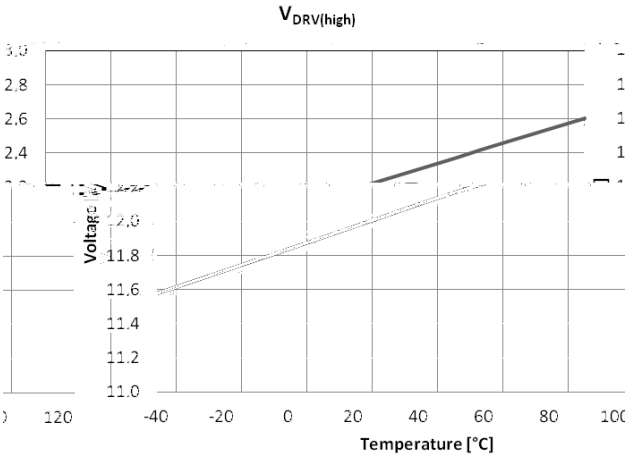

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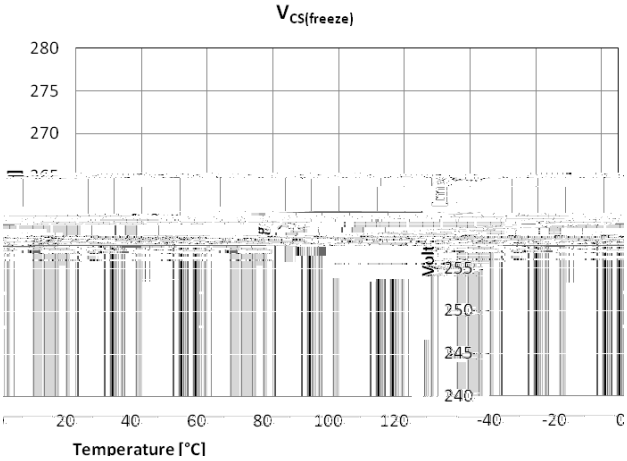

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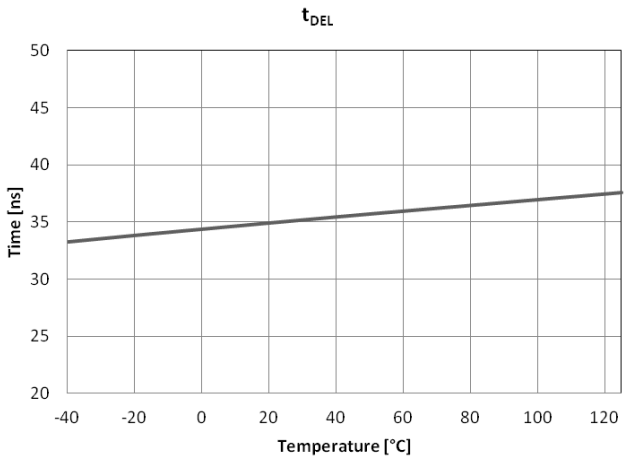

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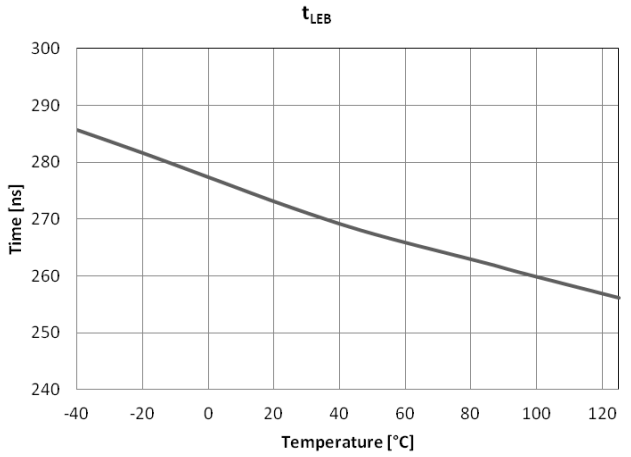

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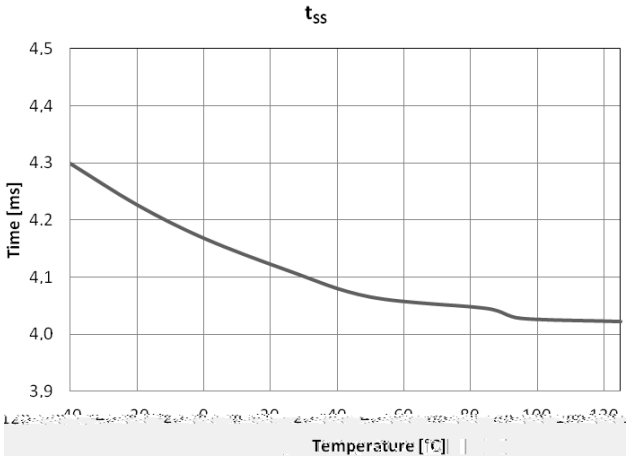

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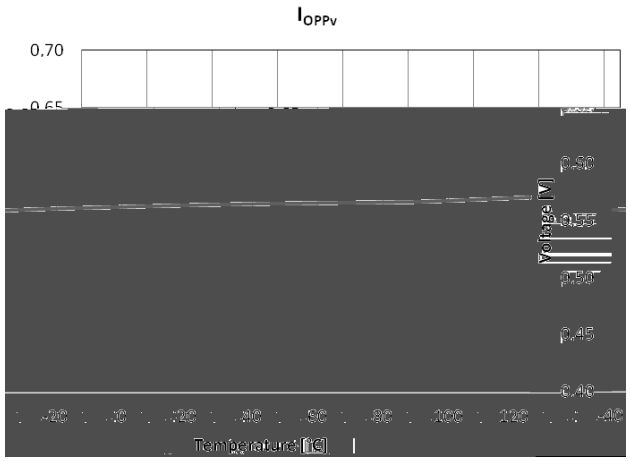

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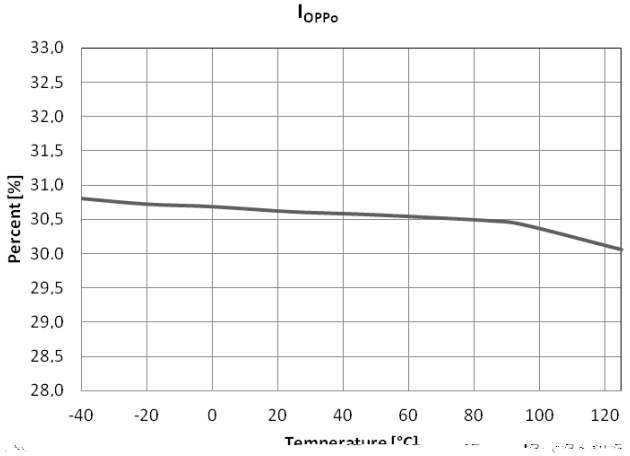

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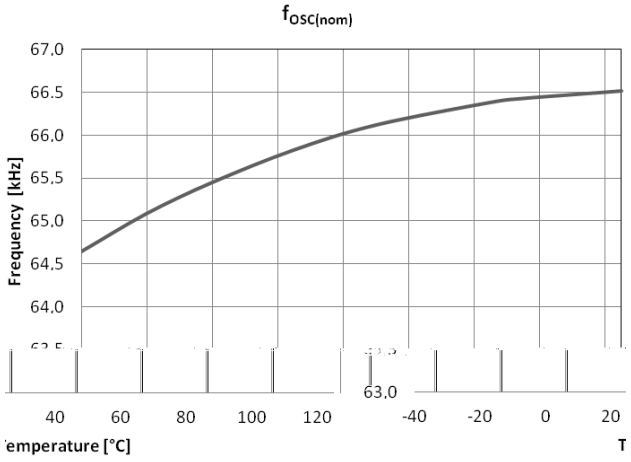

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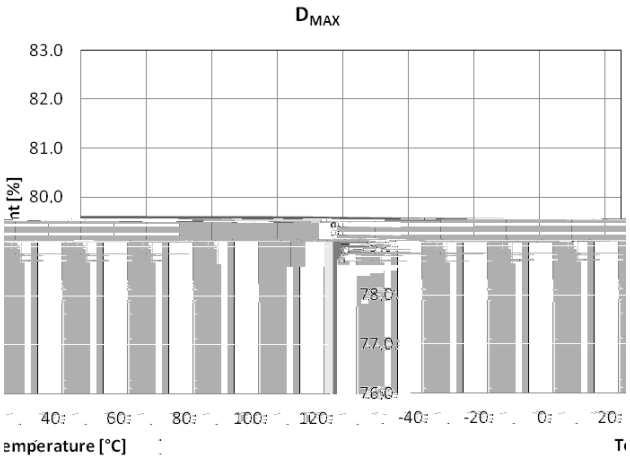

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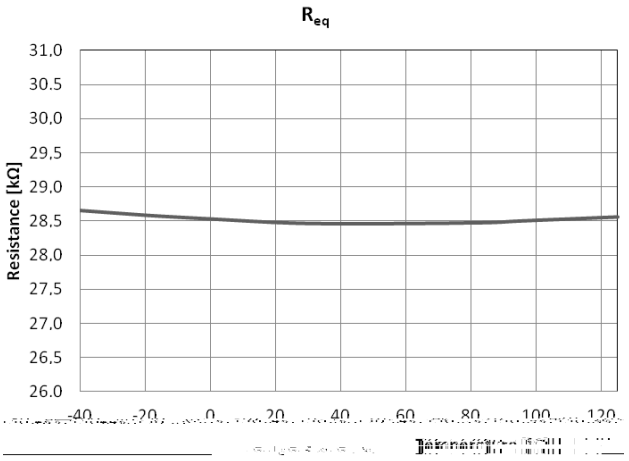

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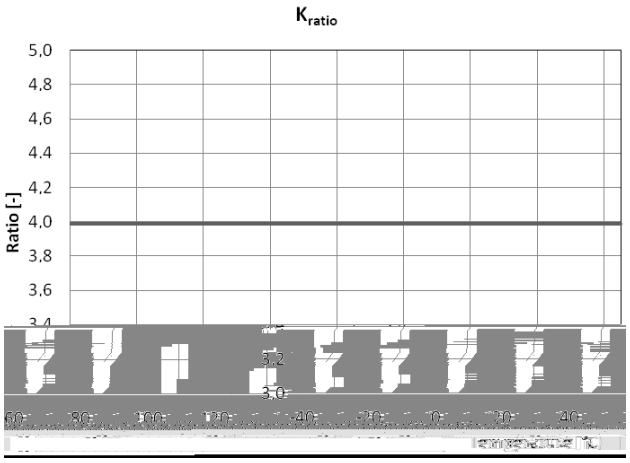

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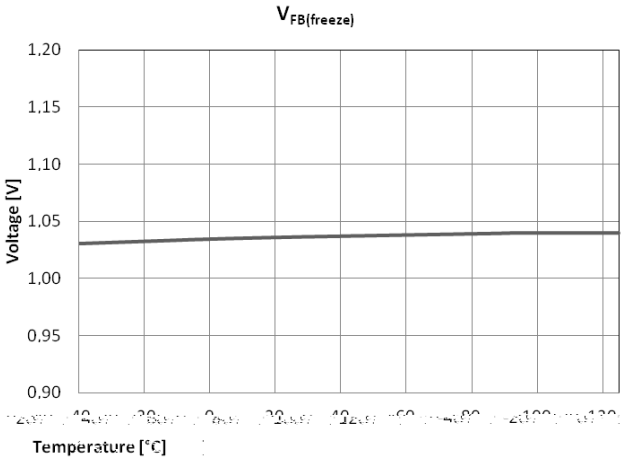

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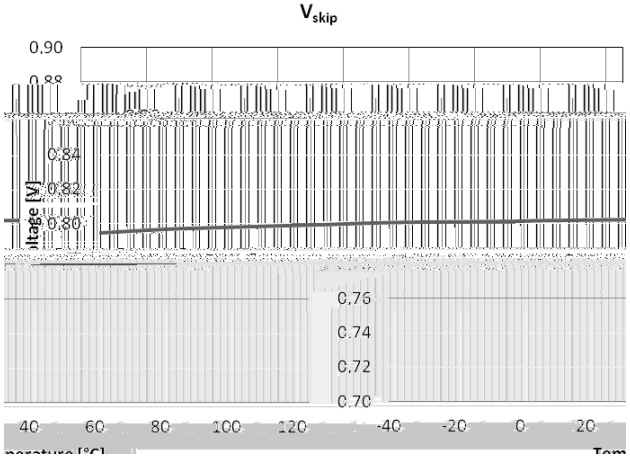

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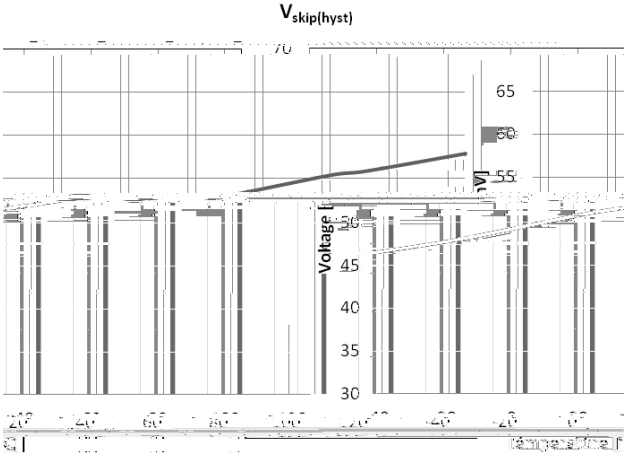

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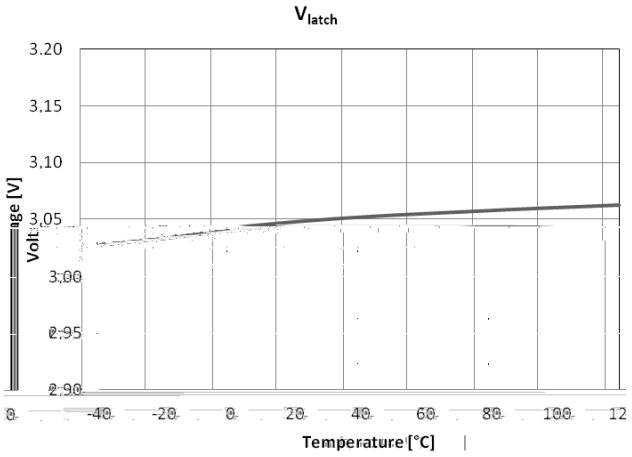

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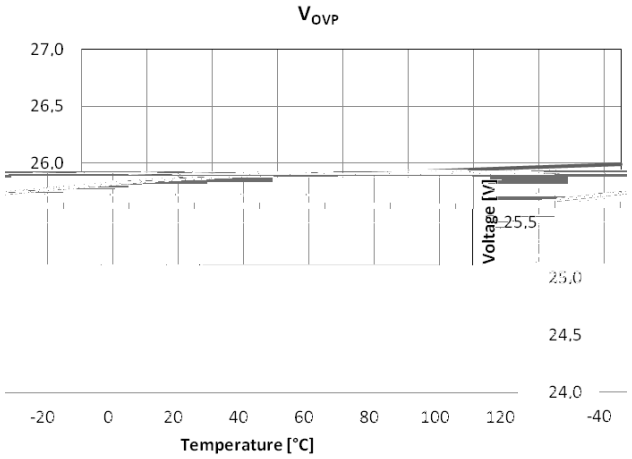

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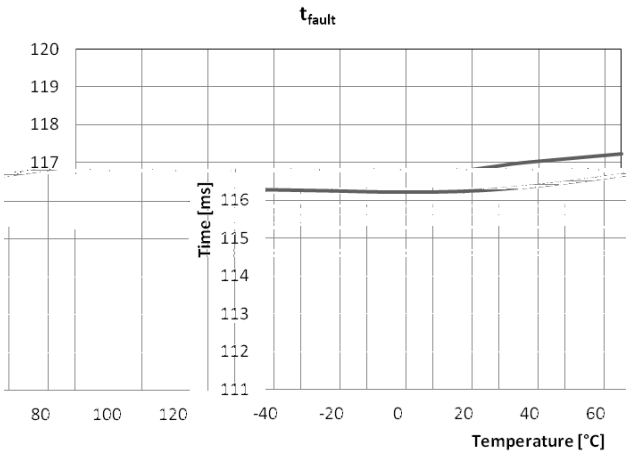

Figure 37.

APPLICATION INFORMATION

Introduction

NCL30073 implements a standard current mode architecture where the switch−off event is dictated by the peak current set point. This component represents the ideal candidate for LED applications. The NCL30073 packs all the necessary components normally needed in today modern LED converter designs, bringing several enhancements such as a non−dissipative OPP, OVP/OTP implementation, short−circuit protection, improved consumption, robustness and ESD capabilities.

- Current−mode Operation with Internal Slope Compensation:
  Implementing peak current mode control at a 65 kHz switching frequency, the NCL30073 offers an internal slope compensation signal that can easily by summed up to the sensed current. Sub harmonic oscillations can thus be fought via the inclusion of a simple resistor in series with the current−sense information.
- Internal OPP:
  By routing a portion of the negative voltage present during the on−time on the auxiliary winding to the dedicated OPP pin (pin 1), the user has a simple and non−dissipative means to alter the maximum peak current set point as the bulk voltage increases. If the pin is grounded, no OPP compensation occurs. If the pin receives a negative voltage, then a peak current is reduced down.
- Low Startup and Standby Current:
  Reaching a low no−load standby power always represents a difficult exercise when the controller draws a significant amount of current during startup.
- Skip Capability:
  A continuous flow of pulses is not desired in all application. The controller monitors FB pin voltage and

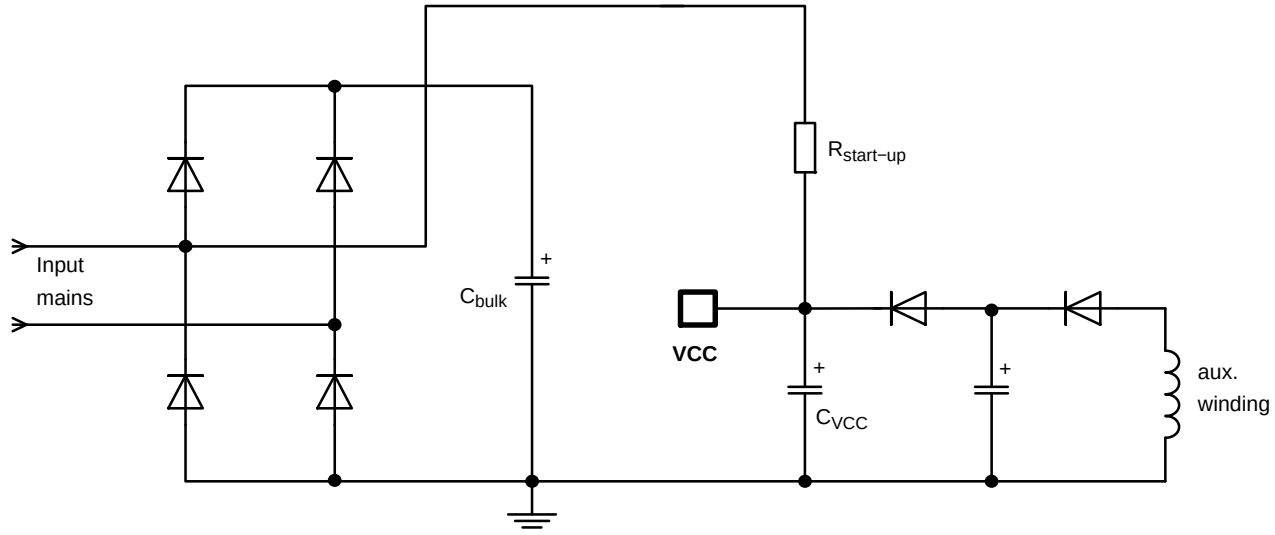

Figure 38. The Startup Resistor can be Connected to the Input Mains for further Power Dissipation Reduction

The first step starts with the calculation of the needed VCC capacitor which will supply the controller which it operates until the auxiliary winding takes it over. Experience shows that this time t_1 can be between 5 and 20 ms. If we consider we need at least an energy reservoir for a t_1 time of 10 ms, the VCC capacitor must be larger than:

$$C_{VCC} \geq \frac{I_{CC} \cdot t_1}{V_{CC(on)} - V_{CC(min)}} \geq \frac{1.6m \cdot 10m}{18 - 8.9} \geq 1.7\ \mu F \quad \text{(eq. 1)}$$

Let us select a 2.2 μF capacitor at first and experiments in the laboratory will let us know if we were too optimistic for the time t_1. The VCC capacitor being known, we can now evaluate the charging current we need to bring the V_{CC} voltage from 0 V to the $V_{CC(on)}$ of the IC. This current has to be selected to ensure a start−up at the lowest mains (85 V_{rms}) to be less than 200 ms (acceptable time):

$$I_{charge} \geq \frac{V_{CC(on)} \cdot C_{VCC}}{t_{start-up}} \geq \frac{18 \cdot 2.2\ \mu}{0.1} \geq 198\ \mu A \quad \text{(eq. 2)}$$

If we account for the 10 μA (maximum) that will flow to the controller, then the total charging current delivered by the start−up resistor must be 208 μA. If we connect the start−up network to the mains (half−wave connection then), we know that the average current flowing into this start−up resistor will be the smallest when V_{CC} reaches the $V_{CC(on)}$ of the controller:

$$I_{CVCC,min} = \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - V_{CC(on)}}{R_{start-up}} \quad \text{(eq. 3)}$$

To make sure this current is always greater than 346 μA, then, the minimum value for $R_{start-up}$ can be extracted:

$$R_{start-up} \leq \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - V_{CC(on)}}{I_{CVCC(min)}} \leq \frac{\frac{85\sqrt{2}}{\pi} - 18}{208\ \mu} \leq 97\ k\Omega \quad \text{(eq. 4)}$$

This calculation is purely theoretical, considering a constant charging current. In reality, the take over time can be shorter (or longer!) and it can lead to a reduction of the VCC capacitor. Thus, a decrease in charging current and an increase of the start−up resistor can be experimentally tested, for the benefit of standby power. Laboratory experiments on the prototype are thus mandatory to fine tune the converter. If we chose the 92 kΩ resistor as suggested by Eq.4 , the dissipated power at high line amounts to:

$$P_{R_{start-up,max}} \approx \frac{V_{ac,peak}^{\ 2}}{4 \cdot R_{start-up}} \approx \frac{(230 \cdot \sqrt{2})^2}{4 \cdot 92k} \approx 287\ mW \quad \text{(eq. 5)}$$

Now that the first VCC capacitor has been selected, we must ensure that the self−supply does not disappear when in no−load conditions. In this mode, the skip−cycle can be so deep that refreshing pulses are likely to be widely spaced, inducing a large ripple on the VCC capacitor. If this ripple is too large, chances exist to touch the $V_{CC(min)}$ and reset the controller into a new start−up sequence. A solution is to grow this capacitor but it will obviously be detrimental to the start−up time. The option offered in Figure 38 elegantly solves this potential issue by adding an extra capacitor on the auxiliary winding. However, this component is separated from the VCC pin via a simple diode. You therefore have the ability to grow this capacitor as you need to ensure the self−supply of the controller without affecting the start−up time and standby power.

Internal Over Power Protection

There are several known ways to implement Over Power Protection (OPP), all suffering from particular problems. These problems range from the added consumption burden on the converter or the skip−cycle disturbance brought by the current−sense offset. A way to reduce the power capability at high line is to capitalize on the negative voltage

swing present on the auxiliary diode anode. During the turn−on time, this point dips to $-N_2 V_{bulk}$, where N_2 being the turns ratio between the primary winding and the auxiliary winding. The negative plateau observed on Figure 39 will have amplitude depending on the input voltage. The idea implemented in this chip is to sum a portion of this negative swing with the internal voltage reference V_{limit} = 0.8 V. For instance, if the voltage swings down to −150 mV during the on−time, then the internal peak current set point will be fixed to the value 0.8 V – 0.150 V = 650 mV. The adopted principle appears in Figure 40 and shows how the final peak current set point is constructed.

Let's assume we need to reduce the peak current from 2.5 A at low line, to 2 A at high line. This corresponds to a 20% reduction or a set point voltage of 640 mV. To reach this level, then the negative voltage developed on the OPP pin must reach:

$$V_{OPP} = 0.8 \cdot V_{limit} - V_{limit} = 0.64 - 0.8 = -160\ mV \quad \text{(eq. 6)}$$

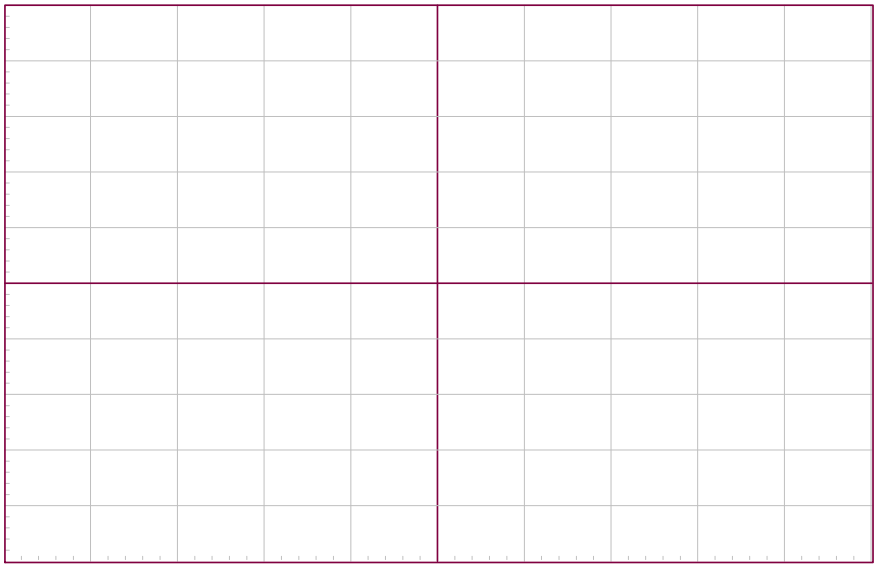

Figure 39. The Signal Obtained on the Auxiliary Winding Swings Negative During the On−time

The OPP pin is surrounded by Zener diodes stacked to protect the pin against ESD pulses. These diodes accept

Slope Compensation

The NCL30073 includes an internal slope compensation signal. This is the buffered oscillator clock delivered during the on−time only. Its amplitude is around 2.5 V at the maximum duty ratio. Slope compensation is a known means used to cure sub harmonic oscillations in CCM−operated current−mode converters. These oscillations take place at half the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty ratio greater than 50%. To lower the current loop gain, one usually injects between 50 and 100% of the primary inductance downslope. Figure 42 depicts how the ramp is generated internally. Please note that the ramp signal will be disconnected from the CS pin during the off−time.

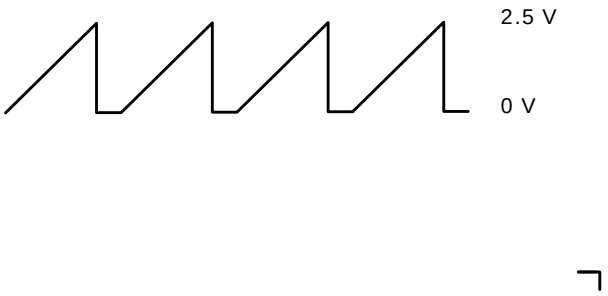

Figure 42. Inserting a Resistor in Series with the Current Sense Information Brings Slope Compensation and Stabilizes the Converter in CCM Operation

Protection Pin

The OPP pin not only allows a reduction of the peak current set point in relationship to the line voltage, it also offers a means to enter the auto−recovery mode.

The auto−recovery detection is made by observing the OPP pin by a comparator featuring a V_{latch} reference voltage. However, for noise reasons and in particular to avoid the leakage inductance contribution at turn off, a blanking delay $t_{latch-blank}$

First, calculate the OPP network with the above equations. Then, suppose we want to trigger auto−recovery of our controller when V_{out} exceeds 25 V. On the auxiliary winding, the plateau reflects the output voltage by the turns ratio between the power and the auxiliary winding. In case of voltage runaway for 19 V output, the plateau will go up to:

$$V_{aux,OVP} = V_{out} \cdot \frac{N_s}{N_{aux}} = 25 \cdot \frac{0.18}{0.25} = 18\ V \quad \text{(eq. 12)}$$

Since our OVP comparator trips at level V_{latch} = 3 V, across the 1 kΩ selected OPP pull−down resistor, it implies a 3 mA current. From 3 V to go up to 18 V, we need an additional 15 V. Under 3 mA and neglecting the series diode forward drop, it requires a series resistor of:

$$R_{OVP} = V_{out} \cdot \frac{V_{aux,OVP} - V_{latch}}{\frac{V_{OVP}}{R_{OPPL}}} = \frac{18 - 3}{\frac{3}{1k}} = 5\ k\Omega \quad \text{(eq. 13)}$$

In nominal conditions, the plateau establishes to around 14 V. Given the divide by 6 ratio, the OPP pin will swing to 14/6 = 2.3 V during normal conditions, leaving 700 mV for the noise immunity. A 100 pF capacitor can be added to improve it and avoid erratic trips in presence of external surges. Do not increase this capacitor too much otherwise the OPP signal will be affected by the integrating time constant.

Over Temperature Protection

In a lot of designs, the converter must be protected against thermal runaways, e.g. when the temperature inside the converter box increases a certain value. Figure 46 shows how to implement a simple OTP using an external NTC and

Combining OVP and OTP

The OTP and Zener−based OVP can be combined together as illustrated by Figure 47. In nominal V_{CC}/output conditions, when the Zener is not activated, the NTC can drive the OPP pin and trigger the protection in case of a fault. On the contrary, in nominal temperature conditions, if the loop is broken, the voltage runaway will be detected and acknowledged by the controller.

In case the OPP pin is not used for either OPP or OVP, it can simply be grounded.

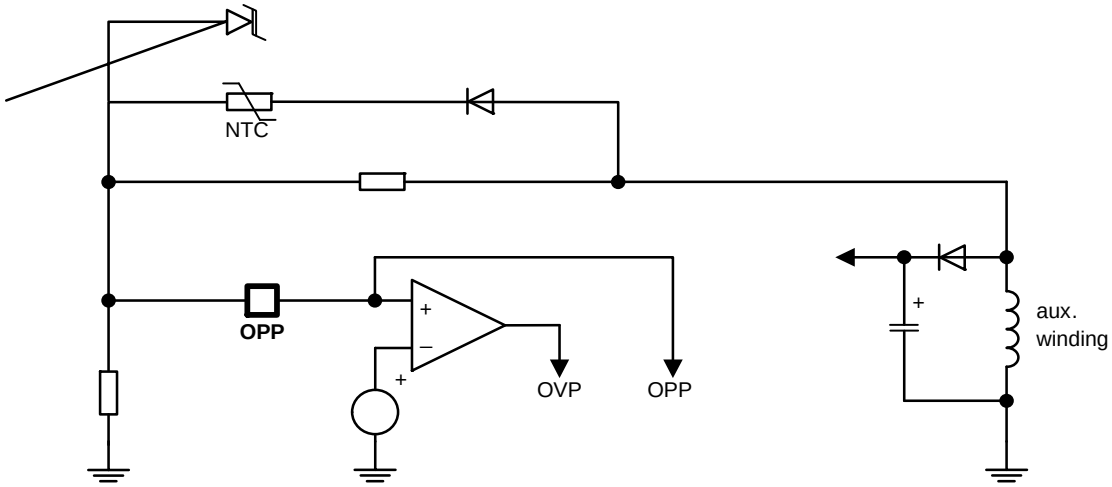

Figure 47. With the NTC Back in Place, the Circuit Nicely Combines OVP, OTP and OPP on the Same Pin

TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024

NOTES:
1. DIMENSIONING AND TOLERAN

TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024

GENERIC
MARKING DIAGRAM*

XXX = Specific Device Code
A =Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O