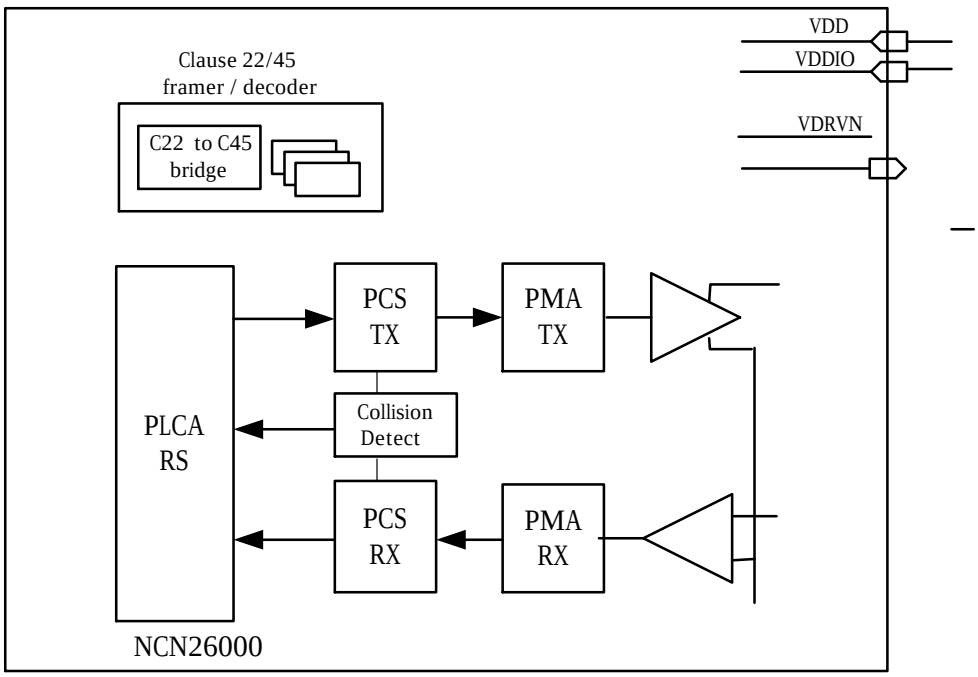
- Data Rate of 10 Mb/s, Half−Duplex
- 3.3V supply
- 5 mm x 5 mm QFN32 Package
- Standard Media Independent Interface (MII). Connects to any


VDD
VDDIO
VDRVN
Clause 22/45
framer / decoder
C22 to C45
bridge
PCS
TX
PMA
TX
PLCA
RS
Collision
Detect
PCS
RX
PMA
RX
NCN26000

12	RSTn	Bi−Directional	8X−Open Drain / Schmitt−	

V_{DD}	Chip Supply	−0.3 to 3.63	V
GND	Ground	−0.3 to 0	V
T_{STG}	Storage Temperature Range	−65 to 150	°C
T_{SLD}	Lead Temperature, Soldering (10 Sec)	260	°C
LINEP	Line Voltage P	−30 to 30	V
LINEN	Line Voltage N	−30 to 30	V
ESD_{HBM}	ESD Capability, Human Body Model (Note 1)	2	kV
ESD_{HBM_LINE}	ESD Capability for LINEP and LINEN Pins, Human Body Model (Note 1)	8	kV
ESD_{CDM}	ESD Capability, Charged Device Model (Note 1)	0.5	kV
LU	Latch−up Current Immunity (Note 1)	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested by the following methods @ T_A = 25 °C:
   ESD Human Body Model tested per JESD22−A114
   ESD Charged Device Model per ESD STM5.3.1
   Latch−up Current tested per JESD78

V_{DD}	Chip Supply	2.97	3.3	3.63	V
V_{DDIO}	I/O Supply for 3.3 V Operation	2.97	3.3	3.63	V
V_{DDIO}	I/O Supply for 2.5 V Operation	2.25	2.5	2.75	V
GND	Ground	−	0	−	V
T_{AMB}	Ambient Operating Temperature	−40	−	125	°C

θ_{JA}	Junction−to−Ambient, Still Air	NCN26000MNTXG	55	K/W

These specifications are over recommended supply voltage and operating free−air temperature unless otherwise noted.

P_{ACTIVE}	Power Consumption (Transmitting and Receiving Ethernet Packets)	VDDIO = VDD = 3.3 V ±10%	−	145	195	mW
$P_{ACTIVERX}$	Receive only Power Consumption (Powered On, but not Transmitting Ethernet Packets)	VDDIO = VDD = 3.3 V ±10%	−	60	−	mW
P_{IDLE}	Idle Power Consumption (Clocked and Enabled, but not Transmitting or Actively Receiving, No Activity on SPI)	VDDIO = VDD = 3.3 V ±10%	−	40	−	mW
F_{XTAL}	XTAL Clock Frequency	VDD = VDDIO = 3.3 V ±10%	−100 ppm	25	+ 100 ppm	MHz
F_{EXT}	External Clock Frequency	VDD = 3.3 V ±10%, VDDIO = 2.5 V ±10%	−100 ppm	25	+100 ppm	MHz
F_{SPI}	SPI Clock Frequency	VDD = VDDIO = 3.3 V ±10%	−	−	25	MHz
		VDD = 3.3 V ±10%, VDDIO = 2.5 V ±10%	−	−	20	
BIT_f	Data Rate (10BASE−T1S)		−	−	10	Mb/s
V_{OUTpp}	Peak Differential Output (Peak−to−peak) (Note 2)	VDD = 3.3 V ±10% TX_GAIN = default	800	1000	1200	mV
J_{TX}	Cycle−to−Cycle Jitter		−	0.2	1	ns
t_{rise}	Rise Time	VDD = 3.3 V ±10%	−	10	−	ns
t_{fall}	Fall Time	VDD = 3.3 V ±10%	−	10	−	ns
R_{OUT}	Output Impedance	VDD = 3.3 V ±10%	40	50	60	Ω
V_{THRX}	Receiver Threshold		−	0	−	mV
V_{EDRX}	Energy Detection Threshold (Note 2)	VDD = 3.3 V ±10% RX_ED				

These specifications are over recommended supply voltage and operating free−air temperature unless otherwise noted.

VIL	LVCMOS Input Level Low	VDDIO = 2.5 V ±10%	−0.3	−	0.7	V
		VDDIO = 3.3 V ±10%	−0.3	−	0.8	V
VIH	LVCMOS Input Level High	VDDIO = 2.5 V ±10%	1.7	−	VDDIO +0.3	V
		VDDIO = 3.3 V ±10%	2.0	−	VDDIO +0.3	V
Vt−(VIL)	Schmitt Trigger Input Level Low	VDDIO = 2.5 V ±10%	0.7	−	1.5	V
		VDDIO = 3.3 V ±10%	0.7	−	1.9	V
Vt+(VIH)	Schmitt Trigger Input Level High	VDDIO = 2.5 V ±10%	0.9	−	1.7	V
		VDDIO = 3.3 V ±10%	0.9	−	2.1	V
Vhyst ($\|V_{t+}-V_{t-}\|$)	Schmitt Trigger Input Hysteresis	VDDIO = 2.5 V ±10%	0.2	−	1.0	V
		VDDIO = 3.3 V ±10%	0.2	−	1.4	V
VOL	Output Level Low	VDDIO = 2.5 V − 10% 4X−Type (Note 3) IOL = 2.48 mA	0	−	0.45	V
		VDDIO = 2.5 V − 10% 8X−Type IOL = 4.83 mA				
		VDDIO = 3.3 V − 10% 4X−Type IOL = 2.93 mA	0	−	0.4	V
		VDDIO = 3.3 V − 10% 8X−Type IOL = 5.65 mA				
VOH	Output Level High	VDDIO = 2.5 V −10% 4X−Type IOH = −2.63 mA	VDDIO − 0.45	−	VDDIO	V
		VDDIO = 2.5 V −10% 8X−Type IOH = −5.11 mA				
		VDDIO = 3.3 V − 10% 4X−Type IOH = 3.19 mA	VDDIO − 0.4	−	VDDIO	V
		VDDIO = 3.3 V − 10% 8X−Type IOH = −6.12 mA				
IIL	Input Current Low	0.0 V ≤ Vin ≤ VDDIO, max				

ype1516803 0 TD-.0007 Tc(VDyN)65.1 Tf6.87488 TD0 T1(VDDIO)Tj.4748-.0019

				(Note 4)
15	Reset	This bit triggers a soft reset of the PHY. 1 = PHY reset 0 = Normal Operation When a soft reset is triggered, all registers revert to their default values and any communication is interrupted. After the soft reset procedure is completed, this bit is automatically reset to 0 (default). The soft reset does not cause the device to enter BOOT state. Therefore, the last strap−pin configuration is preserved, and the device internal initialization will be much faster compared to a hard reset (i.e., driving the nRST pin low).	0	R/W SC
14	Loopback	This bit controls the data loop−back mode of the PHY. 1 = loopback mode enabled 0 = loopback mode disabled When set to 1, all data sent via MII TX is looped backed to MII RX rather than being sent over the line. While loop−back is enabled, the LINEx pins are tri−stated.	0	R/W
13	Speed (LSB)	See Bit 0.6	0	R
12	Link Control	This bit controls the operational status of the PHY. 1 = PHY transmit/receive enabled 0 = PHY transmit/receive disabled NOTE: the implementation of this bit differs from IEEE 802.3 Clause 22.2.4.1.4 (Auto Negotiation Enable). However, it allows the device to be managed by standard software drivers	0	R/W
11	Low−Power	Not implemented. The NCN26000 does not support Low−Power mode.	0	R
10	Isolate	This bit allows entering or leaving the ISOLATED state of the device. 1 = Isolation Enabled 0 = Normal Operation When enabled, all interface pins are set to high−impedance, except for MDC, MDIO, MDINT, DIO0 and DIO1. The default (initial) value of this bit depends on the bootstrap configuration.	−	R/W
9	Link Reset	This bit can be used to reset the TX and RX functions of the PHY. When set to 1, the link is reset, then normal operation resumes.		

				(Note 4)
5	Unidirectional Enable	This function is not available on 10BASE−T1S PHY devices. Therefore, this bit always reads as 0. Additionally, writing to this bit has no effect.	0	R
4:0	−	Not used	0	R

4. Register Type: R = Read, W = Write, SC = Self−Clearing, LH = Latching High

15:12	−	Always reads as 0	0	RO
11	10 Mb/s Half Duplex	Always reads as 1 Indicates that the PHY supports 10 Mb/s Half-Duplex operation.	1	RO
10:8	−	Always reads 0	000	RO
7	Unidirectional Ability	Always reads 0 10BASE−T1S PHY devices do not support unidirectional links	0	RO
6	MF Preamble Suppression	Always reads as 0 The PHY does not accept MDIO frames with suppressed preamble.	0	RO
5	Link Negotiation Complete	1 = link negotiation complete 0 = link negotiation in progress The PHY sets this bit when the PHY Control register bit 12 is set to 1 and bit 9 is set to 0. This bit is further masked by the PLCA status bit when PLCA is enabled. This prevents standard drivers from sending data while PLCA is starting. NOTE: The implementation of this bit is different from IEEE 802.3 Clause 22.2.4.2.10 (Auto negotiation Enable). However, it allows the NCN26000 to be managed by standard software drivers.	−	RO
4	Remote Fault	This bit indicates whether a remote jabber condition was detected since the last read. 1 = remote jabber detected 0 = no remote jabber detected The jabber condition is latched until this field is read or the PHY is reset.	−	R−LH SC
3	Auto−Negotiation Ability	Always reads 1 While auto−negotiation is not supported, this bit is set to 1 to allow the NCN26000 to be managed by standard software drivers.	1	RO
2	Link Status	Although there is not concept of link status for 10BASE−T1S PHY devices, this bit is set after the link control setting. This bit is further masked by the PLCA status bit when PLCA is enabled. This prevents standard drivers from sending data while PLCA is starting. 1 = link is up 0 = link is down NOTE: the implementation of this bit differs from IEEE 802.3 Clause 22.2.4.2.13 (Link Status), because the status is affected by the PLCA−RS status.	−	RO

15:6	Not Used	Not used	0x000	R
5	Physical Collision IRQ Control	1 = MDINT on Physical Collision enabled 0 = MDINT on Physical Collision disabled If enabled, MDINT event is issued every time a physical collision is detected.	0	R/W
4	PLCA Recovery IRQ Control	1 = MDINT on PLCA Recovery enabled 0 = MDINT on PLCA Recovery disabled When enabled, a MDINT event is issued on every PLCA Recovery event. PLCA recovery is flagged when a false carrier event (e.g., impulse noise) occurs on the line. When a CRS event is not followed by the reception of a packet within a certain amount of time the PHY goes into a state depending on its PLCA configuration: When configured as coordinator node, the PHY waits for the line to be quiet for a certain amount of time and then sends a new BEACON. When not configured as a coordinator node, the PHY waits for a BEACON before getting a new transmit opportunity.	0	R/W
3	Remote Jabber IRQ Control	1 = MDINT on Remote Jabber enabled 0 = MDINT on Remote Jabber disabled When enabled, a MDINT event is issued every time the embedded PHY detects a remote jabber condition. A remote jabber condition occurs if a station transmits for longer than maxEnvelopeFrameSize (2000 bytes, including FCS).	0	R/W
2	Local Jabber IRQ Control	1 = MDINT on Local Jabber enabled 0 = MDINT on Local Jabber disabled When enabled, a MDINT event is asserted each time the PHY detects a local jabber condition. A local jabber condition occurs if the TXEN pin is asserted for longer than maxEnvelopeFrameSize (2000 bytes, including FCS).	0	R/W
1	PLCA Status Change IRQ Control	1 = MDINT on change of PLCA Status 0 = no MDINT on change of PLCA Status When enabled, the device issues a MDINT every time the PLCA Status changes. The actual value of PLCA status can be read from the PLCA STATUS REGISTER (MMD 31, Address 51715)	0	R/W
0	Link Status IRQ Control	1 = MDINT on change of Link Status enabled 0 = MDINT on change of Link Status disabled When enabled, a MDINT event is issued every time the link status changes. The actual value of link status can be read from the Link Status bit (1.2) in the PHY Status register (Clause 22, Address 1).	0	R/W

15	Reset IRQ Status	This bit is set at POR or when nRST is asserted. Write 1 to clear. This bit does not generate an interrupt on MDINT and cannot be set once cleared. Its only purpose is to notify the host of a potentially unsolicited reset.	1	R
14:6	Not Used	Not used	0x000	R
5	Physical Collision IRQ Status	When high, this bit indicates that at least one physical collision has been detected since the last read of this register	0	R−LH SC
4	PLCA Recovery IRQ Status	When high, this bit indicates that at least one PLCA recovery event occurred since the last read of this register	0	R−LH SC
3	Remote Jabber IRQ Status	When high, this bit indicates that at least one remote jabber event occurred since the last read of this register	0	R−LH SC
2	Local Jabber IRQ Status	When high, this bit indicates that at least one local jabber event occurred since the last read of this register	0	R−LH SC
1	PLCA Status Change IRQ Status	When high, this bit indicates that the PLCA status bit changed since the last read of this register. The actual value of PLCA status can be read from the PLCA Status Register, PLCASTATUS (MMD 31, Address 51715).	0	R−LH SC
0				

The DIO configuration register controls the function of the General Purpose I/O pins DIO1 and DIO0.

4:1	FN0[3:0]	Selects the function of the DIO0 pin according to the below table:			0x0	R/W
		0x0	Disable	DIOx is set to high−impedance (default)		
		0x1	GPIO (output)	Output value is set after VALx		
		0x2	SFD−TX	Generates a pulse at SFD transmission. VALx sets the pulse polarity.		
		0x3	SFD−RX	Generates a pulse when SFD is detected during RX. VALx sets the pulse polarity. (Note 5)		
		0x4	LED Link Control	Pin drives a LED when port is enabled and link status is up		
		0x5	LED PLCA Status	Pin drives a LED when PLCA status is up		
		0x6	LED TX	LED indicating TX activity		
		0x7	LED RX	LED indicating RX activity. (Note 5)		
		0x8	CLK25M	Output 25 MHz clock		
		0x9 – 0xA	Reserved	Don’t use		
		0xB	SFD− RX&TX	Pulse on DIOx at SFD (RX or TX), VALx sets the polarity of the pulse		
		0xC − 0xE	Reserved	Don’t use		
		0xF	LED TX&RX	LED indicating TX and RX activity		
0	VAL0	Sets the output value of DIO0 when FN0[3:0] is set to GPIO function. It sets the polarity (1 = active high, 0 = active low) for all other modes.			0	R/W

5. Also triggers on TX

The following Clause 45 registers are implemented (reserved registers not shown)

1	5	0005	S	Devices in Package 1
	6	0006		Devices in Package 2
	18	0012		BASE−T1 Extended Ability
	2297	08F9		10BASE−T1S PMA Control
	2298	08FA		10BASE−T1S PMA Status
	2299	08FB		10BASE−T1S Test Mode
3	5	0005		Devices in Package 1
	6	0006		Devices in Package 2
	2291	08F3		10BASE−T1S PCS Control
	2292	08F4		10BASE−T1S PCS Status
	2293	08F5		10BASE−T1S PCS Diagnostic 1
	2294	08F6		10BASE−T1S PCS Diagnostic 2

The following Clause 45 registers are implemented (reserved registers not shown)

30	4096	1000	V	Chip Revision
	4097	1001		PHY Tweaks
	4100	1004		Chip Info
	4101	1005		NVM Health

–

15:13	Test Mode	Test mode in accordance with IEEE802.3cg. The default is “normal operation”	000	R/W
		000 – Normal Operation 001 – Transmitter Output Voltage test 010 – Transmitter Output Droop test 011 – Transmitter PSD mask test 100 – Transmitter high Impedance test 101 – Reserved 110 – Reserved 111 – Reserved		
12:0	reserved	Always reads as 0	0	R

–

15	PCS Reset	1 = PCS reset 0 = normal operation Setting this bit to 1 sets all registers to their default state. Resetting the PCS also causes the PMA and PLCA layers to reset, as if a soft reset was issued.	0	R/W SC
14	Loopback	This bit controls the PCS loopback mode of the PHY. 1 = Loopback enabled 0 = Loopback disabled When enabled, data sent by the MAC through the MII TX is looped back to the MII RX traversing the PCS. This allows testing the MII interface, the 4B/5B encoder/decoder, the TX/RX state machines, and the scrambler/descrambler.	0	R/W
13:0	reserved	Always reads as 0	0	R

–

15:8	–	Always read 0	0	R
7	Fault	1 = Fault condition detected 0 = No fault condition detected If this bit reads as 1, the PCS has latched a jabber fault condition since the last read of this register. This can either be a local or a remote jabber condition.	–	RO−LH
6:0	–	Always read 0	0	R

–

15:0	PCS Remote Jabber Count	Counts the number of detected remote jabber events since this register was last read. For details, see IEEE802.3cg Clause 45.2.3.68e.1. If the count reaches 0xFFFF, no more errors are counted to prevent the counter from overflowing.	0	RO−SC

–

15:0	PCS Physical Collisions Count	Counts the number of physical collision events detected by the PHY since this register was last read. If the count reaches 0xFFFF, no more errors are counted to prevent the counter from overflowing. NOTE: Physical collisions are caused by the superposition of signals transmitted simultaneously by more than one station on the same medium. In contrast to physical collisions, logical collisions in PLCA mode are triggered by the PLCA RS arbitration algorithm.	0	RO−SC

The PHY TWEAKS register allows experienced users to customize the parameters of the analog line driver among other custom parameters. The default values have been carefully selected for optimum performance and do not need modification under typical conditions.

13:10	CD Threshold	Specifies the Collision Detection threshold level. $CD_{Threshold}$ = 150 mV + 50 mV_{pp} * CDL	0xB	R/W

0	150
1	200
2	250
3	300
4	350
5	400
6	450
7	500
8	550
9	600
10	650
11	700 (default)
12	750
13	800
14	850
15	900

NOTE: This is an advanced configuration register. It is recommended to consult with before changing the value from its default settings.

The PHY TWEAKS register allows experienced users to customize the parameters of the analog line driver among other custom parameters. The default values have been carefully selected for optimum performance and do not need modification under typical conditions.

<table>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>9:6</td><td>RX_ED Threshold</td><td colspan="2">Specifies the RX energy detection threshold level following this equation
$RX_{ED\ Threshold}$ = 150 mV + 50 mV_{pp} * RX_ED</td><td>2</td><td>R/W</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>0</td><td>150</td><td></td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>200</td><td></td><td></td></tr>
<tr><td></td><td></td><td>2</td><td>250 (default)</td><td></td><td></td></tr>
<tr><td></td><td></td><td>3</td><td>300</td><td></td><td></td></tr>
<tr><td></td><td></td><td>4</td><td>350</td><td></td><td></td></tr>
<tr><td></td><td></td><td>5</td><td>400</td><td></td><td></td></tr>
<tr><td></td><td></td><td>6</td><td>450</td><td></td><td></td></tr>
<tr><td></td><td></td><td>7</td><td>500</td><td></td><td></td></tr>
<tr><td></td><td></td><td>8</td><td>550</td><td></td><td></td></tr>
<tr><td></td><td></td><td>9</td><td>600</td><td></td><td></td></tr>
<tr><td></td><td></td><td>10</td><td>650</td><td></td><td></td></tr>
<tr><td></td><td></td><td>11</td><td>700</td><td></td><td></td></tr>
<tr><td></td><td></td><td>12</td><td>750</td><td></td><td></td></tr>
<tr><td></td><td></td><td>13</td><td>800</td><td></td><td></td></tr>
<tr><td></td><td></td><td>14</td><td>850</td><td></td><td></td></tr>
<tr><td></td><td></td><td>15</td><td>1</td><td></td><td></td></tr>
</table>

The PHY TWEAKS register allows experienced users to customize the parameters of the analog line driver among other custom parameters. The default values have been carefully selected for optimum performance and do not need modification under typical conditions.

Note that the configuration memory cannot be written by the user, so corrupted data cannot be recovered.

The configuration memory is protected by an ECC scheme that allows the automatic correction of a single bit error and the detection of multiple bit errors. With this feature, a single bit error (SBERR) can be considered a warning, while a reported multiple bit error shall be interpreted as an error impairing the function of the part (partially or entirely), depending on the zone in which it appears.

15	Red Zone NVM Warning	When this bit reads as 1, the ECC controller has corrected a single bit error in the red zone. As single bit errors are corrected by the ECC controller, this is just a warning. The NCN26000 remains fully functional.	0	R
14	Red Zone NVM Error	When this bit reads as 1, the ECC controller has detected at least two unrecoverable bit errors in the red zone. This shall be treated as a permanent error, as correct functionality cannot be guaranteed. The part may still be able to operate with degraded performance.	0	R
13	Yellow Zone NVM Warning	When this bit reads as 1, the ECC controller has corrected a single bit error in the yellow zone. The NCN26000 remains fully functional, and a host relying on the information stored in the NVM is not affected.	0	R
12	Yellow Zone NVM Error	When this bit reads as 1, the ECC controller has detected at least two unrecoverable bit errors in the yellow zone. While this is a permanent error invalidating the content of the OUI and the MAC ID, the NCN26000 remains fully functional. However, a host relying on such information may not initialize correctly.	0	R
11	Green Zone NVM warning	When this bit reads as 1, the ECC controller has corrected a single bit error in the green zone of the trim and configuration memory. The NCN26000 remains fully functional.	0	R

The PHY configuration 1 register allows using non−IEEE802.3 compliant operation modes that can help with debugging and increased performance in noisy environments. Note that these setting should be used with care as they might result in a network configuration that prohibits successful communication.

The PHY configuration 1 register allows using non−IEEE802.3 compliant operation modes that can help with debugging and increased performance in noisy environments. Note that these setting should be used with care as they might result in a network configuration that prohibits successful communication.

1	No Collision Masking	This bit controls whether the PHY shall ignore physical collision events on the line when PLCA and ENI modes are both enabled. 1 = ENI collision detection masking disabled 0 = ENI collision detection masking enabled If set, this bit prevents masking of collision detection when Enhanced Noise Immunity (ENI) mode and PLCA are enabled. Note that even if collisions are masked, the PCS Diagnostic Register 2 still counts detected corruptions of the transmitted signal for diagnostic/debug purposes.	1	R/W
0	RX Delayed	This bit configures the internal path delay length when receiving frames. 1 = delayed reception enabled 0 = delayed reception disabled		

1	Coordinator Mode	This bit controls whether the PLCA coordinator node is allowed to take non−zero IDs. 1 = Coordinator Mode enabled 0 = Coordinator Mode disabled When enabled, the NCN26000 coordinator role is determined by the ‘Coordinator Role’ bit setting in this register. When disabled, the NCN26000 is assigned the coordinator role if its PLCA ID is set to 0 in the PLCA CONTROL 1 Register (as per IEEE 802.3cg specifications)	0	R/W
0	Coordinator Role	1 = node is the PLCA coordinator 0 = node is a PLCA follower When the ‘Coordinator Mode’ bit in this register is set to 1, the PLCA RS takes the coordinator role based only on the setting of this bit.	0	R/W

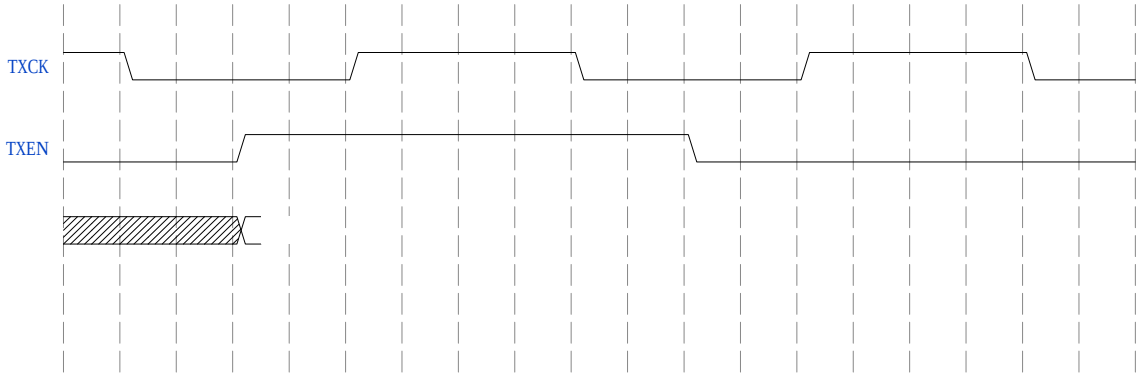
This register allows fine tuning of the NCN26000 line receiver when ENI mode is enabled.
WARNING: changing the setting from their default should only be considered by experienced users at their own risk. Invalid setting may lead to unexpected link down and dropped or corrupted Ethernet frames.

15:14	Not used	−		0x0	R
13:8	PLCA Beacon Detection Threshold	This field selects the threshold level for the PLCA Beacon (NN*) detection in the PMA when ENI mode is enabled. Higher values reduce the chance of false detection (false positive) but reduces the noise tolerance. Lower values achieve the opposite effect.		0x20	R/W
7:3	Not used	−		0x0	R
2:0	Drift Compensation Window Selection				R
		1	r e s e r v e d		
		2	31 bit times		
		7	r e s e r v e d		

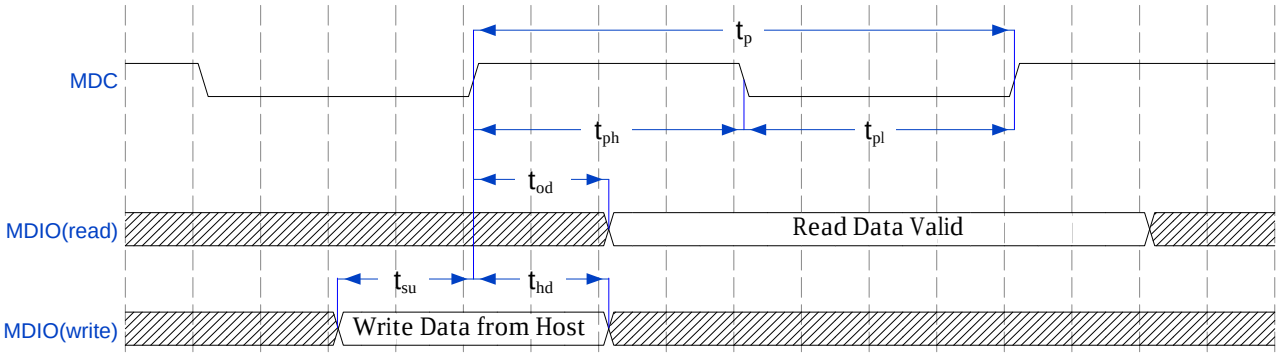
This register allows fine tuning of the NCN26000 line receiver when ENI is enabled.
Warning: changing the setting from their default should only be considered by experienced users at their own risk. Invalid setting may lead to unexpected link down and dropped or corrupted Ethernet frames.

15:14	Not used	−	0x0	R
13:8	Packet Preamble Detection Threshold	Sets the threshold level for the packet preamble (JJHH) detection in the PMA RX when ENI mode is enabled. Higher values reduce the chance of false detection (false positive) but reduce the noise tolerance. Lower values achieve the opposite effect.	0x35	R/W
7:6	Not used	−	0x0	R
5:0	Commit Detection Threshold	Sets the threshold for the Commit (JJ*) detection of the PMA RX when ENI mode is enabled. Higher values reduce the chance of false detection (false positive) but reduce the noise tolerance. Lower values achieve the opposite effect.	0x20	R/W

15	Beacon TX / RX Status			


TXCK
TXEN

t_p	RXCK period	399.96	400	400.04	ns
t_{ph}	RXCK high pulse width	–	200	–	ns
t_{pl}	RXCK low pulse width	–	200	–	ns
t_{od}	RXD, RXER, RXDV output delay from rising edge of RXCK	182	–	250	ns
t_{lat}	CRS to RXD, RXER, RXDV latency	–	6.4	–	µs



t_p	MDC clock period	400	–	–	ns
t_{ph}	MDC high pulse width	–	200	–	ns
t_{pl}	MDC low pulse width	–	200	–	ns
t_{od}	MDIO (PHY output) delay from rising edge of MCD	–	222	–	ns
t_{su}	MDIO (PHY input) setup time to rising edge of MDC	10	–	–	ns
t_{hd}	MDIO (PHY input) hold time from rising edge of MDC	4	–	–	ns

CMC	Common mode choke (e.g. Murata DLW43MH201XK2L or TDK ACT1210E−241−2P−TL−000)	200	μH	

1. Issue a device reset by setting bit 15 in the Control register (Address 0)
2. If NCN26000 was booted in ISOLATE mode, set bit 10 to 0 to have the device enter NORMAL mode.
3. Enable the link by setting bit 13 of the same register

To connect the NCN26000 device to a 10BASE−T1S multi−drop network in PLCA mode of operation, the following configuration is required:

1. Assign the node a unique PLCA ID in the range of 0 to 254, with 0 being the coordinator. This can be achieved by writing register PLCA Control 1 Register (MMD 31, Address 51714)
2. If the node is the coordinator, set the maximum number of allowed transmit opportunities. i.e., the maximum number of nodes allowed to share the media (Note 2). This can be achieved by writing register PLCA Control 1 Register (MMD 31, Address 51714)
3. Configure the TO_TIMER to the value chosen for the network (typically, 24 or 32) (Note 3). This can be achieved by writing register PLCA Transmit Opportunity Timer Register (MMD 31, Address

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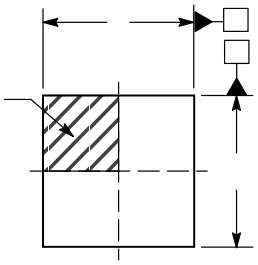

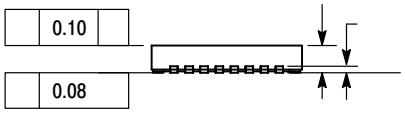

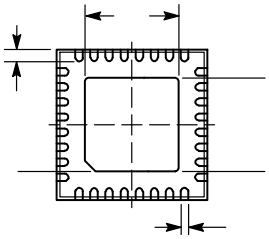

XXXXXXXX
XXXXXXXX
AWLYYWW▪
▪

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb Free Package