10 b/

+ 0 0

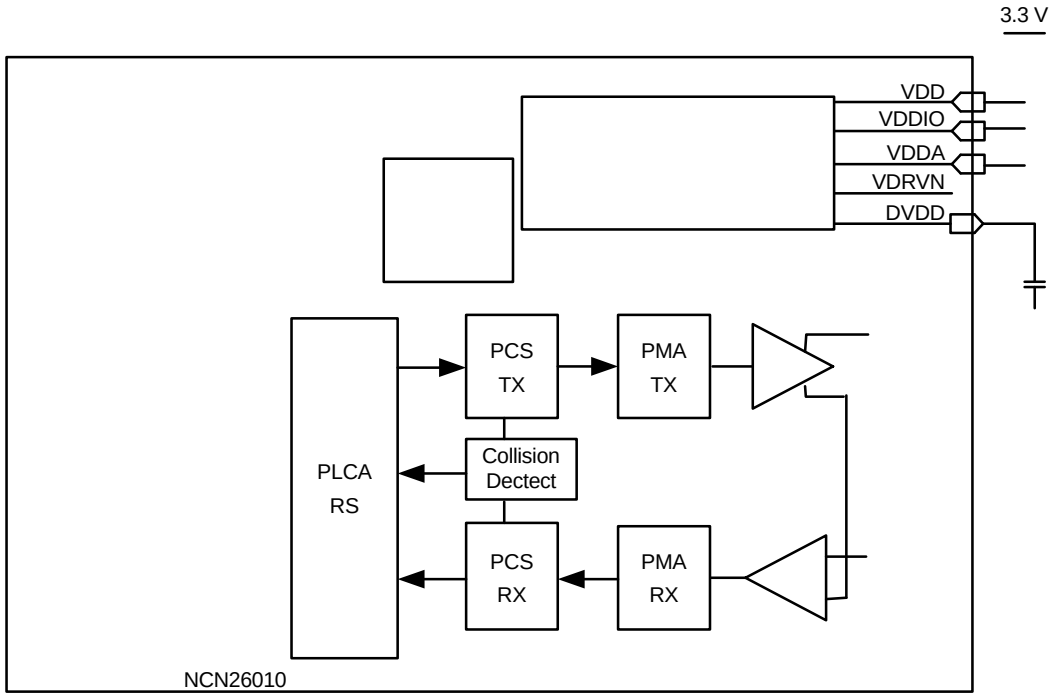
–

2 010

The NCN26010 device is an IEEE 802.3cg compliant Ethernet Transceiver including a Media Access Controller (MAC), a PLCA Reconciliation Sublayer (RS) and a 10BASE T1S PHY designed for industrial multi drop Ethernet. It provides all physical layer functions needed to transmit and receive data over a single unshielded twisted pair. NCN26010 communicates to host MCUs via the Open Alliance MACPHY SPI protocol.

- 10BASE T1S – IEEE 802.3cg Compliant
- 3.3 V Supply Voltage
- Two Configurable Digital Outputs that can Drive Low Current LEDs
- Low Profile 4 mm x 4 mm QFN 32
- Integrated MAC and 10BASE T1S PHY
- Open Alliance Compatible SPI Interface for Exchanging

Publication Order Number:



NOTE: Internal power distribution and GND lines from Power Supply block are not shown.

31	GND	Ground	GND	Ground
32	NC			Reserved, do not connect in the application
EP	GND	Ground	GND	Exposed Pad

VDD	Chip Supply	−0.3 to 3.63	V
GND	Ground	−0.3 to 0	V
T_{STG}	Storage Temperature Range	−65 to 150	°C
T_{SLD}	Lead Temperature, Soldering (10 Sec.)	260	°C
LINEP	Line Voltage P	−30 to 30	V
LINEN	Line Voltage N	−30 to 30	V
ESD_{HBM}	ESD Capability, Human Body Model (Note 1)	2	kV
ESD_{HBM_LINE}	ESD Capability for LINEP and LINEN Pins, Human Body Model (Note 1)	8	kV
ESD_{CDM}	ESD Capability, Charged Device Model (Note 1)	0.5	kV
LU	Latch−up Current Immunity (Note 1)	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested using the following methods @ T_A = 25°C:
   ESD Human Body Model per JESD22−A114
   ESD Charged Device Model per ESD STM5.3.1

(These specifications are over recommended supply voltage and operating free−air temperature unless otherwise noted.)

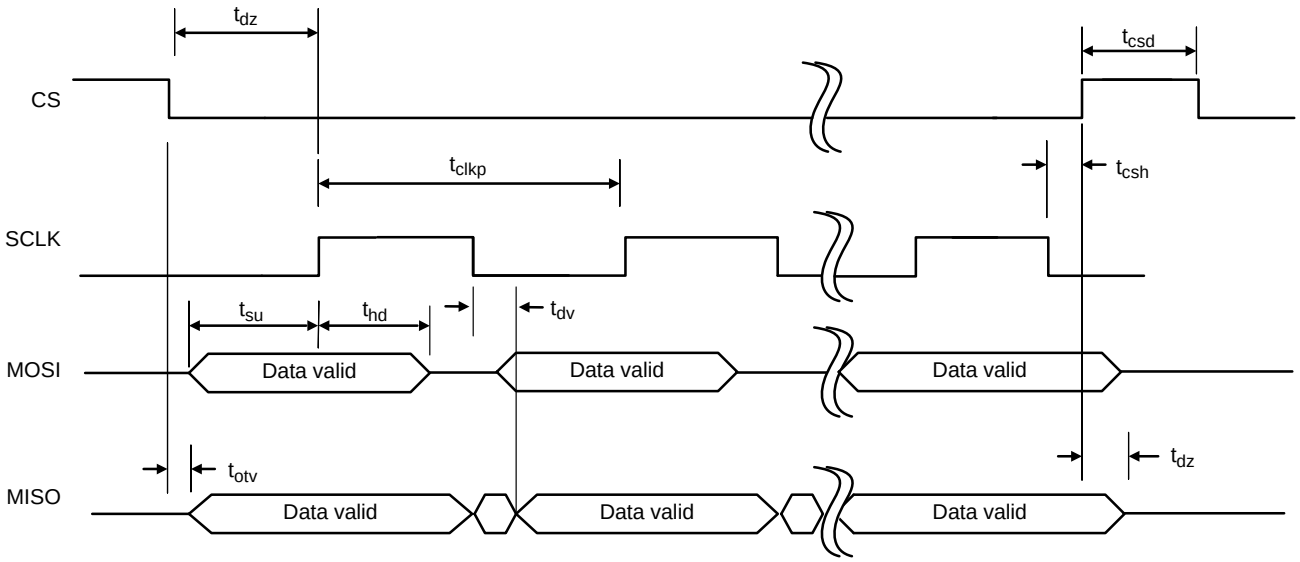
P_{ACTIVE}	Power Consumption (Transmitting and Receiving Ethernet Packets)	VDDIO = VDD = 3.3 V ±10%	−	150	215	mW
$P_{ACTIVERX}$	Receive only Power Consumption (Powered On, but not Transmitting Ethernet Packets)	VDDIO = VDD = 3.3 V ±10%	−	75	−	mW
P_{IDLE}	Idle Power Consumption (Clocked and Enabled, but not Transmitting or Actively Receiving, No Activity on SPI)	VDDIO = VDD = 3.3 V ±10%	−	55	−	mW

(These specifications are over recommended supply voltage and operating free−air temperature unless otherwise noted.) (continued)

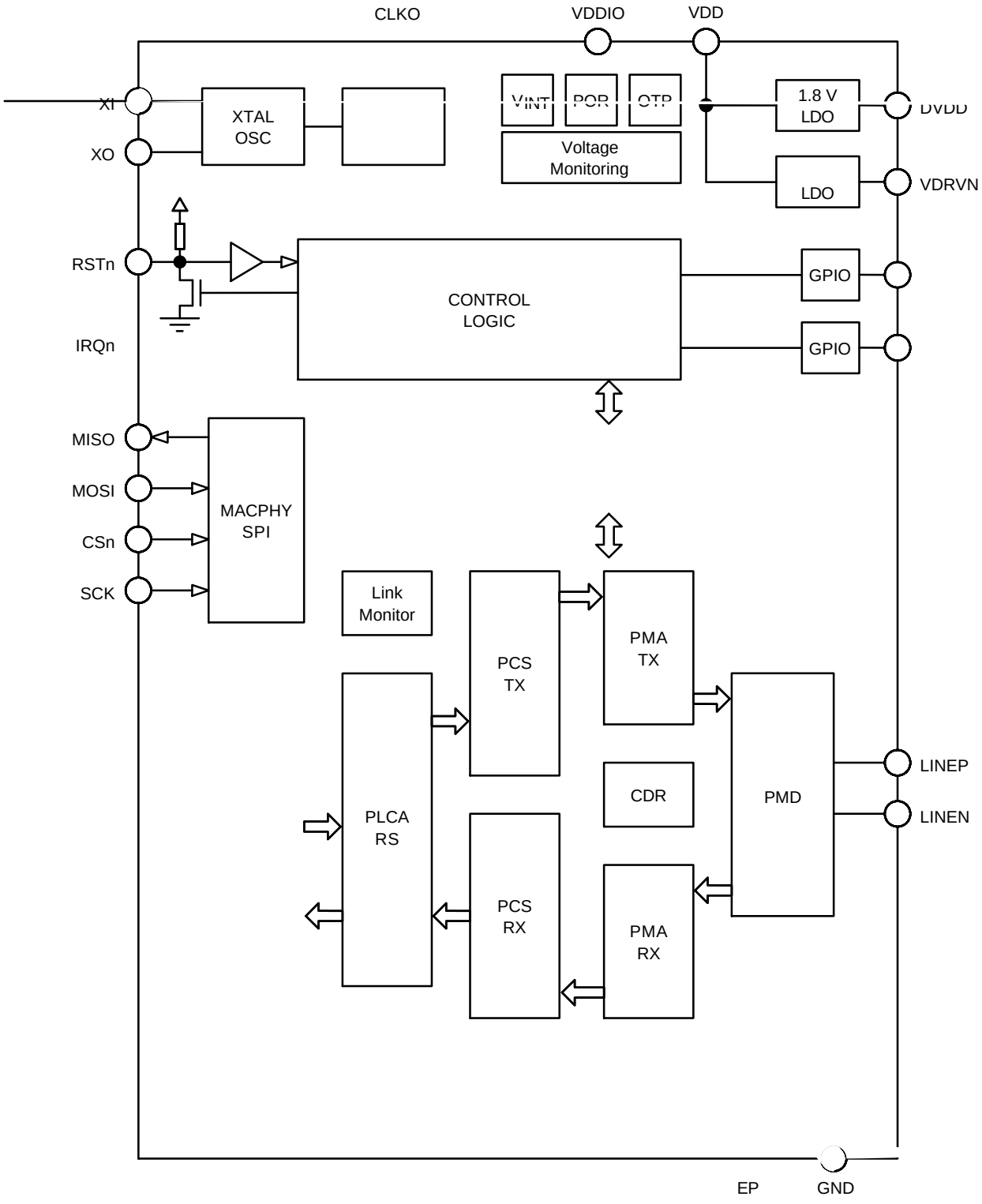
V_{hyst} ($\|V_{t+}-V_{t-}\|$)	Schmitt Trigger Input Hysteresis	VDDIO = 2.5 V ±10%	0.2	−	1.0	V
		VDDIO = 3.3 V ±10%	0.2	−	1.4	V
V_{OL}	Output Level Low	VDDIO = 2.5 V − 10% 4X−Type (Note 3) IOL = 2.48 mA	0	−	0.45	V
		VDDIO = 2.5 V − 10% 8X−Type IOL = 4.83 mA				
		VDDIO = 3.3 V − 10% 4X−Type IOL = 2.93 mA	0	−	0.4	V
		VDDIO = 3.3 V − 10% 8X−Type IOL = 5.65 mA				
V_{OH}	Output Level High	VDDIO = 2.5 V −10% 4X−Type IOH = −2.63 mA	VDDIO − 0.45	−	VDDIO	V
		VDDIO = 2.5 V −10% 8X−Type IOH = −5.11 mA				
		VDDIO = 3.3 V − 10% 4X−Type IOH = 3.19 mA	VDDIO – 0.4	−	VDDIO	V
		VDDIO = 3.3 V − 10% 8X−Type IOH = −6.12 mA				
I_{IL}	Input Current Low	0.0 V ≤ Vin ≤ VDDIO, max supply = 3.63 V	−11	−	11	μA
I_{IH}	Input Current High	0.0 V ≤ Vin ≤ VDDIO, max supply = 3.63 V	−11	−	11	μA
R_{PU}	Pull−Up Resistance		33	54	103	kΩ
R_{PD}	Pull−Down Resistance		30	44	73	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Default Value, can be altered by device configuration.
3. 4X and 8X denote the number of std LVCMOS input loads the buffer is designed to drive.



t_{clkp}	SPI Clock Period	VDDIO = 2.25 V − 3.63 V	40	−	−	ns
t_{su}	Data Input Setup Time	VDDIO = 2.25 V − 3.63 V	8	−	−	ns
t_{hd}	Data Input Hold Time	VDDIO = 2.25 V − 3.63 V	5	−	−	ns
t_{dv}	Output Data Valid	VDDIO = 3.3 V ±10%	−	−	12	ns
		VDDIO = 2.5 V ±10%	−	−	14.5	
t_{otv}	CS Low to MISO Out Valid	VDDIO = 3.3 V ±10%	−	−	12	ns
		VDDIO = 2.5 V ±10%	−	−	14.5	
t_{fc}	CS Low to Rising Edge of SCLK	VDDIO = 2.25 V − 3.63 V	20	−	−	ns
t_{csh}	SCLK Falling to CS De−assert	VDDIO = 2.25 V − 3.63 V	5	−	−	ns
		VDDIO = 2.5 V ±10%	5	−	14.5	
t_{dz}	CS De−assert to MISO HIGH−Z	VDDIO = 3.3 V ±10%	−	−	12	ns
		VDDIO = 2.5 V ±10%	−	−	14.5	


CLKO
VDDIO
VDD
XI
XO
XTAL
OSC
VINT
POR
OTP
Voltage
Monitoring
1.8 V
LDO
DVDD
LDO
VDRVN
RSTn
IRQn
CONTROL
LOGIC
GPIO
GPIO
MISO
MOSI
CSn
SCK
MACPHY
SPI
Link
Monitor
PCS
TX
PMA
TX
PLCA
RS
CDR
PMD
LINEP
LINEN
PCS
RX
PMA
RX
EP
GND

The NCN26010 provides the registers in memory map selection groups. See the below table for details.

0	32	Standard SPI Control and Status, PHY MIIM (Clause 22)
1	32	MAC registers
2	16	PHY− PCS Registers (IEEE802.3 MMD3)

(continued)

			7:0								
1	0x0024	ADDRMASK2L	31:24	ADDRMASK2[31:0]							
			23:16								
			15:8								
			7:0								
	0x0025	ADDRMASK2H	31:24								
			23:16								
			15:8	ADDRMASK2[47:32]							
			7:0								
	0x0026	ADDRMASK3L	31:24	ADDRMASK3[31:0]							
			23:16								
			15:8								
			7:0								
	0x0027	ADDRMASK3H	31:24								
			23:16								

1	0x0038	STFRAMESTX25		STFRAMESTX256[31:0]							
	0x0039	STFRAMESTX51		STFRAMESTX512[31:0]							
	0x003A	STFRAMESTX10		STFRAMESTX1024[31:0]							
	0x003B	STUNDERFLOW								STUNDERFLOW[9:8]	
				STUNDERFLOW[7:0]							
	0x003C	STSINGLECOL								STSINGLECOL[17:16]	
				STSINGLECOL[15:10]							
	0x003D	STMULTICOL								STMULTICOL[17:16]	
				STMULTICOL[15:10]							
	0x003E	STEXCESSCOL								STMULTICOL[9:8]	
				STMULTICOL[7:0]							
	0x003F	STDEFERREDT								STDEFERREDTX[17:16]	
				STDEFERREDTX[15:10]							
	0x0040	STCRSERR								STCRSERR[9:8]	
				STCRSERR[7:0]							
	0x0041	STOCTETSRXL		STOCTETSRX[31:0]							
	0x0042	STOCTETSRXH									
			15:8	STOCTETSRX[47:32]							
			7:0								
	0x0043	STFRAMESRXOK	31:24	STFRAMESRXOK[31:0]							
			23:16								
			15:8								
			7:0								
	0x0044	STBCASTRXOK	31:24	STBCASTRXOK[31:0]							
			23:16								

(continued)

4			7:0								
	0xCA02	PLCACTRL1	15:8	PLCANCNT							
			7:0	PLCAID							
	0xCA03	PLCASTS	15:8	PST							
			7:0								
	0xCA04	PLCATOTMR	15:8								
			7:0	TOTMR							
	0xCA05	PLCABURST	15:8	MAXBC							

31:8	Reserved			

31:16	N/A	Bits contain no valid data	0x0000	RO
15	SYNC	Configuration Synchronization When set to 0, the NCN26010 does not accept TX or RX frames, as its configuration may not be complete. Once the host completes configuration of the NCN26010, it should set this bit to 1. Once set, the bit can only be cleared by a system reset.	0	RW−1
14	TXFCSVE	Transmit Frame CheckSequence Validation Enable. When set, the final 4 octets of all Ethernet frames conveyed via SPI are validated as an Ethernet FCS. When using this option, the FCSA bit in the MACCTRL0 shall be cleared.	0	RW
13	CSARFE	CS Align Receive Frame Enable When set, all received Ethernet frames start at the beginning of the receive chunk following the CSn assertion with a Start Word Offset of zero. When this bit is cleared, received frames may begin anywhere within the chunk payload.	0	RW
12	ZARFE	Zero Align Receive Frame Enable When set, all received Ethernet frames start at the beginning of the received chunk with a Start Word Offset of zero. When this bit is cleared, received frames may begin anywhere within the chunk payload.	0	RW
11:10	TXCTHRESH	Transmit Credit Threshold Configures the minimum number of transmit credits (TXC) that have to be available for asserting IRQn, after TXC went down to zero 00 ≥ 1 credit (the default) 01 ≥ 4 credits 10 ≥ 8 credits 11 ≥ 16 credits	00	RW
9	TXCTE	Transmit cut−through enable When set to one, this bit enables sending frames in cut−through mode to reduce the average TX latency.	0	RW
8	RXCTE	Receive cut−through enable When set to one, this bit enables receiving frames in cut−through mode to reduce the average RX latency.	0	RW
7	FTSE	Frame Timestamp enable This feature is not supported by NCN26010. This bit is read only	0	RO
6	FTSS	Receive Frame Timestamp Select This feature is not supported by NCN26010. This bit is read only	0	RO
5	PROTE	Enable Control Data Read/Write Protection Refer to OPEN Alliance specification section 7.4 for details.	0	RW
4:3	N/A	Not used	00	RO
2:0	CPS	Chunk Payload Size Configuration 0x3 Chunk Payload size is 8 bytes 0x4 Chunk Payload size is 16 bytes 0x5 Chunk Payload size is 32 bytes 0x6 Chunk Payload site is 64 bytes (default)	0x6	RW

31:13	N/A			

31:16	N/A	Not used	0x0000	RO
15	Reset	1 = PHY reset 0 = normal operation When set, a soft reset is initiated. The soft reset does not cause bootstrapping, ignoring changes in strap−pin configuration. All registers revert to their default values and any communication is interrupted. After the soft reset procedure is completed, this bit is automatically reset to 0 (default).	0	RW SC
14				

31:12	−	Always reads 0	0	RO
11	10 Mb/s Half Duplex	Always reads 1 Indicates the PHY is a 10 Mb/s half−duplex device.	1	RO
10:8	−	Always reads 0	000	RO
7	Unidirectional Ability	Always reads 0 10BASE−T1S does not support unidirectional links.	0	RO
6	MF Preamble Suppression	Always reads 0 The PHY does not accept MDIO		

31	EN	1 = Filter enabled 0 = Filter disabled When set, enables the corresponding Address Filter 1. ADRF in the MAC Control register (MMS1, 0x0000 bit 16) shall also be enabled for address filtering to work.	0	RW
30:16	–	Not used	0x0000	RO
15:0	ADDRFILT1[47:32]	Higher order bits of the Filter Address.	0x0000	RW

31:0	ADDFILTL2[31:0]	Holds the 32 lower order bits of the Address Filter 2 that is spilt into ADDRFILT2L and ADDRFILT2H.	0x00000000	RW

31	EN	1 = Filter enabled 0 = Filter disabled When set, enables the corresponding Address Filter 2. ADRF in the MAC Control register (MMS1, 0x0000 bit 16) shall also be enabled for address filtering to work.	0	RW
30:16	–	Not used	0x0000	RO
15:0	ADDRFILT2[47:32]	Higher order bits of the Filter Address.	0x0000	RW

31:0	ADDFILT3[31:0]	Holds the 32 lower order bits of the Address Filter 3 that is spilt into ADDRFILT3L and ADDRFILT3H.	0x00000000	RW

31	EN	1 = Filter enabled 0 = Filter disabled When set, enables the corresponding Address Filter 3. ADRF in the MAC Control register (MMS1, 0x0000 bit 16) shall also be enabled for address filtering to work.	0	RW
30:16	–	Not used	0x0000	RO
15:0	ADDRFILT3[47:32]	Higher order bits of the Filter Address.	0x0000	RW

31:0	ADDRMASK0[31:0]	Holds the 32 lower order bits of the Address Filter 0 mask that is spilt into ADDRMASK0L and ADDRMASK0H.	0xFFFFFFFF	RW

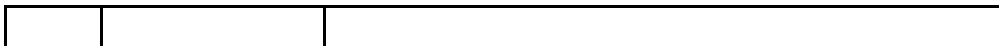
31:16	–	Not used	0x0000	RO
15:0	ADDRMASK0[47:0]	Higher order bits of the Filter 0 Address Mask.	0xFFFF	RW

31:0	ADDRMASK1[31:0]	Holds the 32 lower order bits of the Address Filter 1 mask that is spilt into ADDRMASK1L and ADDRMASK1H.	0xFFFFFFFF	RW

31:16	–	Not used	0x0000	RO
15:0	ADDRMASK1[47:0]	Higher order bits of the Filter 1 Address Mask.	0xFFFF	RW

31:0	ADDRMASK2[31:0]	Holds the 32 lower order bits of the Address Filter 2 mask that is spilt into ADDRMASK2L and ADDRMASK2H.	0xFFFFFFFF	RW

31:16	–	Not used	0x0000	RO
15:0	ADDRMASK2[47:0]	Higher order bits of the Filter 2 Address Mask.	0xFFFF	RW



31:0	STFRAMESTX256	MAC statistic register. Holds the number of frames transmitted successfully since the last read of this register, with a size between 256 bytes and 511 bytes. This counter does not overflow from its maximum value of 0xFFFFFFFF and is cleared after a read access.	0x0000	RO−SCR

31:0	STFRAMESTX512	MAC statistic register. Holds the number of frames transmitted successfully since the last read of this register, with a size between 512 bytes and 1023 bytes. This counter does not overflow from its maximum value of 0xFFFFFFFF and is cleared after a read access.	0x0000	RO−SCR

31:0	STFRAMESTX1024	MAC statistic register. Holds the number of frames transmitted successfully since the last read of this register, with a size of 1024 bytes or more. This counter does not overflow from its maximum value of 0xFFFFFFFF and is cleared after a read access.	0x0000	RO−SCR

31:10	−	Not used	0x000000	RO
9:0	STUNDERFLOW	MAC statistic register. Holds the number of frames aborted due to a TX buffer underflow. This can only happen in cut−through mode, if the host does not send frame data fast enough. This counter does not overflow from its maximum value of 0x000003FF. It is cleared after a read access.	0x0000	RO−SCR

31:18	−	Not used	0x0000	RO
17:0	STSINGLECOL	MAC statistic register. Holds the number of frames transmitted after a single collision event. When PLCA is enabled, the register counts the logical collisions reported		

31:18	−	Not used	0x0000	RO
17:0	STMULTICOL	MAC statistic register. Holds the number of frames transmitted after multiple collision events. When PLCA is enabled, the register should not count any event. Multiple collisions happening on a PLCA enabled network may indicate a misconfiguration of the fundamental parameters (e.g. TO_TIMER), the presence of non−PLCA nodes on the same medium or a defective node on the network. This counter does not overflow from its maximum value of 0x0003FFFF. It is cleared after a read access.	0x00000	RO−SCR

31:10	−	Not used	0x000000	RO
9:0	STEXCESSCOL	MAC statistic register. Holds the number of outgoing frames that were aborted because too many collisions happened. When PLCA is enabled, the register should not count any event. Excessive collisions happening on a PLCA enabled network may indicate wrong configuration of fundamental parameters (e.g. TO_TIMER), the presence of non−PLCA nodes on the network or a defective node. This counter does not overflow from its maximum value of 0x000003FF. It is cleared after a read access.	0x000	RO−SCR

31:18	−	Not used	0x0000	RO
17:0	STDEFERREDTX	MAC statistic register. Holds the number of frames transmitted after being deferred. Refer to IEEE802.3 clause 5.2.2 for details. In PLCA enabled networks, deferral is part of the arbitration mechanism. Therefore, a non−zero value in this counter does not indicate degradation of network performance. This counter does not overflow from its maximum value of 0x0003FFFF. It is cleared after a read access.	0x00000	RO−SCR

−

31:10	−	Not used	0x0000	RO
9:0	STCRSERR	MAC statistic register. Counts events where carrier indication is de−asserted or not asserted by the PHY during transmission of a frame. A non−zero value in this register may indicate a too high level of noise on the line This counter does not overflow from its maximum value of 0x000003FF. It is cleared after a read access.	0x00000	RO−SCR

31:0	STOCTETSRX[31:0]	MAC statistic register. STOCTETSRXL holds the 32 low order bits of the cumulative sum of all data bytes received since the register was last read. Together with the STOCTETSRXH, this register represents the number of received bytes. The bytes comprise the whole frame, from the first byte of the destination address up to (and including) the FCS. If the counter reaches its maximum value of 0xFFFFFFFFFFFF, it wraps to zero. The counter clears when both STOCTETSRXL and STOCTETSRXH have been read. NOTE: internal logic samples the high order bits of the 48−bit counter into the STOCTETSRXH register, every time the STOCTETSRXL register is read. For reading the correct number of bytes received, the host shall read the STOCTETSRXL register first, followed by the STOCTETSRXH register, in that order exactly.	0x00000000	RO−SCR

31:16	−	Not used	0x0000	RO
15:0	STOCTETSRX[47:32]	MAC statistic register. STOCTETSRXH holds the 16 high order bits of the cumulative sum of all data bytes received since the last read.	0x0000	RO−SCR

31:0	STFRAMESRXOK	MAC statistic register. Holds the number of frames received successfully since last read of this register. This counter does not overflow from its maximum value of 0xFFFFFFFF, and it is reset after a read access.	0x0000	RO−SCR

31:0	STBCASTRXOK	MAC statistic register. Holds the number of broadcast frames (destination address FF:FF:FF:FF:FF:FF) received successfully since the last read of this register. This counter does not overflow from its maximum value of 0xFFFFFFFF. It resets to 0 after a read access.	0x0000	RO−SCR

31:0	STMCASTRXOK	MAC statistic register. Holds the number of multicast frames (first bit of destination address set to 1) received successfully since the last read of this register. This counter does not overflow from its maximum value of 0xFFFFFFFF. It resets to 0 after a read access.	0x0000	RO−SCR

−

– –

31:0	STFRAMESRX65	MAC statistic register. Holds the number of frames received successfully since the last read of this register, with a size between 65 bytes and 127 bytes. This counter does not overflow from its maximum value of 0xFFFFFFFF. It is cleared after a read access.	0x0000	RO−SCR

– –

31:10	–	Not used	0x000000	RO
9:0	STRXTOOLONG	MAC statistic register. Holds the number of received frames that were dropped due to their length being longer than 2000 bytes. This counter does not overflow from its maximum value of 0x000003FF and it is cleared after a read access.	0x000	RO−SCR

31:10	–	Not used	0x000000	RO
9:0	STFCSERRS	MAC statistic register. Frame Check Sequence (FCS) error counter. Holds the number of received frames that were dropped due a frame check sequence mismatch. This counter does not overflow from its maximum value of 0x000003FF, and it is cleared after a read access.	0x000	RO−SCR

31:10	–	Not used	0x000000	RO
9:0	STSYMBOLERRS	MAC statistic register. Holds the number of received frames that were dropped due to the PHY reporting a symbol decoding error. This may be caused by excessive differential noise on the line and may also happen if the remote peer aborted the frame. This counter does not overflow from its maximum value of 0x000003FF. It is cleared after a read access.	0x000	RO−SCR

31:10	–	Not used	0x000000	RO
9:0	STALIGNERRS	MAC statistic register. Holds the number of received frames that were dropped because their size was not byte−aligned. This may be caused by excessive differential noise on the line or collisions when PLCA is not enabled. This counter does not overflow from its maximum value of 0x000003FF. It is cleared after a read access.	0x000	RO−SCR

31:10	–	Not used	0x000000	RO
9:0	STRXOVERFLOW	MAC statistic register. Holds the number of received frames that were aborted because the host failed to retrieve data at a sufficient rate, causing the RX buffer to overflow. Note that such aborted frames are still counted as “received successfully” at the MAC layer (and other statistic registers). This counter does not overflow from its maximum value of 0x000003FF. It is cleared after a read access.	0x000	RO−SCR

31:0	STRXDROPPED	MAC statistic register. Holds the number of received frames that were successfully received, but dropped because of address filtering. Dropped frames include frames that did not pass the checks against ADDRFILTx/ADDRMASKx, broadcast frames filtered by the BCSF bit stetting and multicast frames filtered by the MCSF bit setting in the MAC control register (MMS 1, 0x0000). Note that such frames are still counted as ”received successfully” at the MAC layer (and other statistic registers). This counter does not overflow from its maximum value of 0xFFFFFFFF. It is cleared after a read access.	0x00000000	RO−SCR

Memory Map Selection 2 contains a direct mapping of Clause 45 MMD 3 PHY PCS registers implemented in the NCN26010 device.

While register access though the SPI interface is always 32 bit, all MMS2 registers are 16 bit registers. The 2 most significant bytes of these registers always contain 0x0000 and cannot be altered by register writes.

15:4	−	Always reads 0	0x000	RO
3	PCS Present	Always reads 1 Indicating that the device contains the PCS.	1	RO
2	−	Always reads 0	0	RO
1	PMA Present	Always reads 1 Indicating that the device contains the PMA.	1	RO
0	Clause 22 Registers Present	Always reads 1 Indicating that the device contains Clause 22 standard registers.	1	RO

15:0	−	Always reads 0	0x0000	RO

–

15	PCS Reset	1 = PCS reset 0 = normal operation Setting this bit to 1 sets all 10BASE−T1S PCS registers to their default state. This may change the internal state of the PHY's PCS and the state of		

–

15:0	PCS Physical Collisions Count	Counts the number of physical collision events detected by the PHY since this register was last read. If the count reaches 0xFFFF, no more errors are counted to prevent the counter from overflowing. NOTE: Physical collisions are caused by the superposition of signals transmitted simultaneously by more than one station on the same medium. In contrast to physical collisions, logical collisions in PLCA mode are triggered by the PCLA RS arbitration algorithm.	0	RO−SC

Memory Map Selection 3 contains a direct mapping of Clause 45 MMD 3 PHY PCS registers implemented in the NCN26010 device.

All MMS3 registers ar16 bit registers.

15:4	−	Always reads 0	0	RO
3	PCS Present	Always returns 1 Indicating that the device contains the PCS.	1	RO
2	−	Always returns 0	0	RO
1	PMA Present	Always returns 1 Indicating that the device contains the PMA.	1	RO
0	Clause 22 Registers Present	Always returns 1 Indicating that the device contains Clause 22 standard registers.	1	RO

15:0	−	Always reads 0	0x0000	RO

−

15:4	−	Always reads 0	0	RO
3	10BASE−T1S	Always reads 1 This is a 10BASE−T1S only device.	1	RO
2:0	−	Always reads 0	0	RO

−

15	PMA Reset	Alias of Clause 22 bit 0.15 and MII Control Register bit 15 Soft Reset Setting this bit to one triggers a soft reset of the NCN26010. This bit self−clears when the reset finishes.	0	RW−SC
14	Transmit Disable	1 = disable Transmit 0 = enable Transmit When set, the embedded PHY transmitter is shut down and TX requests from the MAC (SPI) are ignored.	0	RW
13:12	−	Always reads 0	0	RO
11	Low Power Mode	Not implemented	0	RO
10	Multi−Drop Enable	Always reads 1 This NCN26010 is a multi−drop only device.	1	RO
9:1	−	Always reads 0	0	RO
0	Loopback Mode	Same as Clause 22 bit 0.14 and MIIM control register MMS1, address 0xFF00, bit 14.	0	RW

–

15:14	−	Always reads 0	0	RO
13	Loopback Ability	Always reads 1, indicating the PHY supports loopback.	1	RO
12	−	Always reads 0	0	RO
11	Low Power Ability	Always reads 0 The PHY does not support Low Power Mode.	0	RO
10	Multi−Drop Ability	Always reads 1 This NCN26010 supports half duplex multi−drop operation.	1	RO
9	Receive Fault Ability	Always reads 1 The PHY supports receive fault detection.	1	RO
8:2	−	Always reads 0	0	RO
1	Remote Jabber	Copy of Clause 22 Register 1.4 and MIIM Status register, MMS1, Address 0xFF01, bit 4. Auto clear to zero on read. See the MIIM Status register for description.	0	RO−LH
0	−	Always reads 0	0	RO

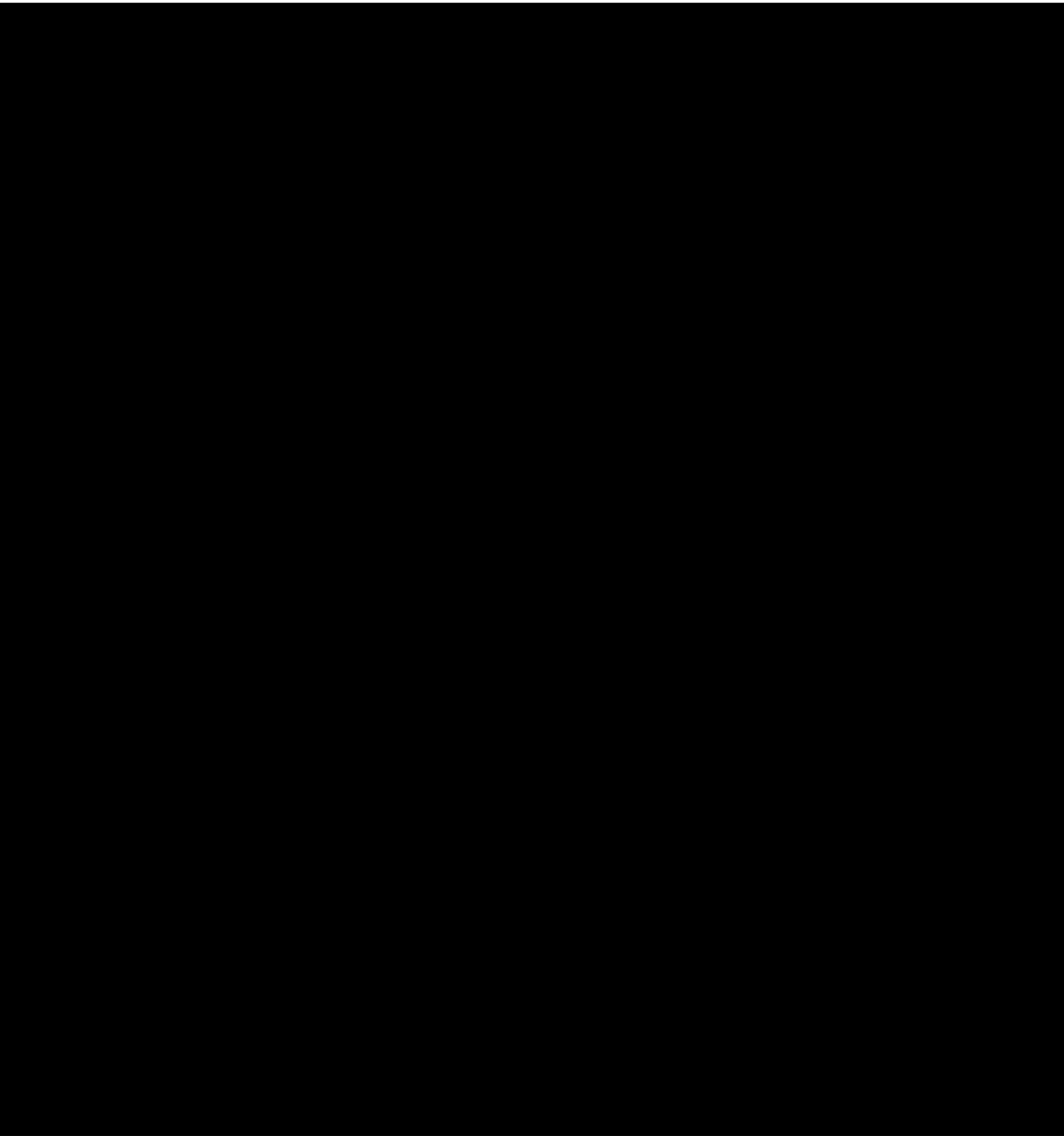
–

15:13	Test Mode	Test mode in accordance with IEEE802.3cg. Default is normal operation	000	RW
		000	Normal Operation	
		001	Transmitter Output Voltage test	
		010	Transmitter Output Droop test	
		011	Transmitter PSD mask test	
		100	Transmitter high Impedance test	
		101	Reserved	
		110	Reserved	
		111	Reserved	
12:0	−	Always reads 0	0	R

Memory Map Selection 4 contains a direct mapping of Clause 45 MMD 31 PLCA and vendor specific PHY registers implemented in the NCN26010 device.

All MMS4 registers are 16 bit registers.

15:12	Major Revision	Major release number		



15	Beacon TX / RX Status PST	When one, this bit indicates that the PLCA RS is receiving / transmitting the BEACON. Note that only the coordinator node transmits the BEACON. When this bit reads 0, the PHY is not ready to send or receive data in PLCA mode. This could also be interpreted as an indicator of PLCA activity on the line.	–	RO
14:0	–	Always reads 0	0x0000	RO

15:8	–	Always reads 0	0x00	RO
7:0				

Memory Map Selection 12 contains a direct mapping of Clause 45 MMD 30 vendor specific registers implemented in the NCN26010 device.

All MMS12 registers are 16 bit registers.

15:6	No Used	Not used	0x000	R
5	Physical Collision Report	1 = PHYINT on Physical Collision enabled 0 = PHYINT on Physical Collision disabled If enabled, a PHYINT event is issued every time a physical collision is detected.	0	R/W
4	PLCA Recovery Report	1 = PHYINT on PLCA Recovery enabled 0 = PHYINT on PLCA Recovery disabled When enabled, a PHYINT is issued on every PLCA Recovery event. PLCA recovery is flagged when a false carrier event (e.g. impulse noise) occurs on the line. When a CRS event is not followed by the reception of a packet within a certain amount of time the embedded PHY goes to either of two states, depending on its PLCA settings: When configured as coordinator node, the PHY waits for the line to be quiet for a certain amount of time and then sends a new BEACON. When not configured as a coordinator node, the PHY will wait for a BEACON before getting a new transmit opportunity.	0	R/W
3	Remote Jabber Report	1 = PHYINT on Remote Jabber enabled 0 = PHYINT on Remote Jabber disabled When enabled, a PHYINT is issued every time the embedded PHY detects a remote jabber condition. A remote jabber condition occurs if a station transmits for longer than a maximum length Ethernet frame transmit duration (2000 bytes, including FCS).	0	R/W
2	Local Jabber Report	1 = PHYINT on Local Jabber enabled 0 = PHYINT on Local Jabber disabled When enabled, a PHYINT event is asserted when the NCN26010 detects a local jabber condition.	0	R/W
1	PLCA Status Change Report	1 = PHYINT on change of PLCA Status 0 = no PHYINT on change of PLCA Status When enabled, the device issues a PHYINT every time the PLCA Status changes. To determine the actual PLCA status, the host interrupt service routine would have to read the PLCA Status Register, PLCASTATUS (MMS4, Address 0xCA03).	0	R/W
0	Link Stats Change Report	1 = PHYINT on change of Link Status enabled 0 = PHYINT on change of Link Status disabled When enabled, a PHYINT event is issued every time the link status changed. The actual link status can be read from the Link Status bit (0.2) in the PHY Status register MMS 0, Address 0xFF01.	0	R/W

5. Note in this table PHYINT is refered to as an interrup request internal to the NCN26010 device and not the IRQn pin on the device. The difference is that the PHYINT can be masked and shall be acknowledged separately.

Whenever an IRQ occurs, the user should read this register to determine the source of the interrupt. All the bits latch high and self−clear on read of this register.

15	Reset Status	This bit is set at Power−On−Reset or any other form of hardware reset. Its		

(continued)

The PHY TWEAKS register allows experienced users to customize the parameters of the analog line driver among other custom parameters. The default values have been carefully selected and do not need modification under normal conditions.

		8	550	
		9	600	
		10	650	
		11	700	
		12	750	
		13	800	
		14	850	
		15	900	
		NOTE: This is an advanced configuration register. It is recommended to consult with before changing the value from its default settings.		
5	Digital Slew Rate	0 = slow 1 = fast (default) Sets the output slew rate of the all digital I/Os, excluding DIO0 and DIO1. Setting the slew rate to “fast” might improve signal integrity when driving higher capacitive loads, but yields the opposite effect in low capacitive load scenarios.	1	R/W
4:3	CMC Compensation	In case a common mode choke is used on the line, these bits can be set to compensate for the added common−mode choke resistance:	0	R/W
			Ω	
		0b00	0 – 0.5 (default)	
		0b01	0.5 – 2−25	
		0b10	2.25 – 3.75	
		0b11	3.75 − 5	
2	TX Slew	0 = slow 1 = fast This sets the slew rate of the TX line driver output. Setting this to “slow” can help improve EMC performance but may have a negative effect on return loss.	0	RW
1	Not Used	−	0	R
0	CLK Out Enable	1 = enabled (default) 0 = disabled When enabled, the PHY’s internal 25 MHz clock is output at CLKO. When disabled, the CLKO pin drives a logic low level.	1	R/W

15:0	MACID [15:0]	Lower 16 bit of the unique MAC address. Together with the upper 8 bits in the MACID1 register, and the OUI from IDVER (MMS0, address 0x0000, bits 31:10), it forms a unique MAC address for the NCN26010 device. Note that no Address Filter is pre−initialized with that MAC address. The user should read MACID0, MACID1 and OUI (from IDVER) to initialize the address filters. The host may also need to use the MAC address as the source address in Ethernet frames sent to the NCN26010.	−	RO

15:8	–	Not used	–	RO
7:0	MACID[23:16]	Upper 8 bits of the MAC address. See description in MACID0 for details.	–	RO

15	Not Used		0	R
14:8	Wafer_Y	Y position on the Wafer from where the part was picked.	–	R
7	Not Used		0	R
6:0	Wafer_X	X position on the Wafer from where the part was picked.	–	R

Clock Source

The NCN26010 requires a precise and robust 25 MHz clock source for correct operation.

The clock can either be fed from an external 25 MHz clock

QFN32 4x4, 0.4P
CASE 485GH
ISSUE O

DATE 20 APR 2021