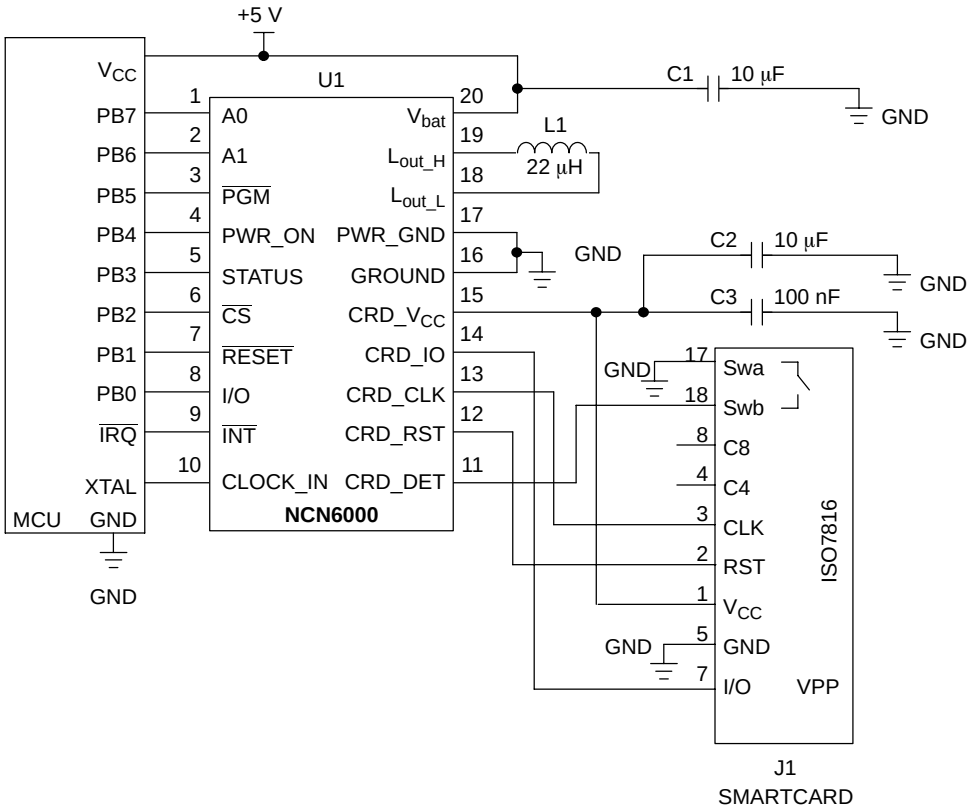
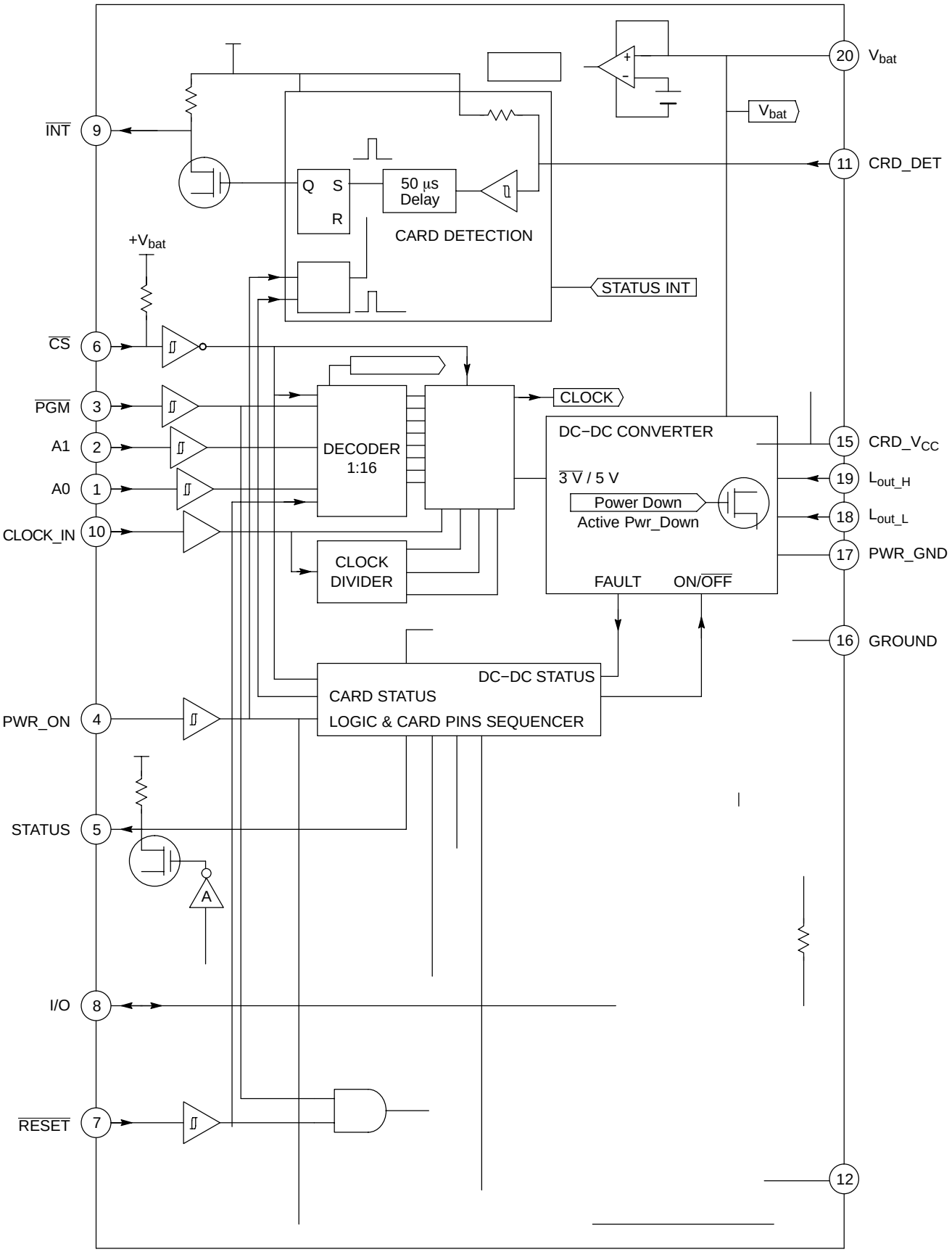
TSSOP−20
DTB SUFFIX
CASE 948E

NCN6000DTB	TSSOP−20*	75 Units / Rail

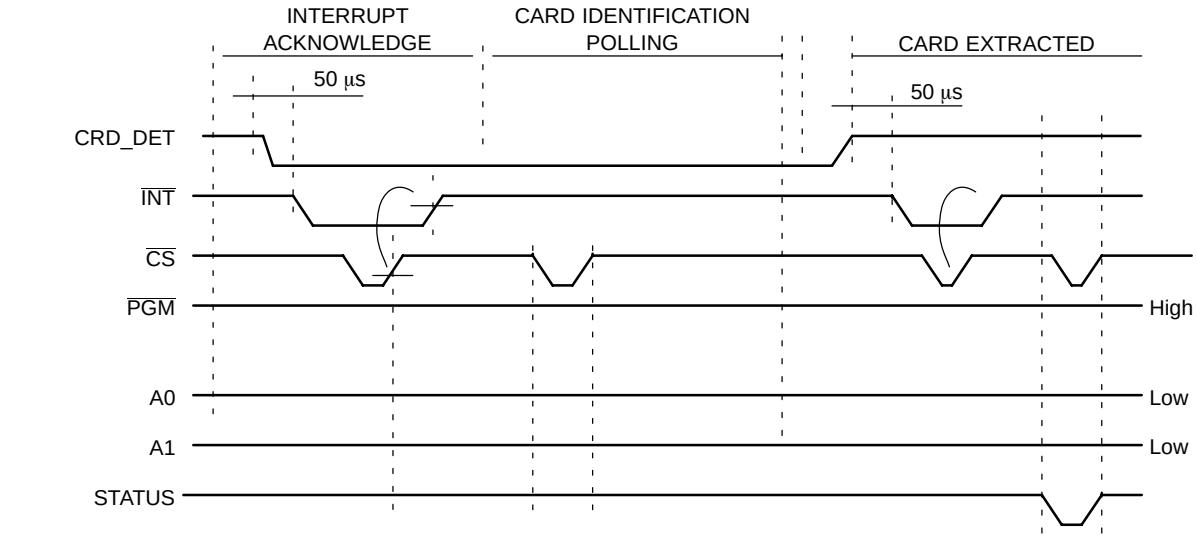

+5 V
U1
C1
10 µF
GND
L1
22 µH
C2
10 µF
C3
100 nF
GND
GND
GND
GND
GND
GND
GND
MCU
VCC
PB7
PB6
PB5
PB4
PB3
PB2
PB1
PB0
IRQ
XTAL
GND
1
2
3
4
5
6
7
8
9
10
A0
A1
PGM
PWR_ON
STATUS
CS
RESET
I/O
INT
CLOCK_IN
Vbat
Lout_H
Lout_L
PWR_GND
GROUND
CRD_VCC
CRD_IO
CRD_CLK
CRD_RST
CRD_DET
20
19
18
17
16
15
14
13
12
11
NCN6000
17
18
8
4
3
2
1
5
7
Swa
Swb
C8
C4
CLK
RST
VCC
GND
I/O
VPP
ISO7816
J1
SMARTCARD


20 Vbat
Vbat
INT 9
11 CRD_DET
Q S
R
50 µs Delay
CARD DETECTION
+Vbat
STATUS INT
CS 6
PGM 3
A1 2
A0 1
CLOCK_IN 10
CLOCK
DECODER 1:16
CLOCK DIVIDER
DC−DC CONVERTER
3 V / 5 V
Power Down
Active Pwr_Down
FAULT
ON/OFF
15 CRD_VCC
19 Lout_H
18 Lout_L
17 PWR_GND
16 GROUND
DC−DC STATUS
CARD STATUS
LOGIC & CARD PINS SEQUENCER
PWR_ON 4
STATUS 5
A
I/O 8
RESET 7
12

- -

3 V CLOCK_IN 1/1
5 V CLOCK_IN 1/1

The programming can be achieved with the card powered ON or OFF. The identification of the interrupt is carried out by polling the STATUS pin, the Vbat voltage and the DC−DC results being provided on the same pin as depicted by the table in Figure 4. During the programming mode, the $\overline{PGM}$ pin can be released to High since the mode is internally latched by the Negative going transition presents on the Chip Select pin.



ABBREVIATIONS

Lout_H	DC−DC External Inductor
Lout_L	DC−DC External Inductor
Cout	Output Capacitor
VCC	Card Power Supply Input
Icc	Current at CRD_VCC Pin
Class A	5.0 V Smart Card
Class B	3.0 V Smart Card
$\overline{CS}$	Chip Select (from MPU)
Z	High Impedance Logic State (according to ISO7816)
CRD_VCC	Interface IC Card Power Supply Output
CRD_CLK	Interface IC Card Clock Output
CRD_RST	Interface IC Card ResN1kCRD_RST

PIN FUNCTIONS AND DESCRIPTION (continued)

Pin	Name	Type	Description
8	I/O	Input/Output Pull Up	This pin is connected to an external microcontroller interface. A bidirectional level translator adapts the serial I/O signal between the smart card and the microcontroller. The level translator is enabled when $\overline{CS}$ = L. The signal present on this pin is latched when $\overline{CS}$ = H. This pin is also used in programming mode (Tables 1, 2 and 3, Figures 4 and 5).
9	$\overline{INT}$	OUTPUT Pull Down	toTJT*0.014 69(Tha logic Tfo6 e mirisg moedg)f eie mrS

NCN6000

POWER SUPPLY SECTION (−25°C to +85°C ambient temperature, unless otherwise noted.)

Rating	Symbol	Pin	Min	Typ	Max	Unit
Power Supply	Vbat	20	2.7	−	6.0	V
Standby Supply Current Conditions: PWR_ON = L, STATUS = H, CLOCK_IN = H, $\overline{CS}$ = H. All other logic inputs and outputs are open: Vbat = 3.0 V Vbat = 5.0 V	$Ibat_{sb}$	20	 − −	 3.0 −	 8.0 15	μA
DC Operating Current (Figure 19) PWR_ON = H, CLOCK_IN = 0, $\overline{CS}$ = H, all CRD pins unloaded @ Vbat = 6.0 V, CRD_VCC = 5.0 V @ Vbat = 3.6 V, CRD_VCC = 5.0 V	$Ibat_{op}$	20	 − −	 7.0 2.0	 − 5.0	mA
Vbat Undervoltage $Detection_{High}$ Vbat Undervoltage $Detection_{Low}$ Vbat Undervoltage $Detection_{Hysteresis}$	$Vbat_{LH}$ $Vbat_{LL}$ $Vbat_{HY}$	20	2.1 2.0 −	− − 100	2.7 2.6 −	

DIGITAL PARAMETERS SECTION @ 2.70 V ≤ Vbat ≤ 6.0 V, NORMAL OPERATING MODE (−25°C to +85°C ambient temperature, unless otherwise noted.) Note: Digital inputs undershoot < −0.30 V to ground, Digital inputs overshoot <0.30 V to Vbat

Rating	Symbol	Pin	Min	Typ	Max	Unit
Input Asynchronous Clock Duty Cycle = 50% @ Vbat = 3.0V over the temperature range	F_{CLKIN}	10	−	−	40	MHz
tr10Clock Rise Time	F_{tr}	10	−	−	5.0	ns
5.0Clock Fall Time	F_{tf}		−	−	5.0	

I/O Data Transfer Switching Time,

SMART CARD SECTION (−25°C to +85°C ambient temperature, unless otherwise noted.)

Rating	Symbol	Pin	Min	Typ	Max	Unit
CRD_RST @ CRD_VCC = +5.0 V		12		−		
Output $\overline{\text{RESET}}$ V_{OH} @ Icrd_rst = −20 μA	V_{OH}		CRD_VCC − 0.9		CRD_VCC	V
Output $\overline{\text{RESET}}$ V_{OL} @ Icrd_rst = 200 μA	V_{OL}		0		0.4	V
Output $\overline{\text{RESET}}$ Rise Time @ Cout = 30 pF	t_R				100	ns
Output $\overline{\text{RESET}}$ Fall Time @ Cout = 30 pF	t_F				100	ns
CRD_RST @ Vcc = +3.0 V						
Output $\overline{\text{RESET}}$ V_{OH} @ Icrd_rst = −20 μA	V_{OH}		CRD_VCC − 0.9		CRD_VCC	V
Output $\overline{\text{RESET}}$ V_{OL} @ Icrd_rst = 200 μA	V_{OL}		0		0.4	V
Output $\overline{\text{RESET}}$ Rise Time @ Cout = 30 pF	t_R				100	ns
Output $\overline{\text{RESET}}$ Fall Time @ Cout = 30 pF	t_F				100	ns
CRD_CLK @ CRD_VCC = +3.0 V or +5.0 V		13		−		
CRD_VCC = +5.0 V						
Output Frequency (See Note 8)	F_{CRDCLK}				5.0	MHz
Output Duty Cycle @ DC Fin = 50% ±1%	F_{CRDDC}		45		55	%
Output CRD_CLK Rise Time @ Cout = 30 pF	t_R				18	ns
Output CRD_CLK Fall Time @ Cout = 30 pF	t_F				18	ns
Output V_{OH} @ Icrd_clk = −20 μA	V_{OH}		3.15		CRD_VCC	V
Output V_{OL} @ Icrd_clk = 100 μA	V_{OL}		0		+0.5	V
CRD_VCC = +3.0 V						
Output Frequency (See Note 8)	F_{CRDCLK}				5.0	MHz
Output Duty Cycle @ DC Fin = 50% ±1%	F_{CRDDC}		40		60	%
Output CRD_CLK Rise Time @ Cout = 30 pF	t_R				18	ns
Output CRD_CLK Fall Time @ Cout = 30 pF	t_F				18	ns
Output V_{OH} @ Icrd_clk = −20 μA @ Cout = 30 pF	V_{OH}		1.85		CRD_VCC	V
Output V_{OL} @ Icrd_clk = 100 μA @ Cout = 30 pF	V_{OL}		0		0.7	V
CRD_I/O @ CRD_VCC = +5.0 V						
CRD_I/O Data Transfer Frequency						
CRD_I/O Rise Time @ Cout = 30 pF						
CRD_I/O Fall Time @ Cout = 30 pF						
Output V_{OH} @ Icrd_i/o = −20 μA						
Output V_{OL} @ Icrd_i/o = 500 μA, V_{IL} = 0 V						
CRD_I/O @ CRD_VCC = +3.0 V						
CRD_I/O Data Transfer Frequency						
CRD_I/O Rise Time @ Cout = 30 pF						
CRD_I/O Fall Time @ Cout = 30 pF						
Output V_{OH} @ Icrd_i/o = −20 μA						
Output V_{OL} @ Icrd_i/o = 500 μA, V_{IL} = 0 V						

Programming and Status Functions

The NCN6000 features a programming interface and a status interface. Figure 4 illustrates the programming mode.

Table 1. Programming and Status Functions Pinout Logic

Pins	Name	CRD_VCC Prg. 3.0 V/5.0 V	CLOCK_IN Divide Ratio	CRD_DET	CLOCK STOP AND START	Poll Card Status	DC−DC Status	Vbat Status	CRD_VCC Status
5	STATUS	Not Affected	Not Affected	Not Affected	Not Affected	READ	READ	READ	READ
6	$\overline{CS}$	Latch On Rising Edge	Latch On Rising Edge	Latch On Rising Edge	Latch On Rising Edge	0	0	0	0
3	$\overline{PGM}$	0	0	0	0	1	1	1	1

Card VCC, Card CLOCK and Card Detection Polarity Programming

The CRD_VCC and CLOCK_IN programming options allows matching the system frequency with the card clock frequency, and to select 3.0 V or 5.0 V CRD_VCC supply. The CRD_DET programming option allows the usage of either Normally Open or Normally Close detection switch. Table 3 highlights the A0, A1, $\overline{PGM}$ and I/O logic states for the possible options. **The default power up reset condition is state 1: asynchronous clock, ratio 1/1, CRD_CLK active, CRD_DET = Normally Open, CRD_VCC = 3.0 V**. All states are latched for each output variable in programming mode at the positive going slope of Chip Select [$\overline{CS}$] signal. It is the system designer's responsibility to set up the options needed to match the chip with the peripherals. In particular, when using Normally Close switch, the CRD_DET polarity must s9he A0,

DC−DC Converter and Card Detector Status

The NCN6000 status can be polled when $\overline{CS}$ = L. Please consult Figures 4 and 5 for a description of input and output signals. The status message is described in Table 4.

Note: in order to cope with a start up under low battery condition, the Vbat OK message uses a negative logic as depicted here below.

Table 4. Card and DC−DC Status Output

$\overline{PGM}$	A1	A0	STATUS	Message
HIGH	L	L	LOW	No Card
HIGH	L	L	HIGH	Card Present
HIGH	L	H	LOW	DC−DC Converter Overloaded
HIGH	L	H	HIGH	DC−DC Converter OK
HIGH	H	L	LOW	Vbat OK
HIGH	H	L	HIGH	Vbat Undervoltage
HIGH	H	H	HIGH	CRD_VCC OK
HIGH	H	H	LOW	CRD_VCC Undervoltage

The STATUS pin provides a feedback related to the detection of the card, the state of the DC−DC converter, the Vbat undervoltage and CRD_VCC undervoltage situations. When $\overline{PGM}$ = H, the STATUS pin returns a High if a card is

Basic Operating Modes Flow Chart

The NCN6000 brings all the functions necessary to handle data communication between a host computer and the smart card. The built−in Chip Select pin provides a simple way to share the same MPU bus with several card interface. On top of that, the logic control are derived from specific pins, avoiding the risk of mixing up the operation when the interface is controlled by a low end microcontroller.

During the transaction operation, the external MPU takes care of whatever is necessary to he data on the single bidirectional I/O line. Leaving aside the DC−DC control and associated failures, the NCN6000 does not take any further responsibility in the data transaction.

When the chip operates in the programming mode, the NCN6000 provide a flexible access to set up the CRD_VCC voltage, the CRD_CLK and the CRD_DET smart card signals.

The external microcontroller takes care of the smart card transaction and shall handle the interface accordingly.

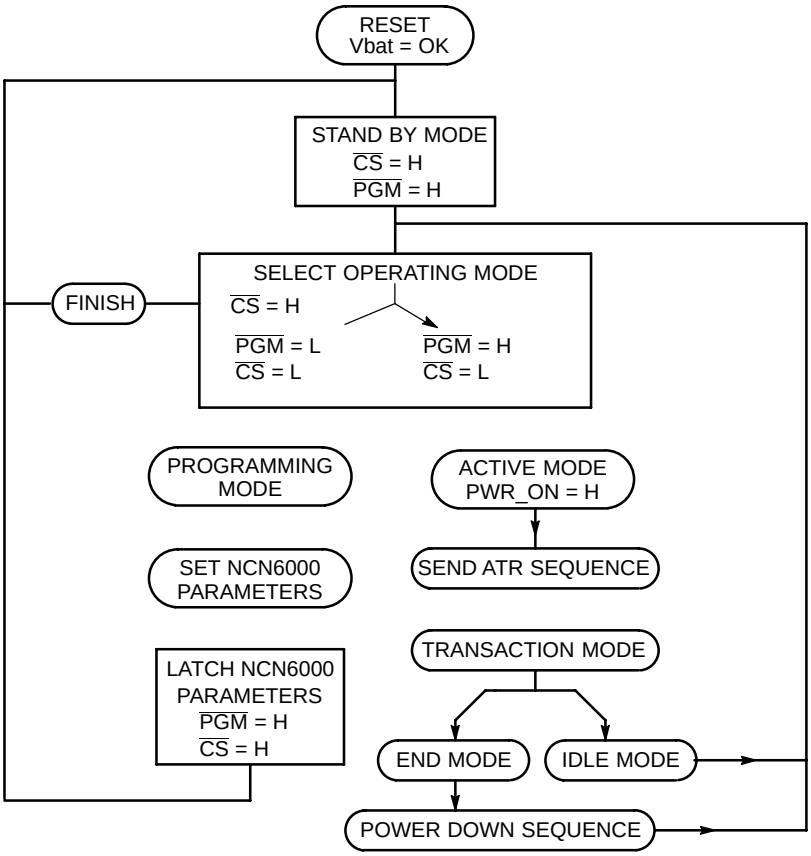


Figure 7. Operating Modes Flow Chart

Programming Mode

The programming mode allows the configuration of the card power supply, card clock and Card Detection input logic polarity. These signals (CRD_VCC, CRD_CLK and CRD_DET) are described in the pin description paragraph associated with Tables 1 and 3 and Figures 4 and 8.

Programming Mode Logic Conditions:		**Card Output:**	
$\overline{CS}$	= L	CRD_VCC	= 0 V
PWR_ON	= L	CRD_CLK	= L
A0	= H/L	CRD_RST	= L
A1	= H/L	CRD_IO	= H/L depending upon the previous I/O pin logic state
$\overline{PGM}$	= L		
I/O	= L/H		
$\overline{RESET}$	= L/H		

The I/O and $\overline{RESET}$ pins are not connected to the smart card and become logic inputs to control the NCN6000 programming sequence. The programmed values are latched upon transition of $\overline{CS}$ from Low to High, $\overline{PGM}$ being Low during the transition.

When a programming mode is validated by a Chip Select negative going transient, the mode is latched and $\overline{PGM}$ can be released to High. This latch is automatically reset when $\overline{CS}$ returns to High.

The logic input signals can be set simultaneously, or one bit a time (using either a STAA or a BSET function), the key point being the minimum delay between the shorter bit and the Chip Select pulse. The programmed value is latched into the NCN6000 register on the $\overline{CS}$ positive going edge.

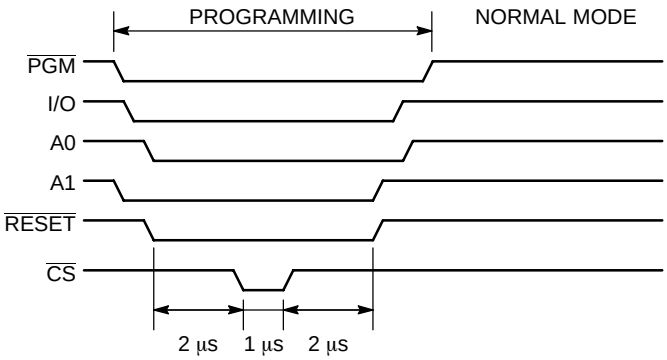


Figure 8. Minimum Programming Timings

Active Mode

In the active mode, the NCN6000 is selected by the external MPU and the STATUS pin can be polled to get the status of either the DC−DC converter or the presence of the card (inserted or not valid). The power is not connected to the card: CRD_VCC = 0 V.

Active Mode Logic Conditions:		**Card Output:**	
$\overline{CS}$	= L	CRD_VCC	= 0 V
PWR_ON	= L	CRD_CLK	= L
A0	= L	CRD_RST	= L
A1	= L	CRD_IO	= H/L depending upon the previous I/O pin logic state
$\overline{PGM}$	= H		
I/O	= Z		
$\overline{RESET}$	= Z		
STATUS	= L/H is Card Inserted?		

The Chip Select pulse [$\overline{CS}$] will automatically clear the previously asserted $\overline{INT}$ signal upon the positive going transition.

If a card is present, the MPU shall activate the DC−DC converter by asserting PWR_ON = H. The NCN6000 will automatically run a power up sequence when the CRD_VCC reaches the undervoltage level (either V_{C5H} or V_{C3H}, depending upon the CRD_VCC voltage supply programmed). The CRD_IO, CRD_RST and CRD_CLK pins are validated, according to the ISO7816−3 sequence. The interface is now in transaction mode and the system is ready for data exchange through the I/O and $\overline{RESET}$ lines. At any time, the microcontroller can change the CRD_CLK frequency and mode, or the CRD_VCC value as determined by the card being in use.

Transaction Mode

During the transaction mode, the NCN6000 maintains power supply and clock signal to the card. All the signal levels related with the card are translated as necessary to cope with the MPU and the card.

The DC−DC converter status and the Vbat state can be monitored on the STATUS by using the A0 and A1 logic inputs as depicted in Tables 3 and 4.

Transaction Mode Logic Conditions:		**Card Output:**	
$\overline{CS}$	= L	CRD_VCC	= 3.0 or 5.0 V
PWR_ON	= H	CRD_CLK	= CLOCK
A0	= H	CRD_RST	= H/L
A1	= H	CRD_IO	= DATA TRANSFER
$\overline{PGM}$	= H		
I/O	= DATA TRANSFER		
$\overline{RESET}$	= H/L		
STATUS	= L/H DC−DC status: Fail/Pass?		

To make sure the data are not polluted by power losses, it

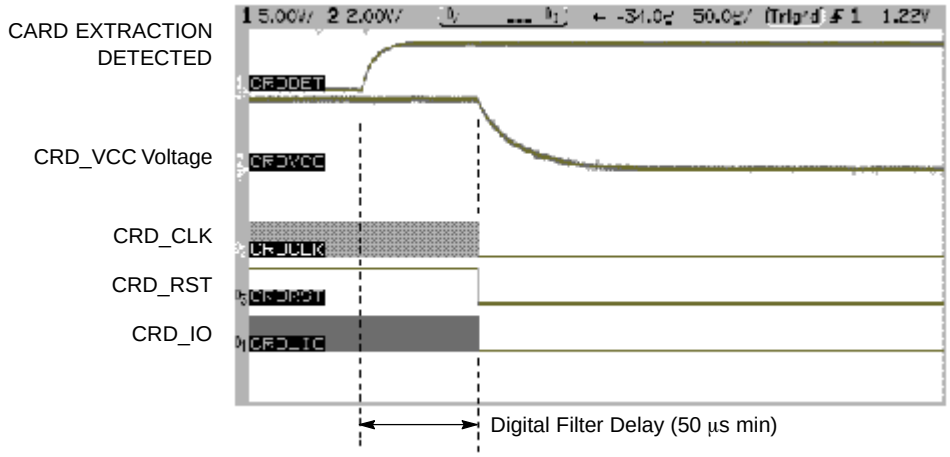


Figure 9. Typical Power Down Sequence in the NCN6000 Interface

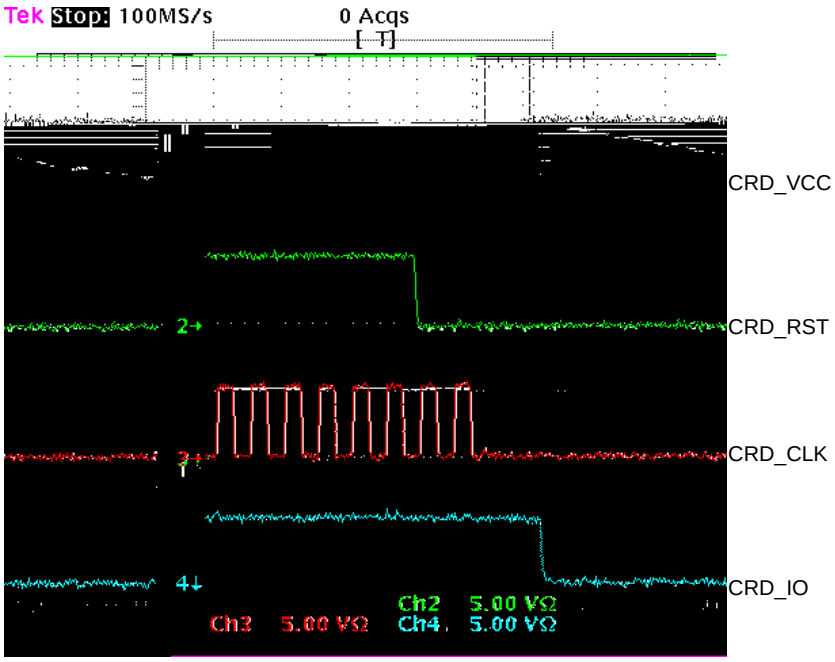


Figure 10. Power Down Sequence Details

Card Detection

The card detector circuit provides a 500 kΩ pull up resistor to bias the CRD_DET pin, yielding a logic High when the pin is left open (assuming a NO switch). The internal logic associated with pin 11 provides an automatic selection of the slope card detection, depending upon the polarity set by the external MPU. At start up, the CRD_DET is preset to cope with Normally Open switch. When a Normally Close switch is used in the card socket, it is mandatory to program the NCN6000 chip during the initialization sequence, otherwise the system will not start if a card was previously inserted. Table 3 gives the programming code for such a function. The next lines provide a typical assembler source to handle this CRD_DET

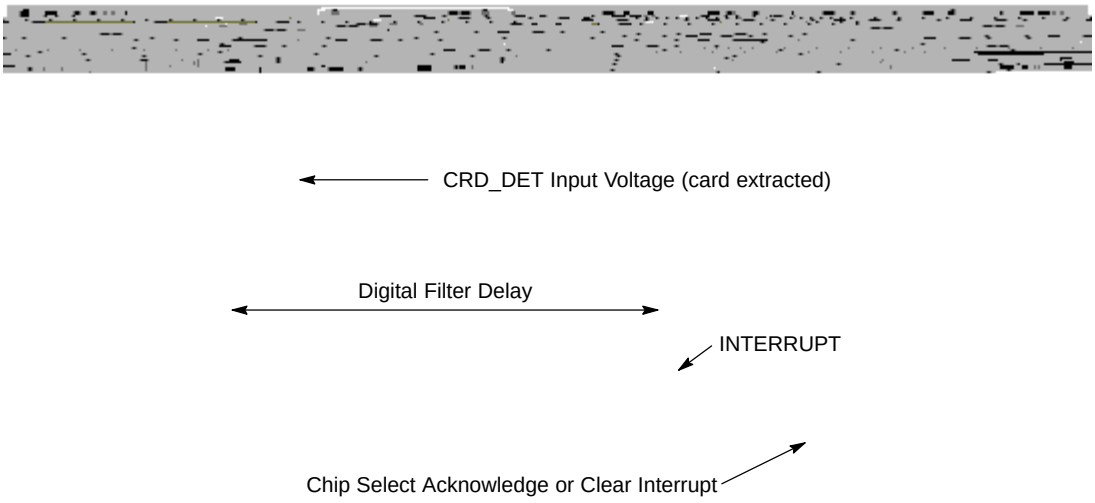


Figure 12. Card Extraction Detection and Interrupt Signals

When the card is extracted, the CRD_DET signal generates an interrupt, assuming the positive pulse width is longer than the digital filter. The oscillogram, Figure 12, depicts the behavior for a Normally Open switch.

Note: since the internal pull up resistor is relatively high (500 kΩ typical), one must use a 10 MΩ input impedance probe to read this signal.

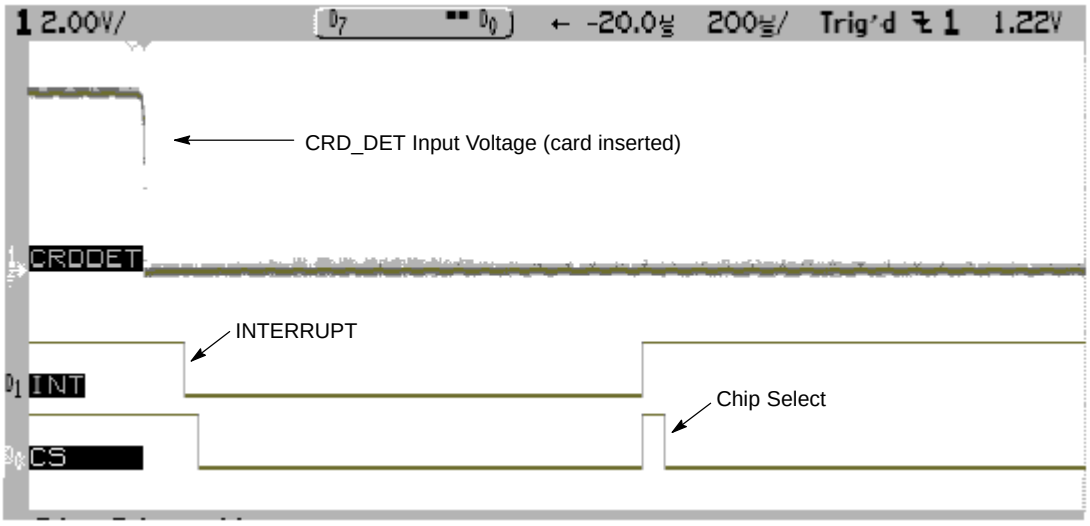


Figure 13. Interrupt Acknowledgement During a Card Insertion Detection Sequence

The interrupt signal, provided pin 9, is cleared by a positive going Chip Select signal as depicted by the oscillogram, Figure 13. The $\overline{CS}$ pulse width is irrelevant, as long as it is larger than 2.0 µs, to activate a different sequence. Leaving the interrupt signal Low has no influence on the internal behavior of the NCN6000, but will be automatically cleared when the DC−DC will be activated by the MPU ($\overline{CS}$=L, PWR_ON = Positive High transition)

Power Management

The purpose of the power management is to activate the circuit functions needed to run a given mode of operation, yielding a minimum current consumption on the Vbat supply. In the Standby mode (PWR_ON = L), the power management provides energy to the card detection circuit only. All the card interface pins are forced to ground potential.

In the event of a power up request coming from the external MPU (PWR_ON = H, $\overline{CS}$ = L), the power manager starts the DC−DC converter.

When the CRD_VCC voltage reaches the programmed value (3.0 V or 5.0 V), the circuit activates the card signals according to the following sequence:

CRD_VCC
⇒CRD_IO
⇒CRD_CLK
⇒CRD_RST

The logic level of the data lines are asserted High or Low, depending upon the state forced by the external MPU, when the start up sequence is completed. Under no situation the NCN6000 shall launch automatically a smart card ATR sequence. Assuming PWR_ON = H, the CRD_VCC voltage is maintained whatever be the logic level presents on Chip Select, pin 6.

At the end of the transaction, asserted by the MPU (PWR_ON = L, $\overline{CS}$ = L), or under a card extraction, the ISO7816−3 power down sequence takes place:

CRD_RST
⇒CRD_CLK
⇒CRD_IO
⇒CRD_VCC

When $\overline{CS}$ = H, the bi−directional I/O line (pins 8 and 15) is forced into the High impedance mode to avoid signal collision with any data coming from the external MPU.

The CRD_VCC voltage is controlled by means of $\overline{CS}$ and PWR_ON logic signal as depicted in Figure 14. The PWR_ON logic level define the CRD_VCC voltage status, the amplitude being the one pre programmed into the chip.

In order to avoid uncontrolled command applied to the smart card, the NCN6000 internal logic circuit, together with the Vbat monitoring, clamps the card outputs until the CRD_VCC voltage reaches the minimum value. During the CRD_VCC slope, all the card outputs are kept Low and no spikes can be write to the smart card. The oscillogram on the right hand side is a magnification of the curves given on the opposite side.

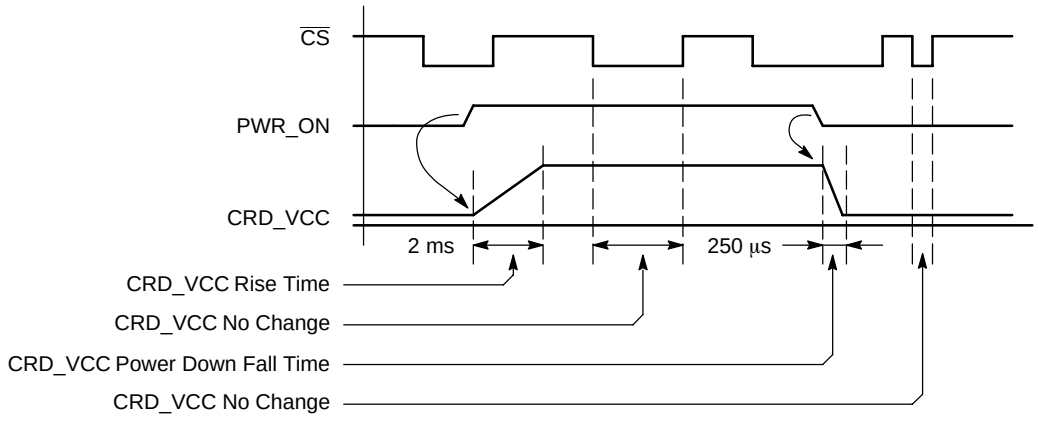


Figure 14. Card Power Supply Control

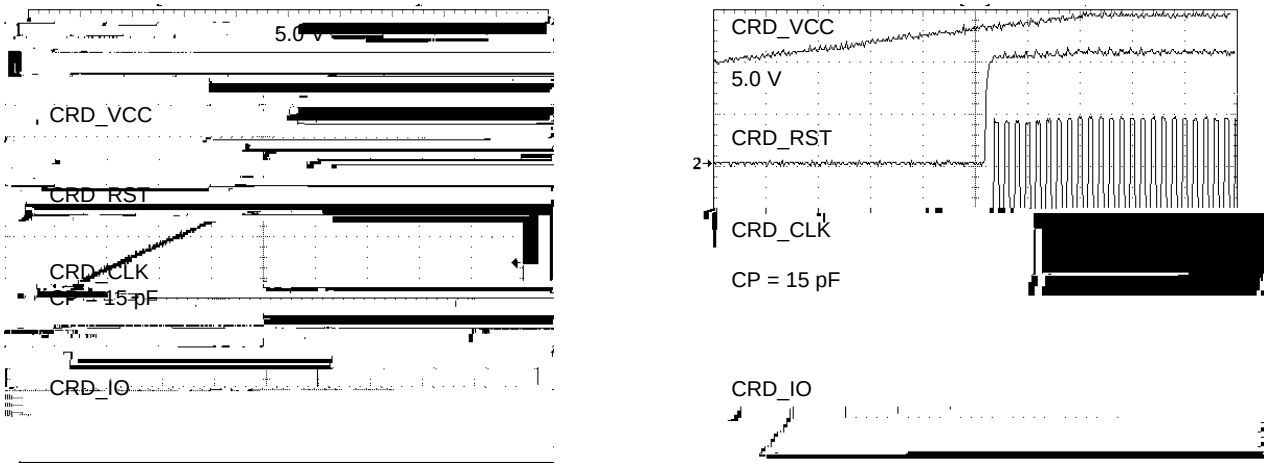


Figure 15. Smart Card Signals Sequence at Power On

Vbat Supply Voltage Monitoring

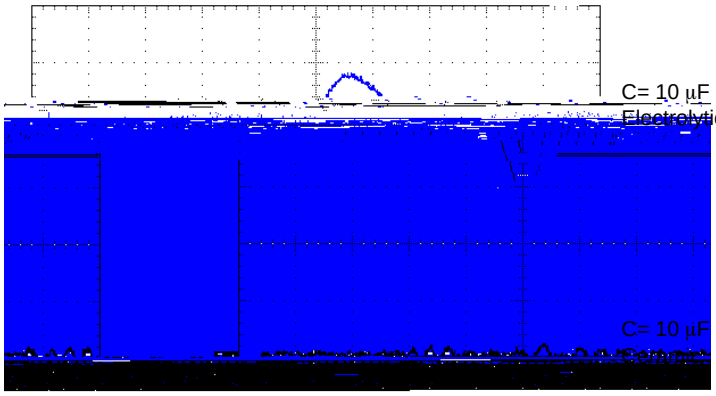
The built−in comparator, associated with the band gap reference, continuously monitors the +Vbat input. During the start up, all the NCN6000 functions are deactivated and

When the input voltage Vbat is lower than the programmed CRD_VCC, the system operates under the boost mode, providing the voltage regulation and current

Based on the experiments carried out during the NCN6000 characterization, the best comprise, at time of printing this document, is to use two 6.8 μF/10 V/Ceramic/X7R capacitor in parallel to achieve the CRD_VCC filtering. The ESR will not extend 50 mΩ over the temperature range and the combination of standard parts provide an acceptable –20% to +20% tolerance, together with a low cost. Obviously, the capacitor must be SMD type to achieve the extremely low ESR and ESL necessary for this application. Figure 21 illustrates the CRD_VCC ripple observed in the NCN6000 demo board depending upon the type of capacitor used to filter the output voltage.

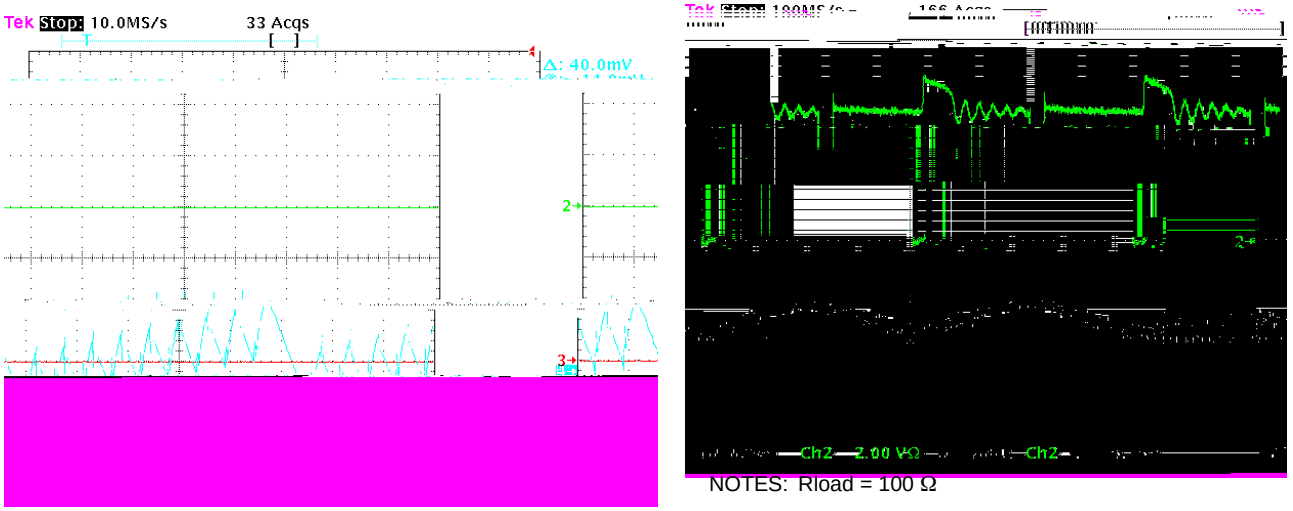
Table 5. Ceramic/Electrolytic Capacitors Comparison

Manufacturers	Type/Series	Format	Max Value	Tolerance	Typ. Z @ 500 kHz
MURATA	CERAMIC/GRM225	0805	10 μF/6.3 V	+80%/−20%	30 mΩ
VISHAY	Tantalum/594C/593C		10 μF/16 V		450 mΩ
VISHAY	Electrolytic/94SV		10 μF/10 V	−20%/+20%	400 mΩ
	Electrolytic Low Cost		10 μF/10 V	−35%/+50%	2.0 Ω



Top Trace = Electrolytic or Tantalum 10 μF
Bottom Trace = X7R 10 μF ceramic
The high ripple pulse across CRD_VCC is the consequence of the large ESR of the electrolytic capacitor.

Figure 21. CRD_VCC Ripple as a Function of the Capacitor Technology



NOTES: Rload = 100 Ω

Clock Divider

The main purpose of the built−in clock generator is threefold:

1. Adapts the voltage level shifter to cope with the different voltages that might exist between the MPU and the Smart Card.
2. Provides a frequency division to adapt the Smart Card operating frequency from the external clock source.
3. Controls the clock state according to the smart card specification.

In addition, the NCN6000 adjusts the signal coming from the microprocessor to get the Duty Cycle window as defined by the ISO7816−3 specification.

The logic input pins A0, A1, $\overline{\text{PGM}}$, I/O and $\overline{\text{RESET}}$ fulfill the programming functions when both $\overline{\text{PGM}}$ and $\overline{\text{CS}}$ are Low. The clock input stage (CLOCK_IN) can handle a 40 MHz frequency maximum, the divider being capable to provide a 1:8 ratio. Of course, the ratio must be defined by the engineer to cope with the Smart Card considered in a

The example given by the oscillogram here above highlights the delay coming from the internal clock duty cycle resynchronization. In this example, the clock is internally divided by 2 prior to be applied to the CRD_CLK pin. Since the clock signal is asynchronous, it is up to the programmer to make sure the next card transaction is not activated before the CRD_CLK signal has been updated. Generally speaking, such a delay can be derived from the maximum clock frequency provided to the interface, keeping in mind the maximum delay is eight incoming clock pulses.

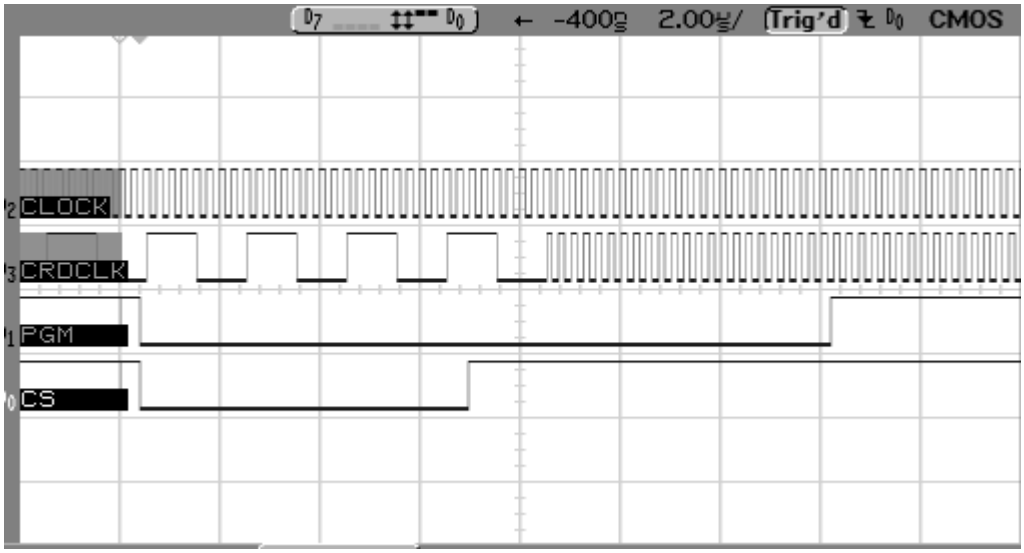


Figure 25. Clock Programming Examples

The clock can be re−programmed without halting the rest of the circuit, whatever be the new clock divider ratio. In particular, the CRD_VCC can be applied to the card while the clock is re−programmed.

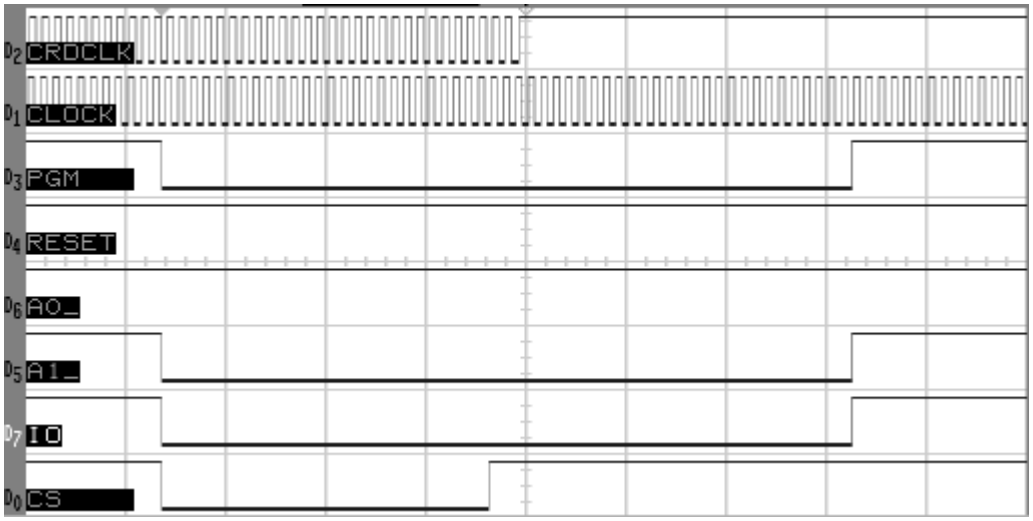


Figure 26. Command Stop Clock HIGH

The CRD_CLK signal is halted in the High logic state, following the Chip Select positive going transition. Logic Input conditions:

$\overline{\text{PGM}}$	= Low	A0	= Low
$\overline{\text{RESET}}$	= Low	A1	= Low
I/O	= Low	$\overline{\text{CS}}$	= Low pulsed

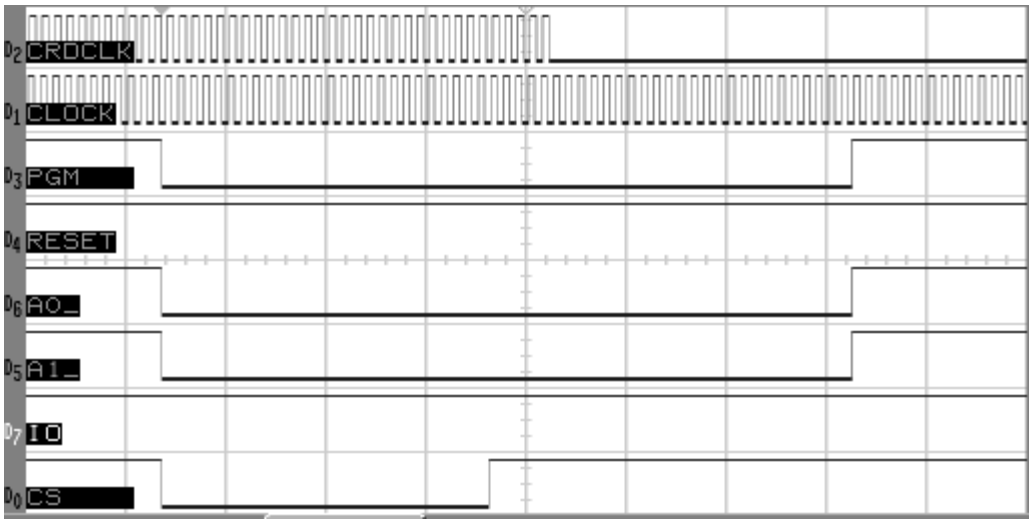


Figure 27. Command Stop Clock LOW

The CRD_CLK signal is halted in the Low logic state, following the Chip Select positive going transition. Logic Input conditions:

$\overline{\text{PGM}}$	= Low	A0	= Low
$\overline{\text{RESET}}$	= Low	A1	= Low
I/O	= High	$\overline{\text{CS}}$	= Low, pulsed

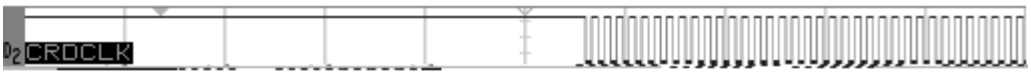


Figure 28. Command Resume Clock Normal Operation

The CRD_CLK signal is resumed in the normal operation, following the Chip Select positive going transition. The previous halted state is irrelevant and the clock signal is synchronized with the internal clock divider to avoid non CRD_CLK 50% duty cycle.

$\overline{PGM}$	= Low	A0	= Low
$\overline{RESET}$	= High	A1	= Low
I/O	= Low	$\overline{CS}$	= Low, pulsed

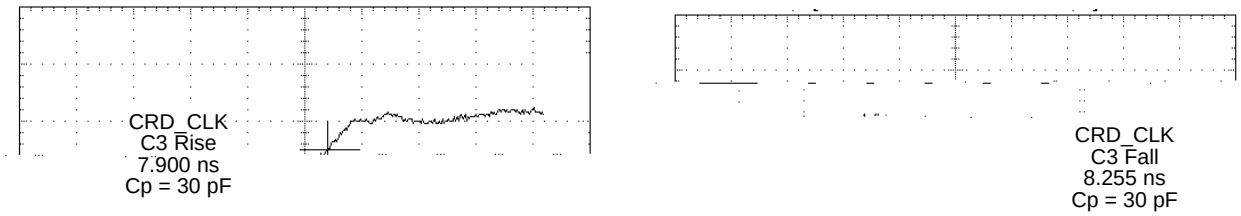


Figure 29. Card Clock Rise and Fall Time

Since the CRD_CLK signal can generate very fast transient (i.e. tr = 2.5 ns @ Cp = 10 pF), adapting the design to cope with the EMV noise specification might be necessary at final check out. Using an external RC network is a way to reduce the dv/dt, hence the EMI noise.

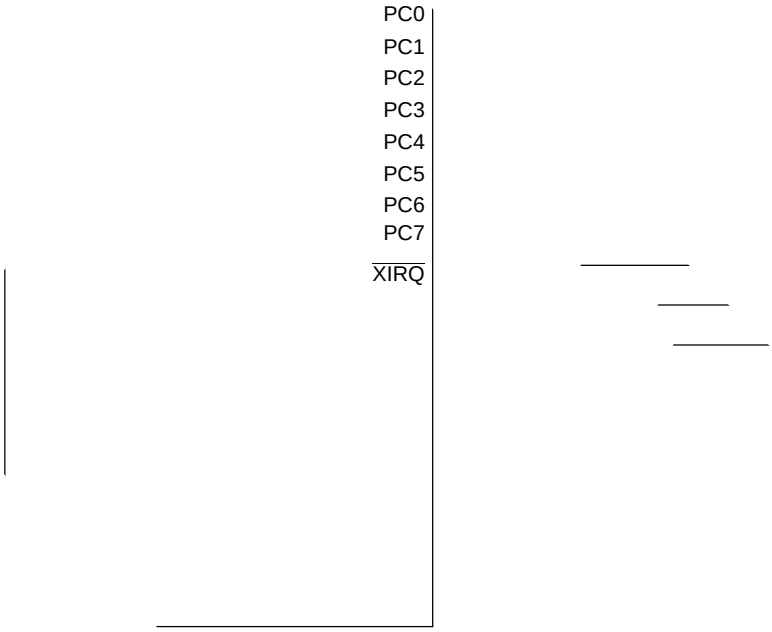
Typically, the external series resistor is 10 Ω, the total capacitance being 30 pF to 50 pF

Input Schmitt Triggers

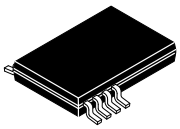
Printed Circuit Board Layout

Since the NCN6000 carries high speed currents together with

NCN6000


PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
XIRQ

NCN6000



SCALE 2:1

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