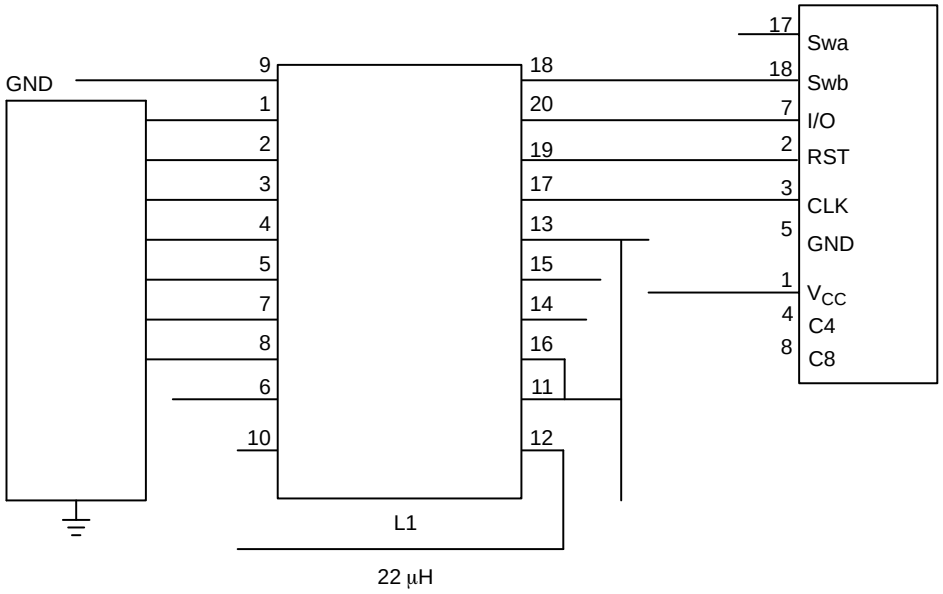
NCN6001

Compact Smart Card Interface IC

The NCN6001 is an integrated circuit dedicated to the smart card interface applications. The device handles any type of smart card through a simple and flexible microcontroller interface. On top of that, thanks to the built−in chip select pin, several couplers can be connected in parallel.

October, 2014 − Rev. 6
Publication Order Number:
NCN6001/D


GND
9
1
2
3
4
5
7
8
6
10
18
20
19
17
13
15
14
16
11
12
L1
22 μH
17
Swa
18
Swb
7
I/O
2
RST
3
CLK
5
GND
1
VCC
4
C4
8
C8

PIN FUNCTIONS AND DESCRIPTION

TSSOP	Name	Type	Description
1	I/O	Input/Output Pullup	This pin is connected to an external microcontroller interface. A bidirectional level translator adapts the serial I/O signal between the smart card and the microcontroller. The level translator is enabled when $\overline{CS}$ = L, the sub address has been selected and the system operates in the Asynchronous mode. When a Synchronous card is in use, this pin is disconnected and the data and the transaction take place with the MISO b3 register. The internal pullup resistor connected on the μC side is activated and visible by the selected chip only.
2	$\overline{INT}$	OUTPUT Pullup	This pin is activated LOW when a card has been inserted and detected by CRD_DET pin. Similarly, an interrupt is generated when the CRD_VCC output is overloaded, or when the card has been extracted whatever be the transaction status (running or standby). The $\overline{INT}$ signal is reset to High according to Table 7 and Figure 10. On the other hand, the pin is forced to a logic High when the input voltage V_{CC} drops below 2.0 V.
3	CLK_IN	CLOCK INPUT High impedance	The built−in Schmitt trigger receiver makes this pin suitable for a large type of clock signal (Figure 29). This pin can be connected to either the microcontroller master clock, or to a crystal signal, to drive the external smart cards. The signal is fed to the internal clock selector circuit and translated to the CRD_CLK pin at either the same frequency, or divided by 2 or 4, depending upon the programming mode. Note: The chip guarantees the EMV 50% Duty Cycle when the clock divider ratio is 1/2 or 1/4, even when the CLK_IN signal is out of the 45% to 55% range specified by ISO and EMV specifications. Care must be observed, at PCB level, to minimize the pick−up noise coming from the CLK_IN line.
4	MOSI	INPUT	Master Out Slave In: SPI Data Input from the external microcontroller. This byte contents the address of the selected chip among the four possible, together with the programming code for a given interface.
5	CLK_SPI	INPUT	Clock Signal to synchronize the SPI data transfer. The built−in Schmitt trigger receiver makes this pin compatible with a wide range of input clock signal (Figure 29). This clock is fully independent from the CLK_IN signal and does not play any role with the data transaction.
6	EN_RPU	INPUT, Logic	This pin is used to activate the I/O internal pullup resistor according to the here below true table: EN_RPU = Low → I/O Pullup resistor disconnected EN_RPU = High → I/O Pullup resistor connected When two or more NCN6001 chips shares the same I/O bus, one chip only shall have the internal pullup resistor enabled to avoid any overload of the I/O line. Moreover, when Asynchronous and Synchronous cards are handled by the interfaces, the activated I/O pullup resistor must preferably be the one associated with the Asynchronous circuit. On the other hand, since no internal pullup bias resistor is built in the chip, pin 6 must be connected to the right voltage level to make sure the logic function is satisfied.
7	MISO	OUTPUT	Master In Slave Out: SPI Data Output from the NCN6001. This byte carries the state of the interface, the serial transfer being achieved according to the programmed mode (Table 2), using the same CLK_SPI signal and during the same MOSI time frame. The three high bits [b7:b5] have no meaning and shall be discarded by the microcontroller. An external 4.7 kΩ Pull down resistor might be necessary to avoid misunderstanding of the pin 7 voltage during the High Z state.
8	$\overline{CS}$	INPUT	This pin synchronizes the SPI communication and provides the chip address and selected functions. All the NCN6001 functions, both programming and card transaction, are disabled when $\overline{CS}$ = H.
9	V_{CC}	POWER	This pin is connected to the NCN6001 supply voltage and must be bypassed to ground by a 10 μF/6.0 V capacitor. Since tantalum capacitors have relative high ESR, using low ESR ceramic type (MURATA X5R, Resr < 100 mΩ) is highly recommended.
10	Lout_L	POWER	

PIN FUNCTIONS AND DESCRIPTION (continued)

TSSOP	Name	Type	Description
11	PWR_GND	POWER	This pin is the Power Ground associated with the built−in DC/DC converter and must be connected to the system ground together with GROUND pin 16. Using good quality ground plane is recommended to avoid spikes on the logic signal lines.
12	Lout_H	POWER	The High Side of the external inductor is connected between this pin and pin 10 to activate the DC/DC function. The built−in NMOS and PMOS devices provide the switching function together with the CRD_VCC voltage rectification (Figure 16).
13	CRD_VCC	POWER	This pin provides the power to the external card. It is the logic level “1” for CRD_IO, CRD_RST, CRD_C4, CRD_C8 and CRD_CLK signals. The energy stored by the DC/DC external inductor Lout must be smoothed by a 10 μF/Low ESR capacitor, connected across CRD_VCC and GND. Using ceramic type of capacitor (MURATA X5R, ESR < 50 mΩ) is strongly recommended. In the event of a CRD_VCC U_{VLOW} voltage, the NCN6001 detects the situation and feedback the information in the STATUS bit. The device does not take any further action, particularly the DC/DC converter is neither stopped nor re programmed by the NCN6001. It is up to the external MPU to handle the situation. However, when the CRD_VCC is overloaded, the NCN6001 shuts off the DC/DC converter, runs a Power Down ISO sequence and reports the fault in the STATUS register. Since high transient current flows from this pin to the load, care must be observed, at PCB level, to minimize the series ESR and ESL parasitic values. The NCN6001 demo board provides an example of a preferred PCB layout.
14	C8/S1	I/O	Auxiliary mixed analog/digital line to handle either a synchronous card, or as Chip Select Identification (MISO, Bit 0): see Figure 8. The pin is driven by an open drain stage, the pullup resistor being connected to the CRD_VCC supply. When the pin is used as a logic input (asynchronous cards), the positive logic condition applies: Connected to GND → Logic = Zero Connected to V_{CC} or left Open → Logic = One A built−in accelerator circuit makes sure the output positive going rise time is fully within the ISO/EMV specifications. NOTE: The pin is capable of reading the logic level when the chip operates an asynchronous interface, but is not intended to read the data from the external card when operated in the synchronous mode. It merely returns the logic state forced during a write instruction to the card.
15	C4/S0	I/O	Auxiliary mixed analog/digital line to handle either a synchronous card, or as Chip Select Identification (MISO, Bit 1): see Figure 8. The pin is driven by an open drain stage, the pullup resistor being connected to the CRD_VCC supply. When the pin is used as a logic input (asynchronous cards), the positive logic condition applies: Connected to GND → Logic = Zero Connected to V_{CC} or left Open → Logic = One A built−in accelerator circuit makes sure the output positive going rise time is fully within the ISO/EMV specifications. NOTE: The pin is capable of reading the logic level when the chip operates an asynchronous interface, but is not intended to read the data from the external card when operated in the synchronous mode. It merely returns the logic state forced during a write instruction to the card.
16	GND	SIGNAL	The logic and low level analog signals shall be connected to this ground pin. This pin must be externally connected to the PWR_GND pin 12. The designer must make sure no high current transients are shared with the low signal currents flowing into this pin.
17	CRD_CLK	OUTPUT	This pin is connected to the CLK pin of the card connector. The CRD_CLK signal comes from the clock selector circuit output. An internal active pull down NMOS device forces this pin to Ground during either the CRD_VCC startup sequence, or when CRD_VCC = 0 V. The rise and fall slopes, either FAST or SLOW, of this signal can be programmed by the MOSI message (Table 2). Care must be observed, at PCB level, to minimize the pick−up noise coming from the CRD_CLK line.

PIN FUNCTIONS AND DESCRIPTION (continued)

TSSOP	Name	Type	Description
18	CRD_DET	INPUT	The signal coming from the external card connector is used to detect the presence of the card. A built−in pullup low current source biases this pin High, making it active LOW, assuming one side of the external switch is connected to ground. A built−in digital filter protect the system against voltage spikes present on this pin. The polarity of the signal is programmable by the MOSI message, according to the logic state depicted Table 2. On the other hand, the meaning of the feedback message contained in the MISO register bit b4, depends upon the SPI mode of operation as defined here below: SPI Normal Mode: The MISO bit b4 is High when a card is inserted, whatever be the polarity of the card detect switch. SPI Special Mode: The MISO bit b4 copies the logic state of the Card detect switch as depicted here below, whatever be the polarity of the switch used to handle the detection: CRD_DET = Low $\rightarrow$ MISO/b4 = Low CRD_DET = High $\rightarrow$ MISO/b4 = High In both cases, the chip must be programmed to control the right logic state (Table 2). Since the bias current supplied by the chip is very low, typically 5.0 μA, care must be observed to avoid low impedance or cross coupling when this pin is in the Open state.
19	CRD_RST	OUTPUT	This pin is connected to the RESET pin of the card connector. A level translator adapts the RESET signal from the microcontroller to the external card. The output current is internally limited to 15 mA. The CRD_RST is validated when $\overline{CS}$ = Low and hard wired to Ground when the card is deactivated, by and internal active pull down circuit. Care must be observed, at PCB design level, to avoid cross coupling between this signal and the CRD_CLK clock.
20	CRD_IO	I/O Pullup	This pin handles the connection to the serial I/O pin of the card connector. A bidirectional level translator adapts the serial I/O signal between the card and the microcontroller. An internal active pull down MOS device forces this pin to Ground during either the CRD_VCC startup sequence, or when CRD_VCC = 0 V. The CRD_IO pin current is internally limited to 15 mA. Care must be observed, at PCB design level, to avoid cross coupling between this signal and the CRD_CLK clock.

DIGITAL PARAMETERS @ 2.7 V < V_{CC} < 5.5 V (−25°C to +85°C ambient temperature, unless otherwise noted).
Note: Digital inputs undershoot < − 0.3 V to ground, Digital inputs overshoot < 0.3 V to V_{CC}.

Rating	Pin	Symbol	Min	Typ	Max	Unit
Input Asynchronous Clock Duty Cycle = 50% @ V_{CC} = 3.0 V Over the Temperature Range @ V_{CC} = 5.0 V Over the Temperature Range	3	F_{CLKIN}	 − −	 − −	 30 40	MHz
Input Clock Rise Time						
Input Clock Fall Time						

POWER SUPPLY @ 2.7 V < V_{CC} < 5.5 V (−25°C to +85°C ambient temperature, unless otherwise noted).

Rating	Pin	Symbol	Min	Typ	Max	Unit
Input Power Supply	9	V_{CC}	2.70	−	5.50V	V
Standby Supply Current Conditions: $\overline{INT}$ = CLK_IN = CLK_SPI = $\overline{CS}$ = H I/O = MOSI = EN_RPU = H, No Card Inserted V_{CC} = 3.0 V V_{CC} = 5.0 V	9	ICC_{sb}	 − −	 25 35	 50 60	μA
DC Operating Current CLK_IN = Low, All Card Pins Unloaded @ V_{CC} = 3.3 V, CRD_VCC = 5.0 V @ V_{CC} = 5.5 V, CRD_VCC = 5.0 V	9	ICC_{op}	 − −	 − −	 0.5 1.5	mA
V_{CC} Under Voltage Detection$_{High}$ V_{CC} Under Voltage Detection$_{Low}$ V_{CC} Under Voltage (Note 6)	9	VCC_{LH} VCC_{LL} VCC_{POR}	2.20 2.00 1.50	− − −	2.70 2.60 2.20	V
Output Card Supply Voltage @ 2.7 V < V_{CC} < 5.5 V CRD_VCC = 1.8 V @ Iload = 35 mA CRD_VCC = 3.0 V @ Iload = 60 mA CRD_VCC = 5.0 V @ Iload = 65 mA	13	 V_{C2H} V				

SMART CARD INTERFACE @ 2.7 V < V_{CC} < 5.5 V (−25°C to +85°C ambient temperature, unless otherwise noted).
Note: Digital inputs undershoot < −0.3 V to ground, Digital inputs overshoot < 0.3 V to V_{CC}.

Rating	Pin	Symbol	Min	Typ	Max	Unit

PROGRAMMING

Write Register → WRT_REG

The WRT_REG register handles three command bits [b5:b7] and five data bits [b0:b4] as depicted in Table 1.

Table 2. WRT_REG BITS DEFINITIONS AND FUNCTIONS

ADDRESS				PARAMETERS							
CHIP BANK									MOSI bits [b3:b2]	MOSI bits [b1:b0]	MOSI bits [b7:b0]
1	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**	CRD_CLK	CRD_VCC	CRD_DET
1	0	X	X	RST	0	0	0	0	Low	0	−
1	0	X	X	RST	0	1	0	1	1/1	1.8 V	−
1	0	X	X	RST	1	0	1	0	1/2	3.0 V	−
1	0	X	X	RST	1	1	1	1	1/4	5.0 V	−
1	1	0	1	0	0	0	0	0	−	−	NO
1	1	0	1	0	0	0	0	1	−	−	NC
1	1	0	1	0	0	0	1	0	−	−	Special
1	1	0	1	0	0	0	1	1	−	−	Normal
1	1	0	1	0	0	1	0	0	−	−	SLO_SLP
1	1	0	1	0	0	1	0	1	−	−	FST_SLP
1	1	1	1	−	−	−	−	−	−	−	RFU
2	1	0	0	RST	0	0	0	0	Low	0	−
2	1	0	0	RST	0	1	0	1	1/1	1.8 V	−
2	1	0	0	RST	1	0	1	0	1/2	3.0 V	−
2	1	0	0	RST	1	1	1	1	1/4	5.0 V	−
2	1	1	0	RST	CLK	I/O	C4	C8	−	−	Data to Sync. Card
2	1	0	1	0	0	0	0	0	−	−	NO
2	1	0	1	0	0	0	0	1	−	−	NC
2	1	0	1	0	0	0	1	0	−	−	Special
2	1	0	1	0	0	0	1	1	−	−	Normal
2	1	0	1	0	0	1	0	0	−	−	SLO_SLP
2	1	0	1	0	0	1	0	1	−	−	FST_SLP
2	1	1	1	−	−	−	−	−	−	−	RFU

11. Chip Bank 1 = Asynchronous cards, four slots addresses 1 to 4.
    Chip Bank 2 = Asynchronous or synchronous card, single slot.
12. Address 101 and bits [b0 : b4] not documented in the table are reserved for future use.
    Address 111 is reserved for future use.

Although using the %111XXXXX code is harmless from a NCN6001 silicon standpoint, care must be observed to avoid uncontrolled operation of the interface sharing the same digital bus. When this code is presented on the digital bus, the CRD_RST signal of any interface sharing the $\overline{CS}$ signal, immediately reflects the digital content of the MOSI bit b4 register. Similarly, the MISO register of the shared interface is presented on the SPI port. Consequently, data collision, at MISO level, and uncontrolled card operation are likely to happen if the system uses a common Chip Select line. It is strongly recommended to run a dedicated $\overline{CS}$ bit to any external circuit intended to use the $111xxxxx code.

On the other hand, the CRD_RST signal will be forced to Low when the internal register of the chip is programmed to accommodate different hardware conditions (NO/NC, Special/Normal, SLO_SLP/FST_SLP). Generally speaking, such a configuration shall take place during the Power On Reset to avoid CRD_RST activation.

STARTUP DEFAULT CONDITIONS

At startup, when the V_{CC} power supply is turned on, the internal POR circuit sets the chip in the default conditions as defined in Table 4.

Table 4. STARTUP DEFAULT CONDITIONS

CRD_DET

At powerup, the CRD_VCC voltage rise time depends upon the current capability of the DC/DC converter associated with the external inductor L1 and the reservoir capacitor connected across CRD_VCC and GROUND. During this sequence, the average input current is 300 mA typical (Figure 3), assuming the system is fully loaded during the startup. Finally, the application software is responsible for the smart card signal sequence.

On the other hand, at turn off, the CRD_VCC fall time depends upon the external reservoir capacitor and the peak current absorbed by the internal NMOS transistor built across CRD_VCC and GROUND. These behaviors are depicted in Figure 4.

Since these parameters have finite values, depending upon the external constraints, the designer must take care of these limits if the t_{ON} or the t_{OFF} provided by the data sheets

POWER DOWN SEQUENCE

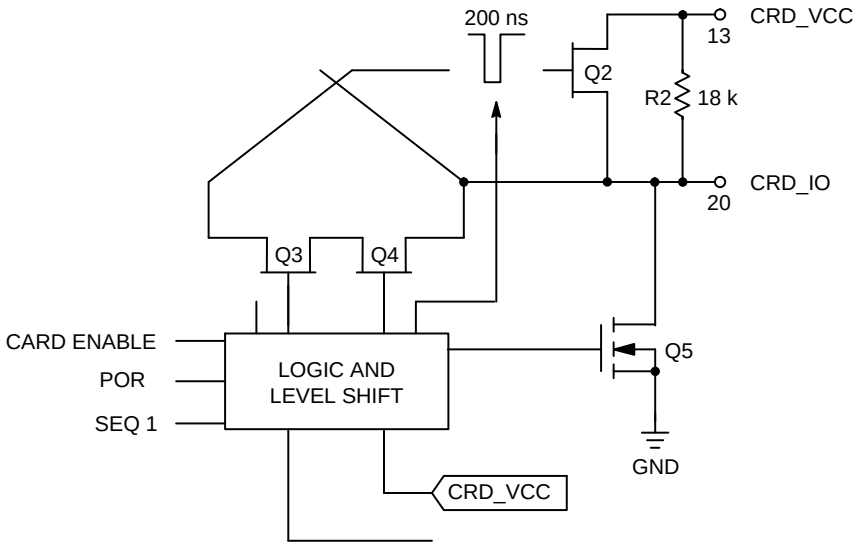
The NCN6001 provides an automatic Power Down sequence, according to the ISO7816−3 specifications, and the communication session terminates immediately. The sequence is launched when the card is extracted, or when the CRD_VCC voltage is overloaded as described by the ISO/CEI 7816−3 sequence depicted hereafter:

ISO7816−3 sequence:
→Force RST to Low
→Force CLK to Low, unless it is already in this state
→Force C4 & C8 to Low
→Force CRD_IO to Low
→Shut Off the CRD_VCC supply

Since the internal digital filter is activated for any card insertion or extraction, the physical power sequence will be activated 50 μs (typical) after the card has been extracted. Of course, such a delay does not exist when the MPU intentionally launches the power down. Figure 6 shows the oscillogram captured in the NCN6001 demo board.

DATA I/O LEVEL SHIFTER

The level shifter accommodates the voltage difference that might exist between the microcontroller and the smart card. A pulsed accelerator built−in circuit provides the fast positive going transient according to the ISO7816−3 specifications. The basic I/O level shifter is depicted in Figure 7.



GENERAL PURPOSE CRD_C4 AND CRD_C8

These two pins can be used as a logic input to define the address of a given interface (in the range $00 to $11), or as a standard C4/C8 access to the smart card's channels. Since these pins can be directly connected to the V_{CC} power supply, both output stages are built with switched NMOS/PMOS totem pole as depicted in Figure 9.

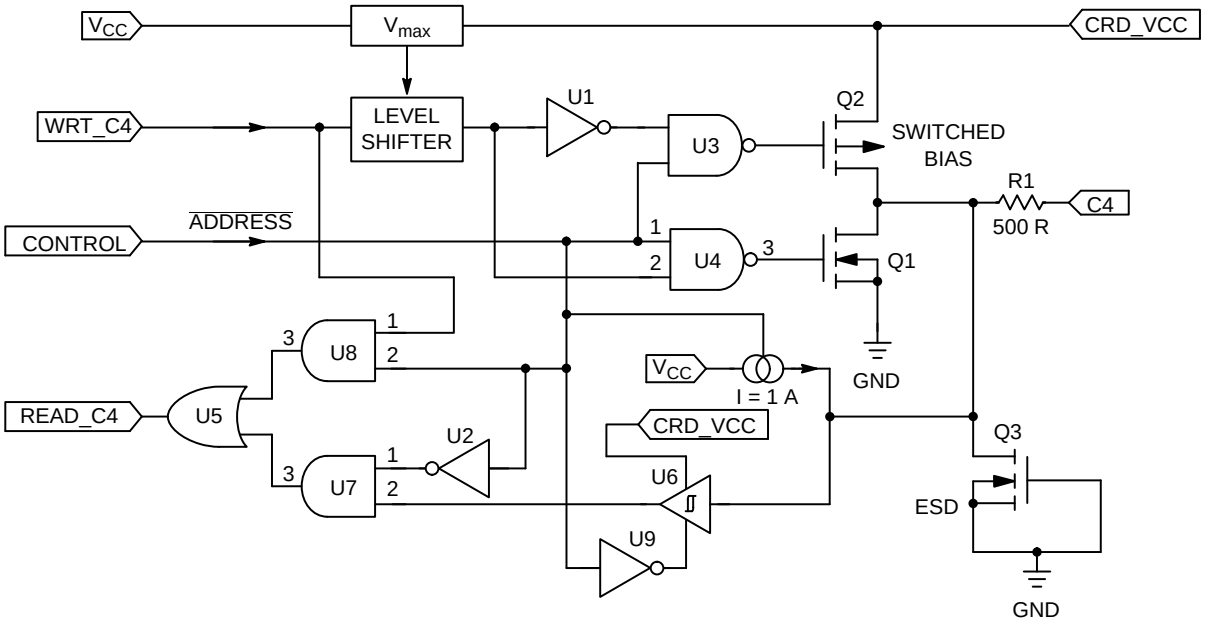


Figure 9. Typical CRD_C4 Output Drive and Logic Control

The C4 and C8 pins are biased by an internal current source to provide a logic one when the pin is left open. In this case, care must be observed to avoid relative low impedance to ground to make sure the pin is at a High logic level. However, it is possible to connect the pin to V_{CC} (battery supply) to force the logic input to a High level, regardless of the input bias. Thanks to the CONTROL internal signal, the system automatically adapts the mode of operation (chip address or data communication) and, except the leakage, no extra current is drawn from the battery to bias these pins when the logic level is High.

When any of these pins is connected to GND, a continuous 1 μA typical sink current will be absorbed from the battery supply.

The switched Totem Pole structure provides the fast positive going transient when the related pin is forced to the High state during a data transfer. In the event of a low impedance connected across C4 or C8 to ground, the current flow is limited to 15 mA, according to the ISO7816−3 specification.

The two general purpose pins can transfer data from the external microcontroller to the card and read back the logic state, but none of these pins can read the data coming from the external smart card. On the other hand, both C4 and C8 can read input logic, hence the physical address of a given chip.

In order to sustain the 8 kV ESD specified for these pins, an extra protection structure Q3 has been implemented to protect the MOS gates of the input circuit.

INTERRUPT

When

SPI PORT

The product communicates to the external microcontroller by means of a serial link using a Synchronous Port Interface protocol, the CLK_SPI being Low or High during the idle state. The NCN6001 is not intended to operate as a Master controller, but execute commands coming from the MPU.

The CLK_SPI, the $\overline{CS}$ and the MOSI signals are under the microcontroller's responsibility. The MISO signal is generated by the NCN6001, using the CLK_SPI and $\overline{CS}$ lines to synchronize the bits carried out by the data byte. The basic timings are given in Figure 11 and Figure 12. The system runs with two internal registers associated with the MOSI and MISO data:

WRT_REG is a write only register dedicated to the MOSI data.

READ_REG is a read only register dedicated to the MISO data.

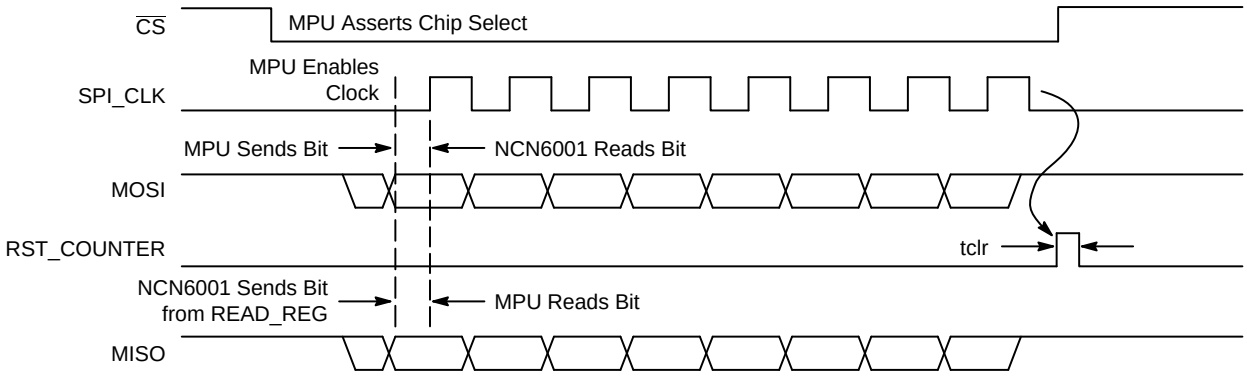


Figure 11. Basic SPI Timings and Protocol

When the $\overline{CS}$ line is High, no data can be written or read on the SPI port. The two data lines becomes active when $\overline{CS}$ = Low, the internal shift register is cleared and the communication is synchronized by the negative going edge of the $\overline{CS}$ signal. The data present on the MOSI line is considered valid on the negative going edge of the CLK_SPI clock and is transferred to the shift register on the next positive edge of the same CLK_SPI clock.

To accommodate the simultaneous MISO transmit, an internal logic identifies the chip address on the fly (reading and decoding the three first bits) and validates the right data present on the line. Consequently, the data format is MSB first to read the first three signal as bits B5, B6 and B7. The chip address is decoded from this logic value and validates the chip according to the C4 and C8 conditions (Figure 12).

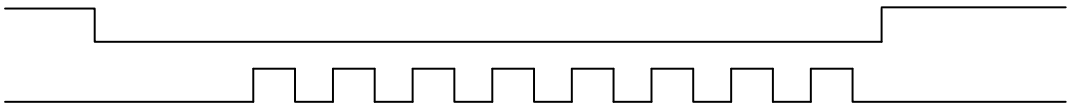


Figure 12. Chip Address Decoding Protocol and MISO Sequence

When the eight bits transfer is completed, the content of the internal shift register is latched on the positive going edge of the $\overline{CS}$ signal and the NCN6001 related functions are updated accordingly.

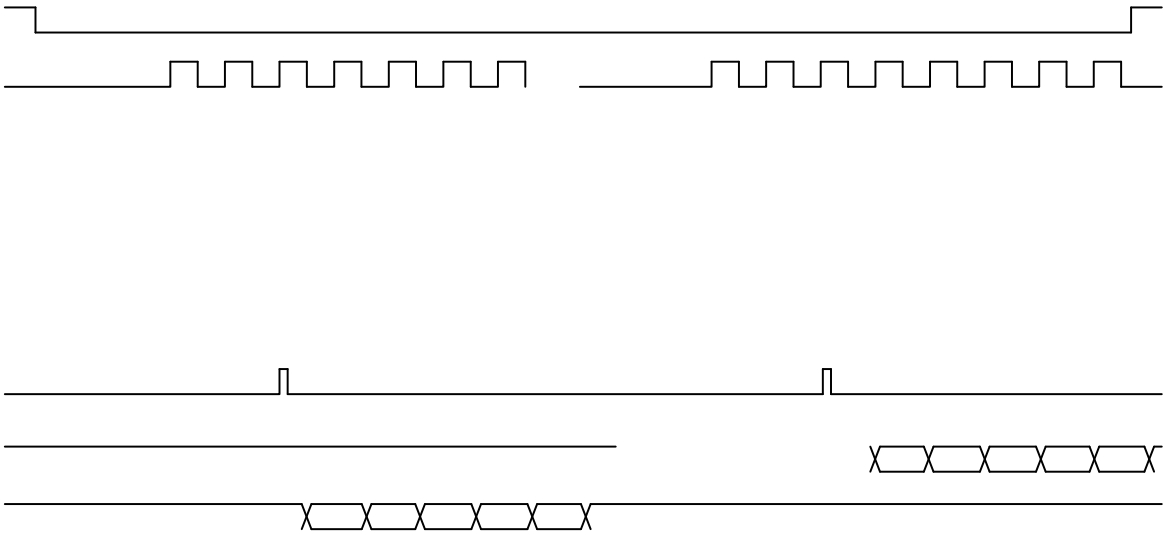


Figure 13. Basic Multi Command SPI Bytes

Protocol: Special Mode

Protocol: Standard SPI

Figure 15. MISO Read Out Sequences

DC/DC OPERATION

The power conversion is based on a full bridge structure capable to handle either step up or step down power supply (Figure 16). The operation is fully automatic and, beside the output voltage programming, does not need any further adjustments.

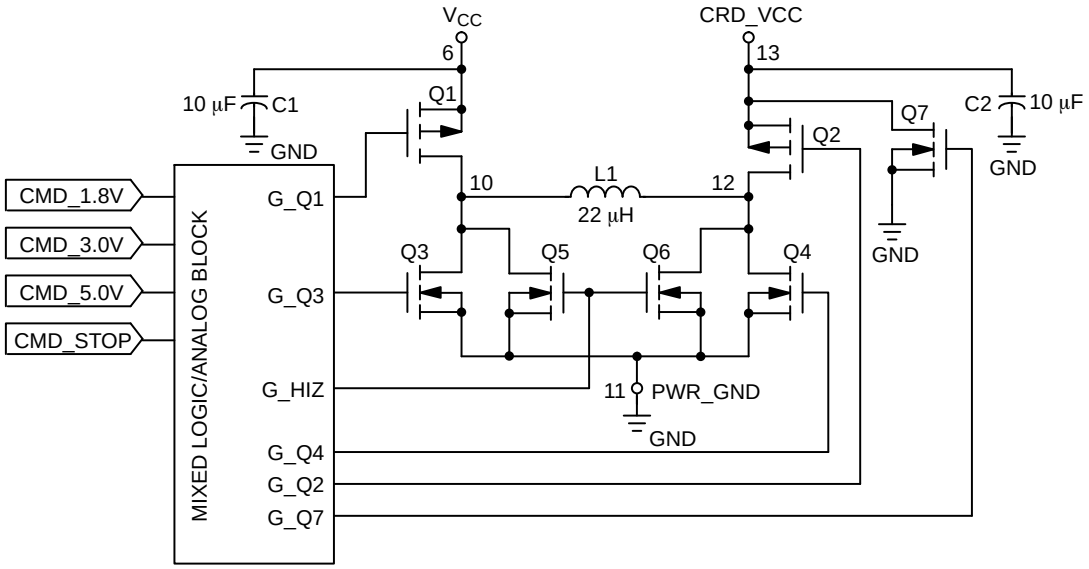


Figure 16. Basic DC/DC Converter

In order to achieve the 250 μs max time to discharge CRD_VCC to 400 mV called by the EMV specifications, an active pull down NMOS is provided (Q7) to discharge the external CRD_VCC reservoir capacitor. This timing is guaranteed for a 10 μF maximum load reservoir capacitor value (Figure 4).

The system operates with a two cycles concept (all comments are referenced to Figure 16 and Figure 17):

1 − Cycle 1 Q1 and Q4 are switched ON and the inductor L1 is charged by the energy supplied by the external battery. During this phase, the pair Q2/Q3 and the pair Q5/Q6 are switched OFF.

The current flowing the two MOSFET Q1 and Q4 is internally monitored and will be switched OFF when the Ipeak value (depending upon the programmed output voltage value) is reached. At this point, Cycle 1 is completed and Cycle 2 takes place. The ON time is a function of the battery voltage and the value of the inductor network (L and Zr) connected across pins 10/11.

A 4 μs timeout structure ensures the system does run in a continuous Cycle 1 loop

2 − Cycle 2 Q2 and Q3 are switched ON and the energy stored into the inductor L1 is dumped into the external load through Q2. During this phase, the pair Q1/Q4 and the pair Q5/Q6 are switched OFF.

The current flow period is constant (900 ns typical) and Cycle 1 repeats after this time if the CRD_VCC voltage is below the specified value.

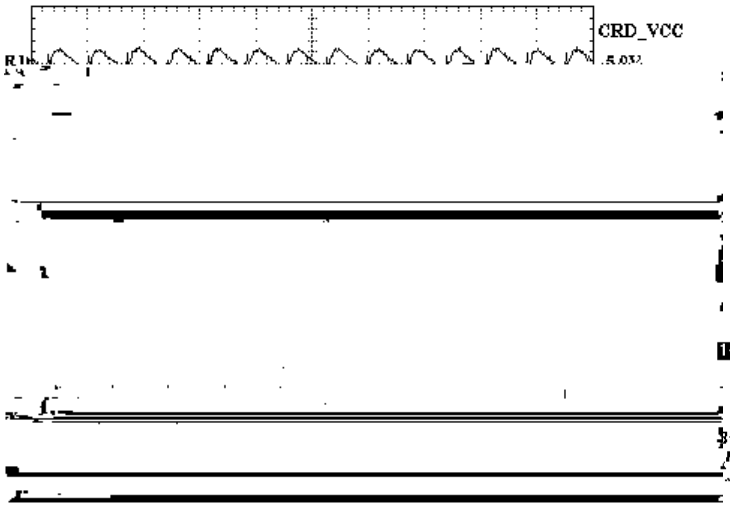
When the output voltage reaches the specified value (1.8 V, 3.0 V or 5.0 V), Q2 and Q3 are switched OFF immediately to avoid over voltage on the output load. In the meantime, the two extra NMOS Q5 and Q6 are switched ON to fully discharge any current stored into the inductor, avoiding ringing and voltage spikes over

Table 9. CERAMIC/ELECTROLYTIC CAPACITORS COMPARISON

Manufacturers	Type/Series	Format	Max Value	Tolerance	Typ. Z @ 500 kHz
MURATA	CERAMIC/GRM225	0805	10 μF/6.3 V	−20%/+20%	30 mΩ
MURATA	CERAMIC/GRM225	0805	4.7 μF/6.3 V	−20%/+20%	30 mΩ
VISHAY	Tantalum/594C/593C	−	10 μF/16 V	−	450 mΩ
VISHAY	Electrolytic/94SV	−	10 μF/10 V	−20%/+20%	400 mΩ
−	Electrolytic Low Cost	−	10 μF/10 V	−35%/+50%	2.0 Ω

The DC/DC converter is capable to start with a full load connected to the CRD_VCC output as depicted in Figure 19.

In this example, the converter is fully loaded when the system starts from zero.



Test Conditions: Cout = 2x 4.7 μF/6 V/ceramic X7R,
Temp = +25°C
Iout = Maximum Specification

Figure 18. Typical CRD_VCC Ripple Voltage

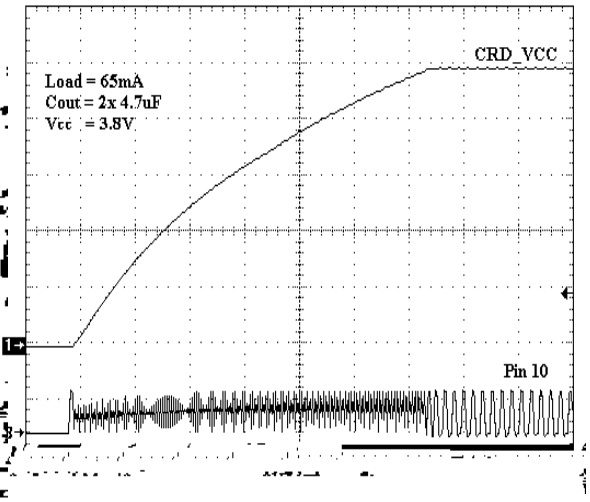
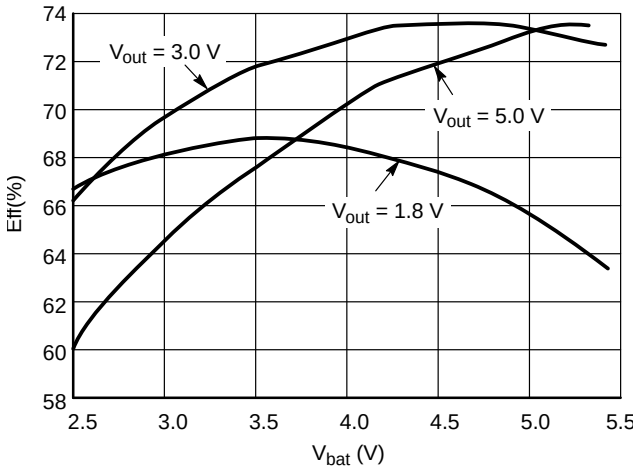


Figure 19. Output Voltage Startup Under Full Load Conditions



L_{out} = 22 μH/ESR = 2 Ω

Figure 20. CRD_VCC Efficiency as a Function of the Input Supply Voltage

The curves illustrate the typical behavior under full output current load (35 mA, 60 mA and 65 mA), according to EMV specifications.

NCN6001

The input clock can be divided by 1/1, ½ or , depending upon the specific application, prior to be applied to the smart card driver. On the other hand, the positive and negative going slopes of the output clock (CRD_CLK) can be programmed to optimize the operation of the chip (Table 10). The slope of the output clock can be programmed on the fly, independently of either the CRD_VCC voltage or the operating frequency, but care must be observed as the CRD_RST will reflect the logic state present at MOSI/b4 register.

Table 10. OUTPUT CLOCK RISE AND FALL TIME SELECTION

B0	B1	CRD_CLK Division Ratio	CRD_CLK SLO_SLP	CRD_CLK FST_SLP
0	0	–	Output Clock = Low	Output Clock = Low
0	1	1	10 ns (typ.)	2 ns (typ.)
1	0	1/2	10 ns (typ.)	2 ns (typ.)
1	1	1/4	10 ns (typ.)	2 ns (typ.)

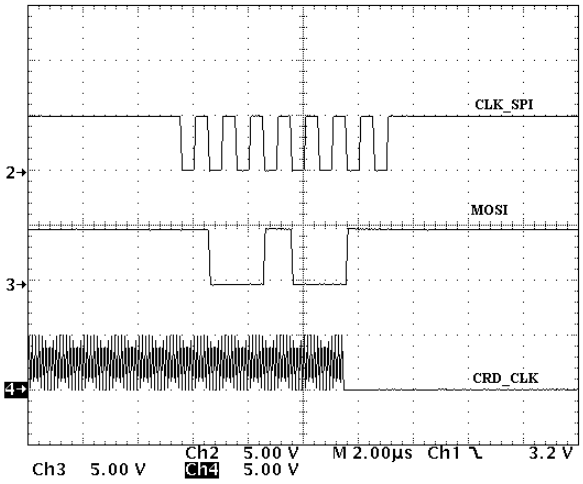


Figure 26. Force CRD_CLK to Low

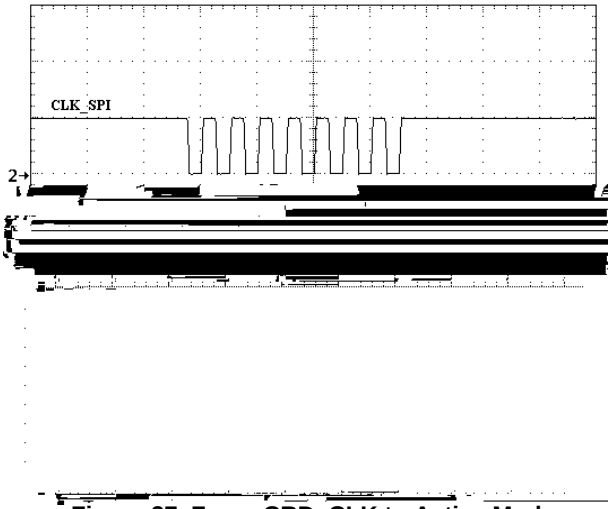


Figure 27. Force CRD_CLK to Active Mode

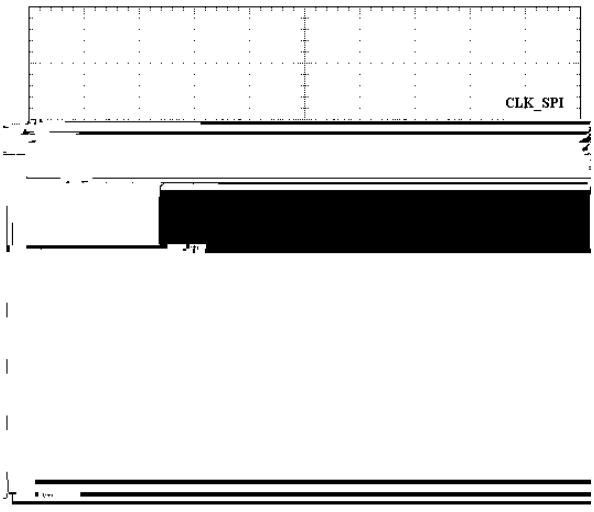
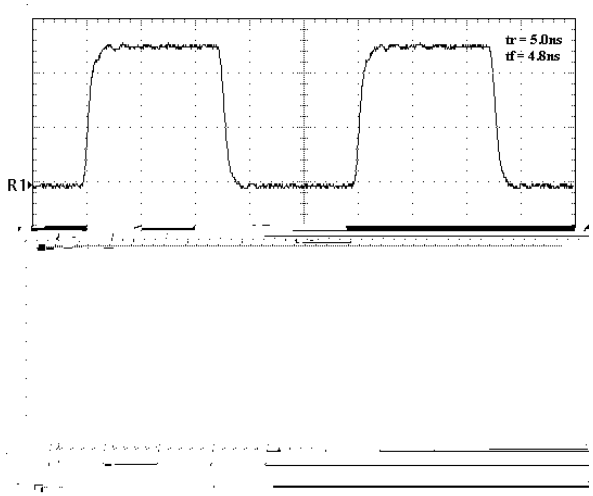


Figure 28. CRD_CLK Programming



Note: Waveforms recorded without external compensation network.

Figure 29. CRD_CLK Operating Low Speed (Top Trace), Full Speed (Bottom Trace)

INPUT SCHMITT TRIGGERS

All the Logic Input pins have built−in Schmitt trigger circuits to protect the NCN6001 against uncontrolled operation. The typical dynamic characteristics of the related pins are depicted in Figure 30.

The output signal is guaranteed to go High when the input voltage is above 0.70* V_{CC}, and will go Low when the input voltage is below 0.30* V_{CC}.

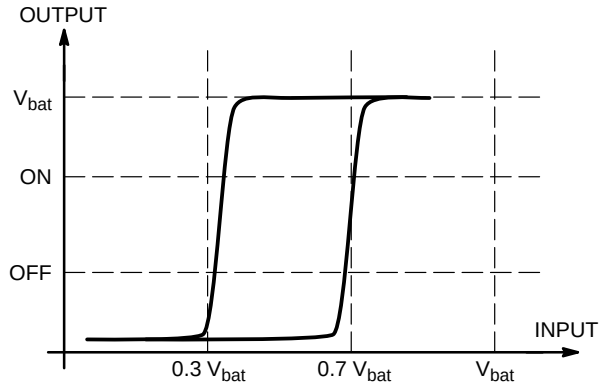


Figure 30. Typical Schmitt Trigger Characteristic

SECURITY FEATURES

In order to protect both the interface and the external smart card, the NCN6001 provides security features to prevent catastrophic failures as depicted hereafter.

Pin Current Limitation: In the case of a short circuit to ground, the current forced by the device is limited to 15 mA for any pins, except CRD_CLK pin. No feedback is provided to the external MPU.

DC/DC Operation: The internal circuit continuously senses the CRD_VCC voltage and, in the case of either over or under voltage situation, updates the READ_REG register accordingly and forces $\overline{INT}$ pin to Low. This register can be read out by the MPU.

Battery Voltage: Both the over and under voltage are detected by the NCN6001, the READ_REG register being updated accordingly. The external MPU can read the register through the MISO pin to take whatever is appropriate to cope with the situation.

ESD PROTECTION

The NCN6001 includes silicon devices to protect the pins against the ESD spikes voltages. To cope with the different ESD voltages developed across these pins, the built−in structures have been designed to handle either 2.0 kV, when related to the microcontroller side, or 8.0 kV when connected with the external contacts. Practically, the CRD_RST, CRD_CLK, CRD_IO, CRD_C4, and CRD_C8 pins can sustain 8.0 kV, the maximum short circuit current being limited to 15 mA. The CRD_VCC pin has the same ESD protection, but can source up to 65 mA continuously, the absolute maximum current being internally limited to 150 mA.

PRINTED CIRCUIT BOARD LAYOUT

Since the NCN6001 carries high speed currents together with high frequency clock, the printed circuit board must be carefully designed to avoid the risk of uncontrolled operation of the interface.

A typical single sided PCB layout is provided in Figure 32 highlighting the ground technique. Dual face printed circuit board may be necessary to solve ringing and cross talk with the rest of the system.

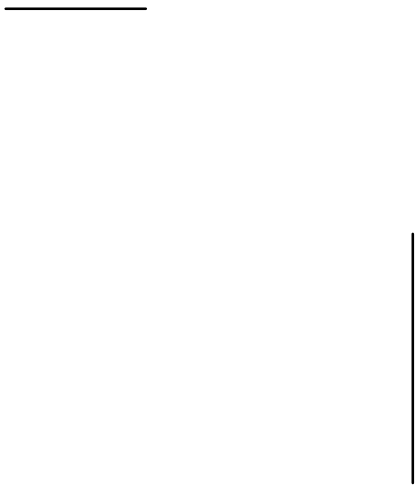
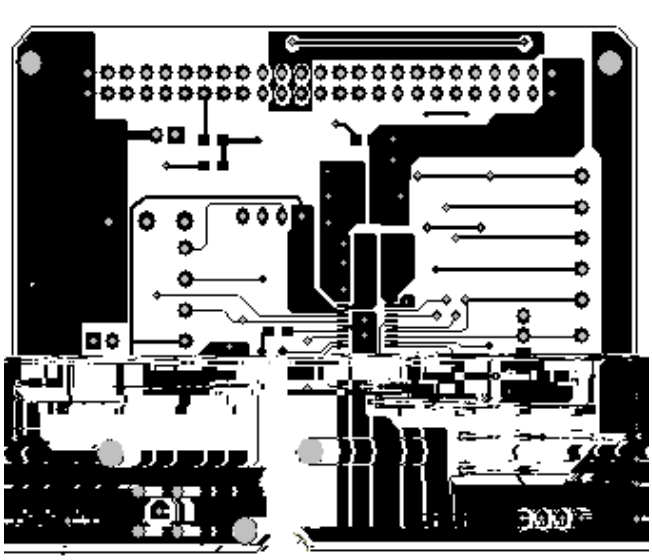
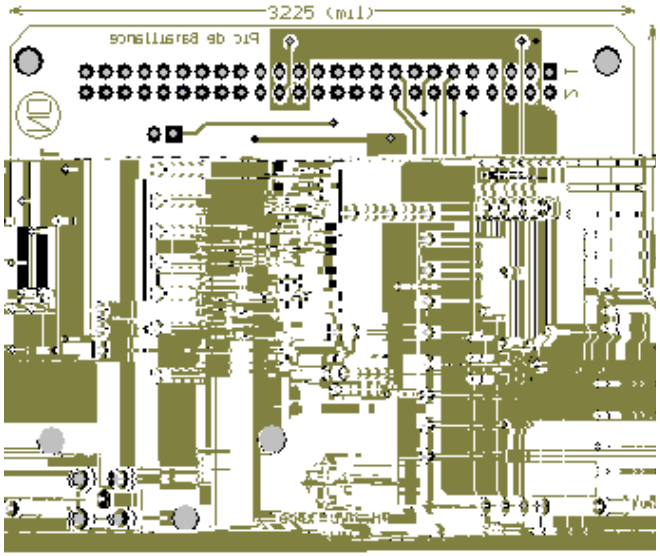


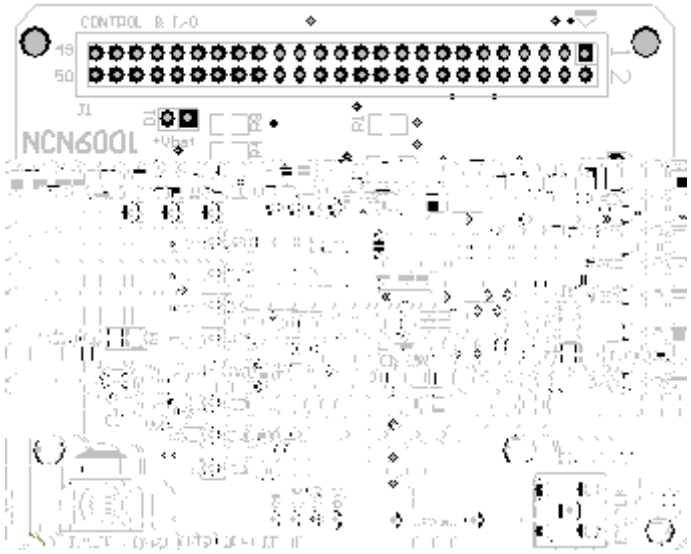
Figure 31. NCN6001 Engineering Test Board Schematic Diagram



Component Side (Top)



Copper Side (Bottom)



Top side

Figure 32. NCN6001 Demo Board Printed Circuit Board Layout

Table 11. DEMO BOARD BILL OF MATERIAL

Desig.	Part Type	Footprint	Description	Supplier	Part Number
C1	10 μF	1206	Capacitor	MURATA	GRM40−X5R−106K6.3
C2	10 μF	1206	Capacitor	MURATA	GRM40−X5R−106K6.3
C3	22 pF	805	Capacitor	MURATA	
C7	4.7 μF	1206	Capacitor	MURATA	GRM40−034X5R−475K6.3
C8	4.7 μF	1206	Capacitor	MURATA	GRM40−034X5R−475K6.3
D1	V				

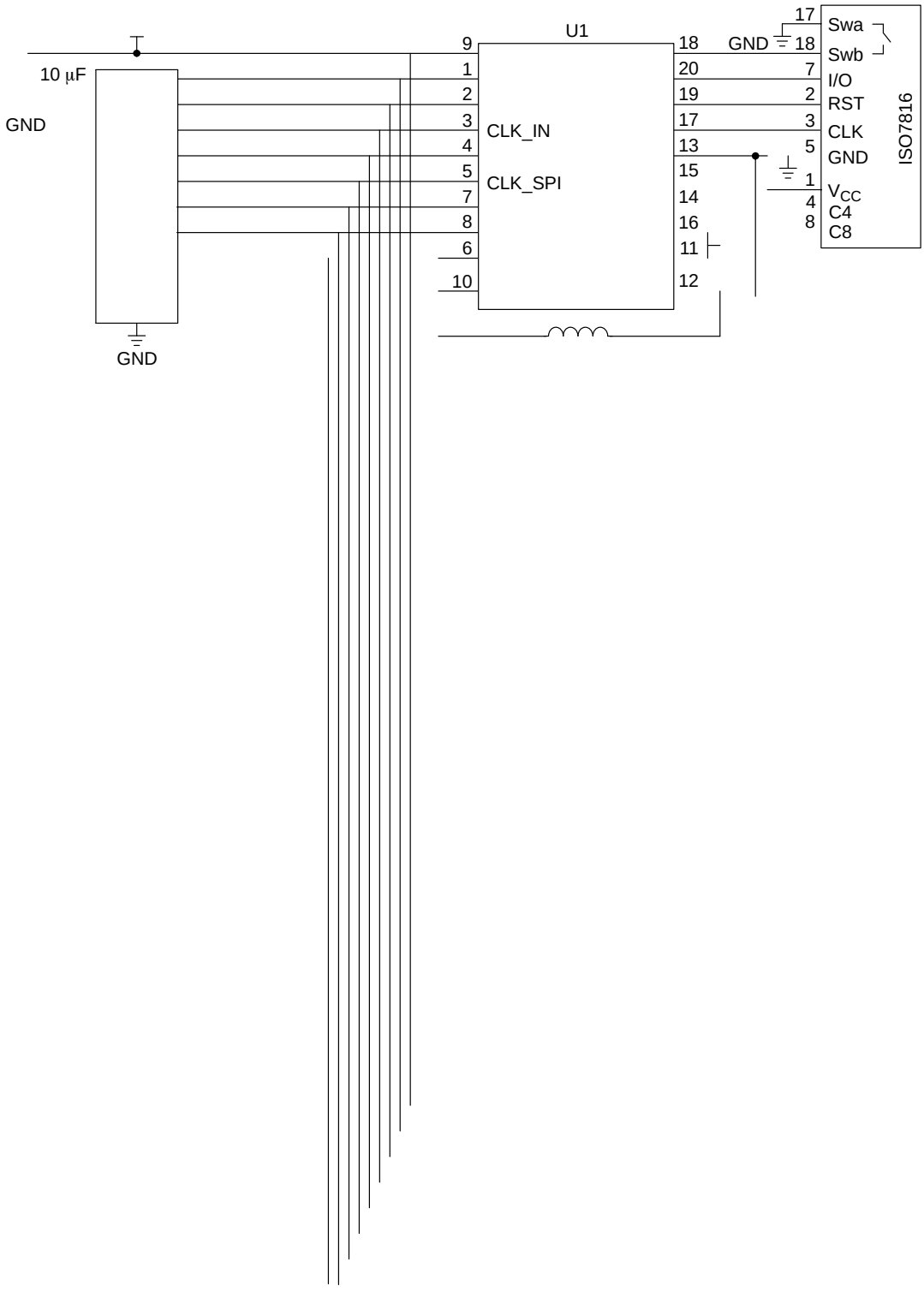
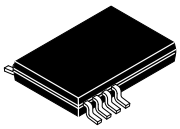


Figure 33. Typical Multiple Parallel Interfaces



SCALE 2:1

TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016