The NCN6010 is a level shifter analog circuit designed to translate the voltages between a SIM Card and an external microcontroller. A built-in DC-DC converter makes the NCN6010 useable to drive any type of SIM card. The device fulfills the GSM 11.11 specification. The external MPU has an access to a dedicated input STOP pin, providing a way to switch off the power applied to the SIM card in case of failure or when the card is removed.

Features

- Supports 3.0 V or 5.0 V Operating SIM Card
- Built-in Pull Up Resistor for I/O Pin in Both Directions
- All Pins are Fully ESD Protected, According to GSM Specification
- Supports 10 MHz Clock
- 6.0 kV ESD Proof on SIM Card Pins
- These are Pb-Free Devices**

Typical Applications

- Cellular Phone SIM Interface
- Identification Module

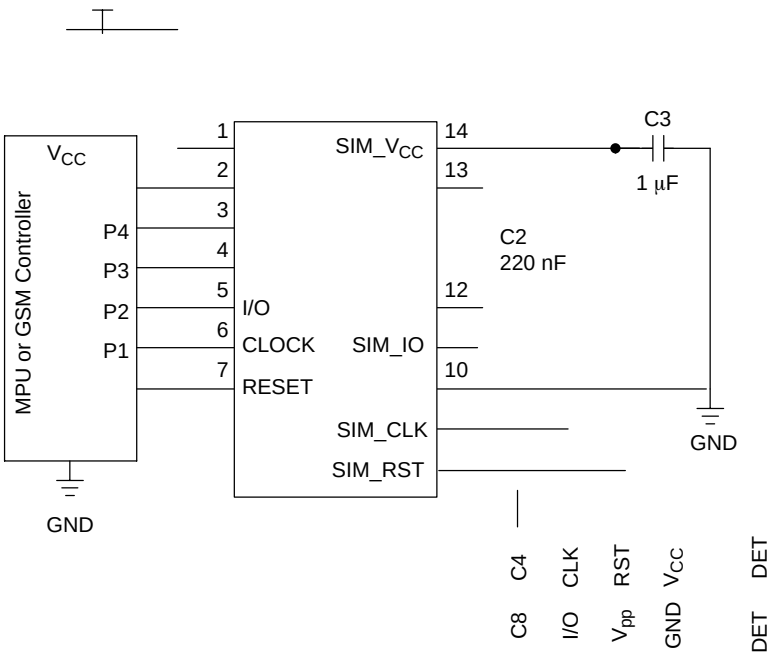
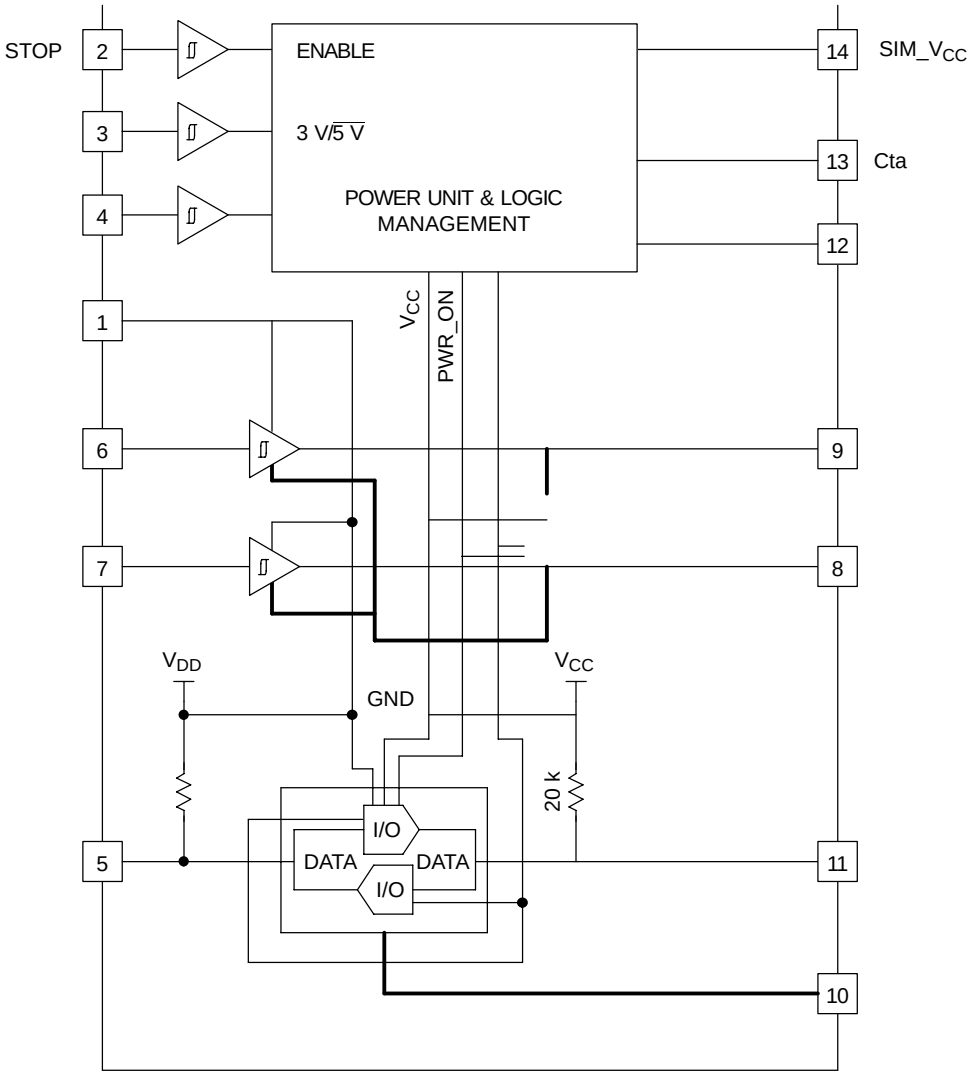


Figure 1. Typical Interface Application


STOP
2
3
4
1
6
7
5
14
13
12
9
8
11
10
ENABLE
3 V/5 V
POWER UNIT & LOGIC
MANAGEMENT
SIM_VCC
Cta
VCC
PWR_ON
VDD
GND
VCC
20 k
I/O
DATA
DATA
I/O

PIN DESCRIPTIONS

Pin	Name	Type	Description
1	V_{DD}	POWER	This pin is connected to the system controller power supply suitable to operate from a

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply	V_{DD}	7.0	V
External Card Power Supply and Level Shifter	SIM_VCC	7.0	V
Digital Input Voltage Digital Input Current	STOP	$-0.3 \leq V \leq V_{DD}$ 1.0	V mA
Digital Input Voltage Digital Input Current	RESET	$-0.3 \leq V \leq V_{DD}$ 1.0	V mA
Digital Input Voltage Digital Input Current	CLOCK	$-0.3 \leq V \leq V_{DD}$ 1.0	V mA
Digital Input Voltage Digital Input Current	I/O	$-0.3 \leq V \leq V_{DD}$ 1.0	V mA
Digital Output Voltage Digital Output Current	SIM_RST	$-0.3 \leq V \leq$ SIM_VCC 25	V mA

POWER SUPPLY SECTION (-25 °C to +85°C)

Rating	Symbol	Pin	Min	Typ	Max	Unit
Power Supply	V_{DD}	1	2.7	-	3.6	V
Standby Supply Current @ No Input Clock, All Input Logic to H, No Load Connected to the SIM Interface.	I V_{DD}	1	-	500	-	nA
Ground Current, @ V						

SIM INTERFACE SECTION (Note 7)

Rating	Symbol	Pin	Min	Typ	Max	Unit
SIM_VCC = +5.0 V Output RESET V_{OH} @ Isim_rst = +200 μA Output RESET V_{OL} @ Isim_rst = -200 μA Output RESET Rise Time @ Cout = 50 pF Output RESET Fall Time @ Cout = 50 pF SIM_VCC = +3.0 V Output RESET V_{OH} @ Isim_rst = +200 μA Output RESET V_{OL} @ Isim_rst = -200 μA Output RESET Rise Time @ Cout = 50 pF Output RESET Fall Time @ Cout = 50 pF	SIM_RST Note 5	8	SIM_VCC - 0.7 0SI92.8o 332.64 690.36()TjET239.04 594.96 0.60001 115.2 2j1.3292yir			

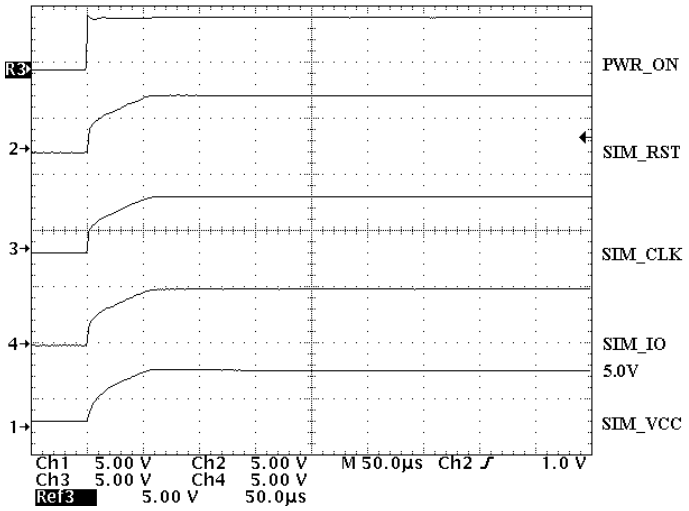


Figure 3. Power On Sequence

Power Down Operation

The power down mode can be initiated by either the PWR_ON or by the STOP pin condition. In both cases, the communication I/O session is terminated immediately, according to the ISO7816-3 sequence as depicted in Figure 4. When the PWR_ON signal is set Low, the NCN6010 goes to the power down mode. According to the ISO7816-3 procedure defined to deactivate the SIM contacts, the input pins I/O, CLOCK and RESET must be Low before the PWR_ON is taken Low. When the PWR_ON is Low, the SIM_IO, SIM_CLK and SIM_RST pins are forced to Low and the SIM_VCC pin is left floating.

When the STOP signal is Low, the SIM_IO, SIM_CLK and SIM_RST are forced Low, the SIM_VCC being left floating, until the STOP pin is taken High again.

When the card is extracted, the external MPU shall detect the operation and run the Power Down of the card by forcing PWR_ON input to Low. The NCN6010 fulfills the power sequence as defined by the ISO/CEI 7816-3 norm (see oscillogram given in Figure 5).

Force SIM_RST to Low
Force SIM_CLK to Low, unless it is already in this state
Force SIM_IO to Low
Shut Off the SIM_V_{CC} supply

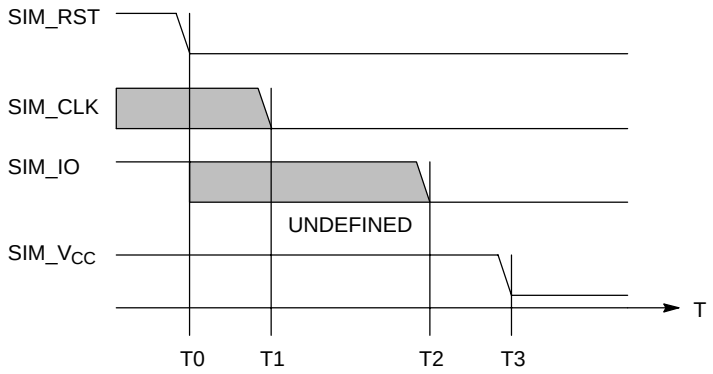


Figure 4. ISO7816-3 Power Down Sequence

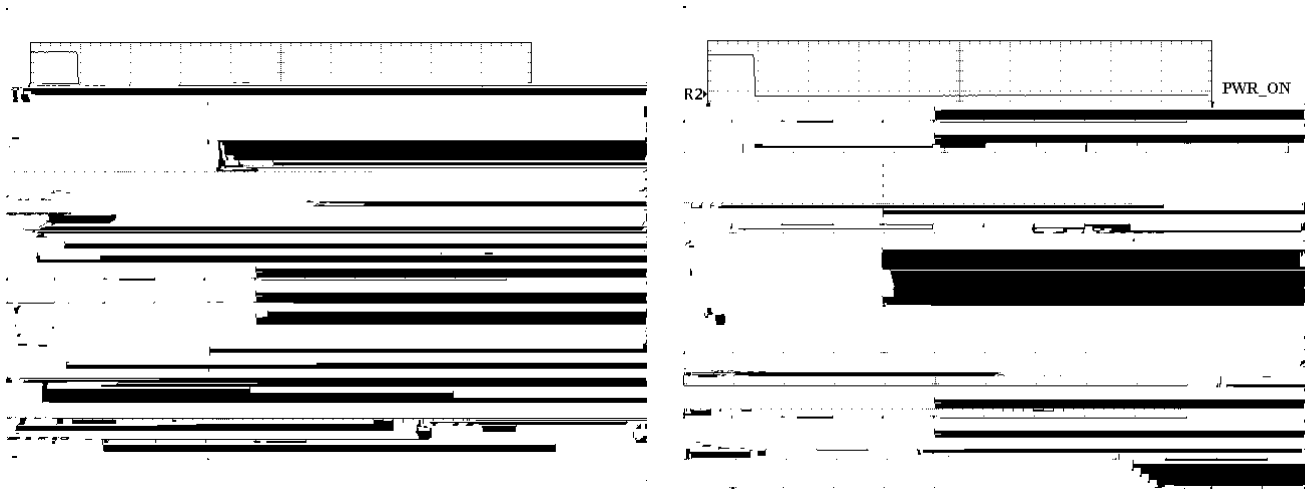


Figure 5. Power Down Sequence Oscillogram

Level Shifters

When the SIM card voltage is either higher or lower than the MPU V_{DD} supply, the level shifters can be

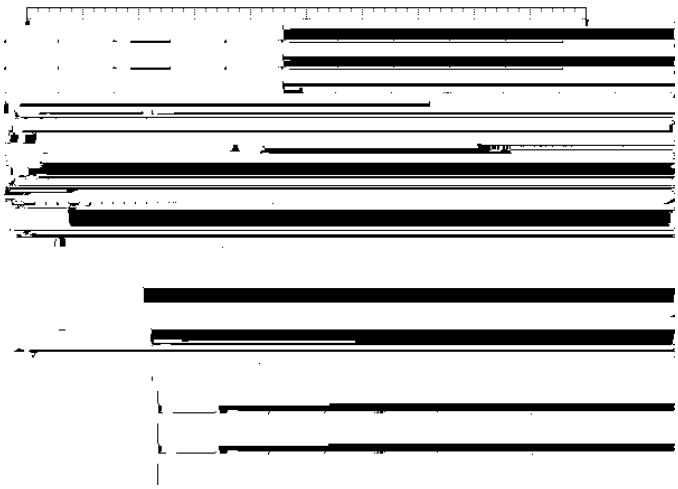


Figure 7. SIM_IO Rise and Fall Time Oscillogram

Input Schmitt Triggers

All the Logic Input pins have built-in Schmitt trigger circuits to prevent the NCN6010 against uncontrolled operation. The typical dynamic characteristics of the related pins are depicted in Figure 8.

The output signal is guaranteed to go High when the input voltage is above 0.70*Vbat, and will go Low when the input voltage is below 0.30 * Vbat.

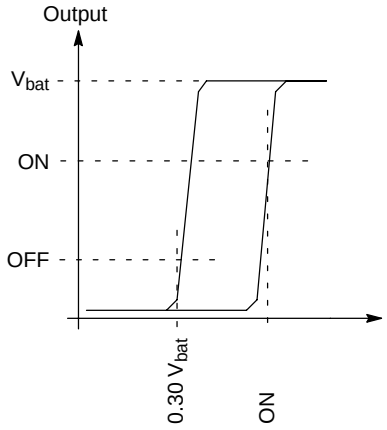


Figure 8. Typical Schmitt Trigger Characteristic

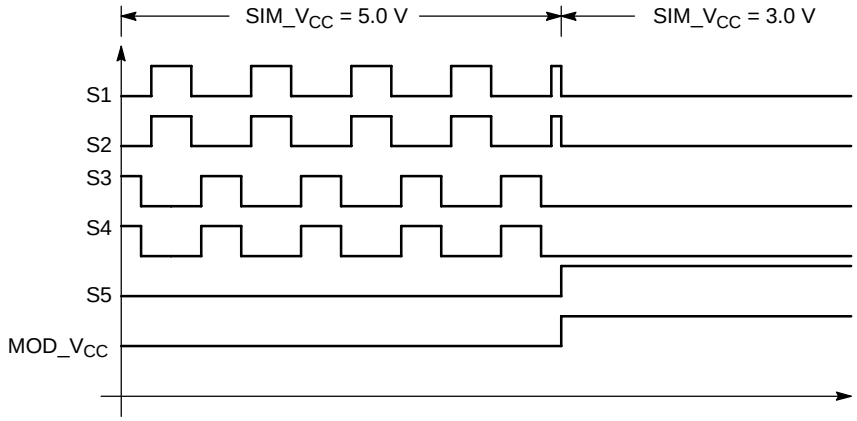


Figure 10. Basic Charge Pump Operating Timings

When the NCN6010 is programmed in the 5.0 V output voltage, the clocks are activated, switch S5 is disconnected and the output voltage is the result of the C1 charge transfer into the output load. The current is limited by three mains parameters:

- the Ron of the switching MOS (S1 through S4)
- the operating frequency
- the C1/C2 ratio and their ESR

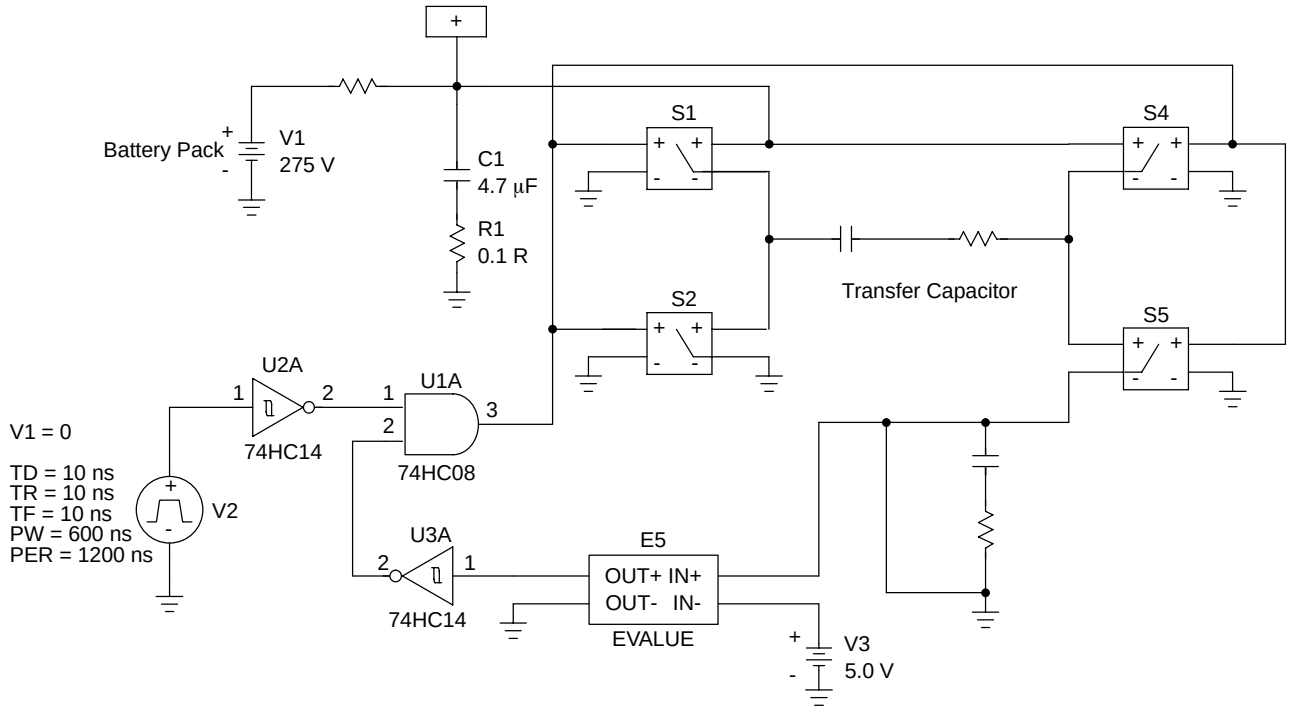
The first parameters are depending upon the internal structure and size of the NMOS/PMOS devices used to design the chip. The third parameter is adjustable by the user and, beside the micro farad values, the type of capacitors plays a significant role. As a matter of fact, using a low cost electrolytic model will ruin the efficiency due to the high ESR of such a capacitor. It is highly recommended to use ceramic types, preferably from the X5R or X7R series, to achieve the efficiency and the SIM_VCC output voltage ripple. Table 2 summarizes the characteristics of the most common type of capacitors.

Table 2. Comparison of Capacitor Types

Manufacturers	Type/Serie	Format	Max Value	Tolerance	Typ. Z @ 500 kHz

It is clear that, with nearly half an ohm of resistance is series with the pure capacitor, the tantalum or the electrolytic type will generate high voltage spikes and poor regulation in the high frequency operating charge pump built into the NCN6010. Moreover, with ESR in the 3.0 Ohm range, low cost capacitors are not suitable for this application.

Figure 11 provides the schematic diagram of the simulated charge pump circuit. Although this schematic does not represent the accurate internal structure of the NCN6010, it can be used for engineering purpose. The ABM devices S1, S2, S4 and S5 have been defined in the PSPICE model to represent the NMOS and PMOS used in the silicon. The ESR value of C2 and C3 can be adjusted, at PSPICE level, to cope with any type of external capacitors and are useful to double check the behavior of the system as a function of the external passives components.



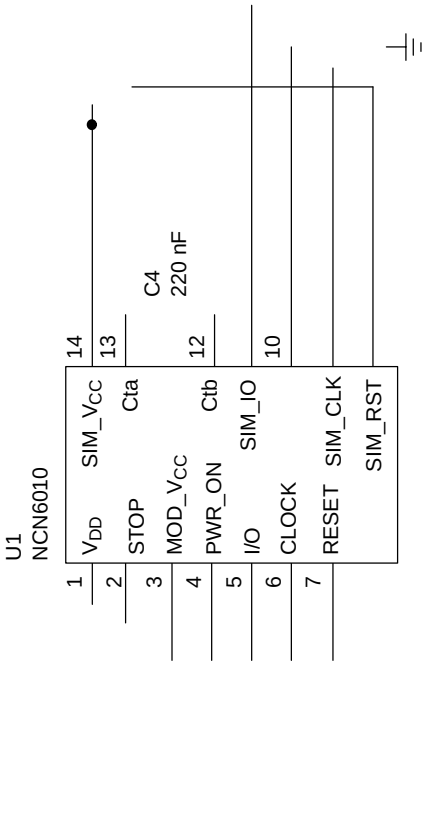


Figure 14. Engineering Test Board

The layout of the PCB is a key parameter to avoid the voltage spikes that could pollute the rest of the system. Figure 16 represents a typical printed circuit lay out, based on the schematic diagram given in Figure 14, highlighting the large ground plane used in this engineering tool. Obviously, a GSM application will use much less area, but cares must be observed to locate the capacitors as close as possible to the integrated circuit associated pins.

Capacitors C1, C2, C3, C4 and C5 are ceramic, X7R, 10 V, surface mount.