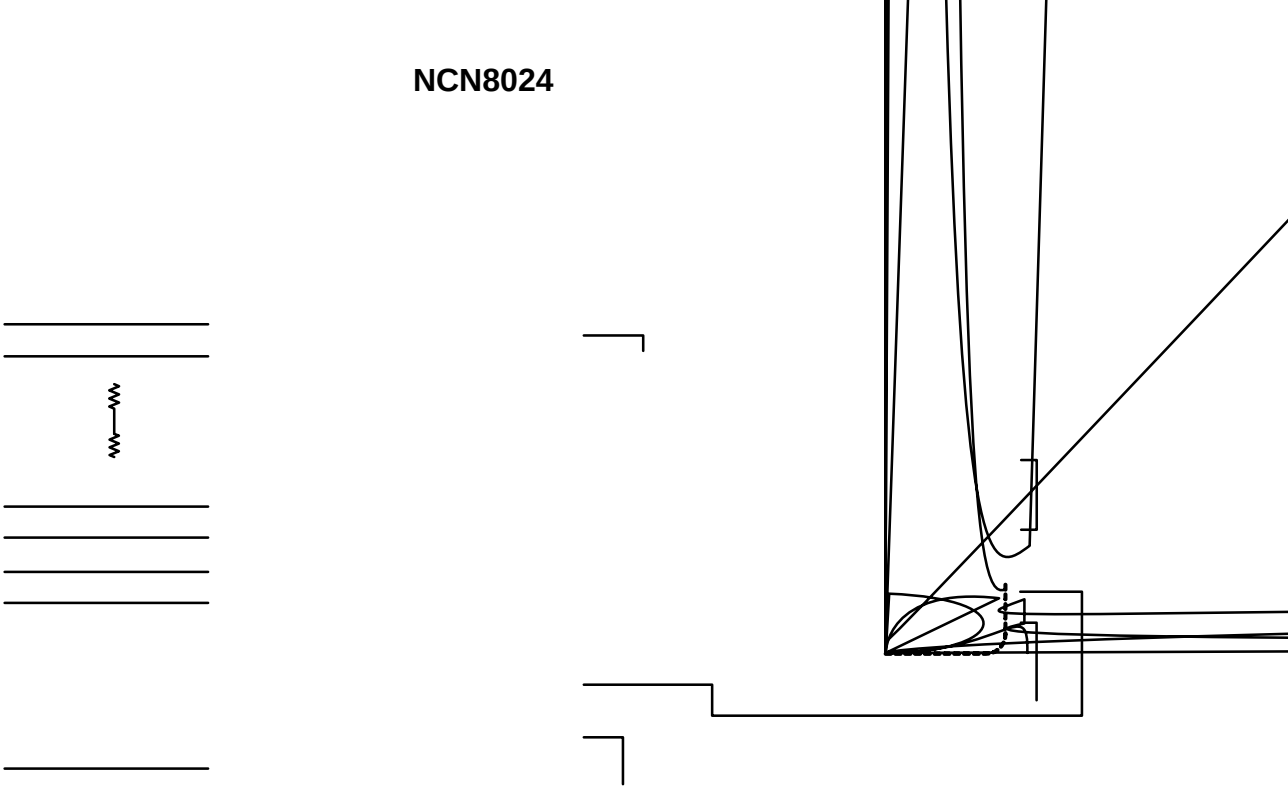


Figure 1. Typical Smart Card Interface Application

PIN FUNCTION AND DESCRIPTION

Pin #	Name	Type	Description
11	CRD_I/O	Input/ Output	This pin handles the connection to the serial I/O (C7) of the card connector. A bi directional level translator adapts the serial I/O signal between the card and the micro controller. An 11 kΩ (typical) pullup resistor to CRD_V_{CC} provides a High impedance state for the smart card I/O link.
12	CRD_AUX2	Input/ Output	This pin handles the connection to the chip card's serial auxiliary AUX2 I/O pin (C8). A bi directional level translator adapts the serial I/O signal between the card and the micro controller. An 11 kΩ (typical) pullup resistor to CRD_V_{CC} provides a High impedance state for the smart card C8 pin.
13	CRD_AUX1	Input/ Output	This pin handles the connection to the chip card's serial auxiliary AUX1 I/O pin (C4). A bi directional level translator adapts the serial I/O signal between the card and the micro controller. An 11 kΩ (typical) pullup resistor to CRD_V_{CC} provides a High impedance state for the smart card C4 pin.
14	CRD_GND	GND	Card Ground
15	CRD_CLK	Output	This pin is connected to the CLOCK card connector's pin (Chip card's pin C3). The Clock signal comes from the CLKIN input through clock dividers and level shifter.
16	CRD_RST	Output	This pin is connected to the chip card's RESET pin (C2) through the card connector. A level translator adapts the external Reset (RSTIN) signal to the smart card.
17	CRD_VCC	Power	This pin is connected to the smart card power supply pin. An internal DC/DC converter is programmable using the pin 5V/$\overline{3V}$ to supply either 5 V or 3 V output voltage. An external distributed

ATTRIBUTES

Characteristics	Values
ESD protection Human Body Model (HBM) (Note 1) Card Pins (Card Interface Pins 9 17) All Other Pins Machine Model (MM) Card Pins (Card Interface Pins 9 17) All Other Pins	 8 kV 2 kV 400 V 150 V
Moisture sensitivity (Note 2) SOIC 28 and TSSOP 28	Level 3
Flammability Rating Oxygen Index: 28 to 34	UL 94 V 0 @ 0.125 in
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch up Test	

1. Human Body Model (HBM), R = 1500 Ω, C = 100 pF.
2. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 3)

Rating	Symbol	Value	Unit
DC/DC Converter Power Supply Voltage	V_{DDP}	$0.3 \le V_{DDP} \le 5.5$	V
Power Supply from Microcontroller Side	V_{DD}	$0.3 \le V_{DD} \le 5.5$	V
External Card Power Supply	CRD_V_{CC}	$0.3 \le$ CRD_$V_{CC} \le 5.5$	V
Charge Pump Output	V_{UP}	$0.3 \le V_{UP} \le 5.5$	
Digital Input Pins	V≤		

POWER SUPPLY SECTION (V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25 C; F_{CLKIN} = 10 MHz)

Pin	Symbol	Rating	Min	Typ

POWER SUPPLY SECTION (V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25 C; F_{CLKIN} = 10 MHz)

Pin	Symbol	Rating	Min	Typ	Max	Unit
DC/DC CONVERTER						
17	CRD_V_{CC}	Output Card Supply Voltage @ 3.6 V ≤ V_{DDP} ≤ 5.5 V with $\|I_{CC}\|$ ≤ 65 mA load transient from 100 Hz to 200 MHz (including ripple) (Note 4) CRD_V_{CC} = 3.0 V CRD_V_{CC} = 5.0 V	 2.76 4.65	 3.00 5.00	 3.20 5.25	 V V
17	CRD_V_{CC}	Output Card Supply Voltage @ 4.5 V< V_{DDP} < 5.5 V with Current Load Pulses of 40 nAs/t < 400 ns and $\|I_{CC}\|$ < 200 mA Peak Current (Including Ripple) (Note 4) CRD_V_{CC} = 3.0 V CRD_V_{CC} = 5.0 V	 2.76 4.65	 3.00 5.00	 3.20 5.25	 V V
17	I_{CRD_VCC}	Card Supply Current @ CRD_V_{CC} = 3.0 V @ CRD_V_{CC} = 5.0 V			 75 75	mA
17	$I_{CRD\_VCC\_SC}$	Short Circuit Current CRD_V_{CC} Shorted to Ground		110	150	mA
17	ΔV_{CRD_VCC}	Output Card Supply Voltage Ripple Peak to Peak f_{ripple} = 100 Hz to				

DIGITAL INPUT/OUTPUT SECTION CLKIN, RSTIN, I/Ouc, AUX1uc, AUX2uc, CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, 5V/$\overline{\text{3V}}$
(V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25 C; F_{CLKIN} = 10 MHz)

Pin	Symbol	Rating	Min	Typ	Max	Unit
26, 27, 28	V_{OH}	I/Ouc, AUX1uc, AUX2uc data channels, @ Cs ≤ 30 pF High Level Output Voltage (CRD_I/O = CRD_AUX1 = CRD_AUX2 = CRD_V_{CC}) I_{OH} = 0 I_{OH} = 40 μA	0.9 x V_{DD} 0.75 x V_{DD}		V_{DD} + 0.1 V_{DD} + 0.1	V V
	V_{OL}	Low Level Output Voltage (C_I/O= CRD_AUX1 = CRD_AUX2 = 0 V) I_{OL} = +1 mA	0		0.3	V
	$t_{Ri/Fi}$	Input Rising/Falling Times (Note 6)			1.2	μs
	$t_{Ro/Fo}$	Output Rising/Falling Times (Note 6)			0.1	μs
26, 27, 28	F_{bidi}	Maximum Frequency through Bidirectional I/O, AUX1 and AUX2 Channels (Note 6)			1	MHz
26, 27, 28	R_{pu}	I/0uc, AUX1uc, AUX2uc Pullup Resistor	8.0	11	16	kΩ
23	V_{OH}	Output High Voltage $\overline{\text{INT}}$ @ I_{OH} = 15 μA (Source)	0.75 x V_{DD}			V
23	V_{OL}	Output Low Voltage $\overline{\text{INT}}$ @ I_{OL} = 2 mA (Sink)	0		0.30	V
23	R_{INT}	$\overline{\text{INT}}$ Pullup Resistor	14	20	26	kΩ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Guaranteed by design and characterization

SMART CARD INTERFACE SECTION, CRD_IO, CRD_AUX1, CRD_AUX2, CRD_CLK, CRD_RST, CRD_PRES, $\overline{\text{CRD\_PRES}}$ (V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25 C; F_{CLKIN} = 10 MHz)

Pin	Symbol	Rating	Min	Typ	Max	Unit
9, 10	 $\lvert I_{IH}\rvert$ $\lvert I_{IL}\rvert$	CRD_PRES, $\overline{\text{CRD\_PRES}}$ High level input leakage current, $V_{IH} = V_{DD}$ CRD_PRES $\overline{\text{CRD\_PRES}}$ Low level input leakage current, V_{IL} = 0 V CRD_PRES $\overline{\text{CRD\_PRES}}$		 5 5	 10 1 1 10	μA
9, 10	$T_{debounce}$	Debounce Time CRD_PRES and $\overline{\text{CRD\_PRES}}$ (Note 7)	5	8	11	ms
11, 12, 13, 16	I_{CRD_IO}	CRD_IO, CRD_AUX1, CRD_AUX2 Current Limitation			15	mA
15	I_{CRD_CLK}	CRD_CLK Current Limitation			70	mA
16	I_{CRD_RST}	CRD_RST Current Limitation			20	mA
	t_{act}	Activation Time (Note 7)	30		100	μs
	t_{deact}	Deactivation Time (Note 7)	30		250	μs
	$Temp_{SD}$	Shutdown Temperature		160		C

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Guaranteed by design and characterization

POWER SUPPLY

The NCN8024 smart card interface has two power supplies: V_{DD} and V_{DDP}.

V_{DD} is usually common to the system controller and the interface. The applied V_{DD} ranges from 2.7 V up to 5.5 V. If V_{DD} goes below 2.35 V typical ($UVLO_{VDD}$) a power-down sequence is automatically performed. In that case the interrupt ($\overline{\text{INT}}$) pin is set Low.

A built-in charge-pump-based DC/DC converter followed by a Low Drop-Out (LDO) regulator is used to provide the 3 V or 5 V power supply voltage (CRD_V_{CC}) to the card. V_{DDP} is the converter's input voltage. VUP is the charge-pump converter's output. It is connected to the LDO input. A reservoir capacitor of 100 nF is connected to VUP. CRD_V_{CC} is the LDO output. Even if the converter can operate with a single output reservoir capacitor as low as 100 nF at CRD_V_{CC}, it is recommended to use a capacitor of at least 320 nF in order to satisfy the datasheet specifications. The best recommended combination guaranteeing optimal performances consists in a distributed set of capacitors 220 nF + 330 nF (in particular recommended for optimally satisfying the NDS standard). To minimize dI/dt effects, the fly capacitor (100 nF) and the reservoir capacitors VUP and CRD_V_{CC} have to be connected as close as possible to the corresponding device's pin and feature very low ESR values (lower than 50 mΩ). The fly capacitor is connected between C1 and C2. The decoupling capacitors on V_{DD} and V_{DDP} respectively 100 nF and 10 μF have also to be connected close to the respective IC pins.

The CRD_VCC pin can source up to 75 mA continuously over the V_{DDP} range (from 3.3 V to 5.5 V), the absondr combination1 509S66 35fBT8 09.10c4 0pin and fa10.3(e)verte

PORADJ pin is used to modify the UVLO threshold according to the below relationship considering an external resistor divider R1 / R2 (see block diagram Figure 1):

$$UVLO = \frac{R1 + R2}{R2} V_{POR}$$

If PORADJ is connected to Ground the V_{DD} UVLO threshold (V_{DD} falling) is typically 2.35 V. In some cases it can be interesting to adjust this threshold at a higher value and by the way increase the V_{DD} supply dropout detection level which enables a deactivation sequence if the V_{DD} voltage is too low.

The clock can also be applied to the card using a RSTIN mode allowing controlling the clock starting by setting RSTIN Low (Figure 4). Before running the activation sequence, that is before setting Low $\overline{\text{CMDVCC}}$ RSTIN is set High. In these initial conditions CRD_CLK starts when RSTIN is pulled Low. This allows a precise count of clock pulses before toggling CRD_RST High for ATR (Answer To Reset) request.

The internal activation sequence activates the different channels according to a specific hardware built−in sequencing internally defined but at the end the actual activation sequencing is the responsibility of the application software and can be redefined by the micro−controller to comply with the different standards and the different ways the standards manage this activation (for example light differences exist between the EMV and the ISO7816 standards).

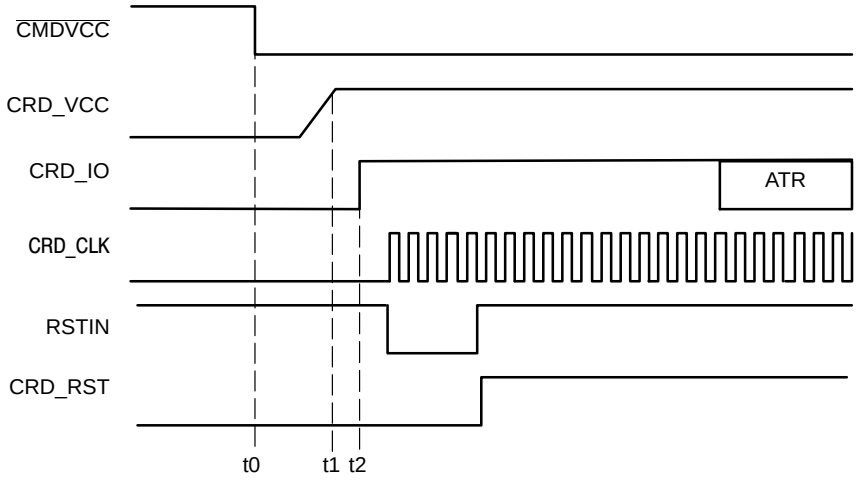


Figure 4. Activation Sequence − RSTIN mode (RSTIN Starting High)

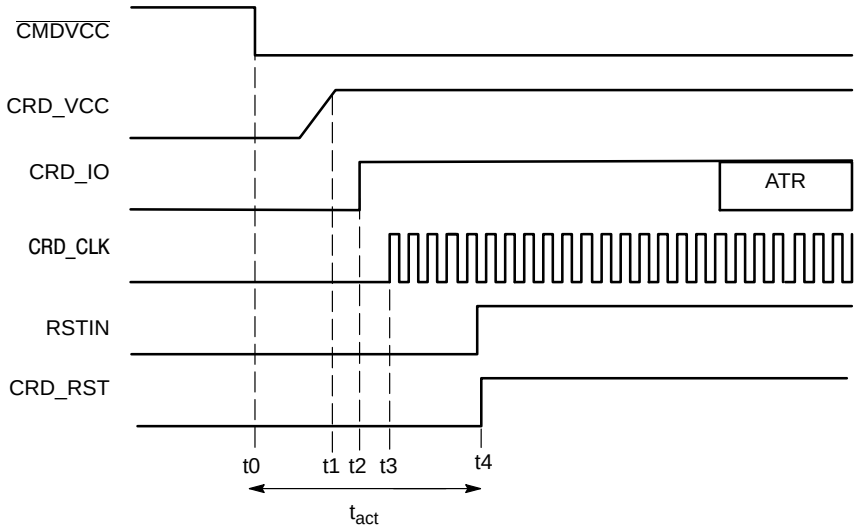


Figure 5. Activation Sequence − Normal Mode

POWER−DOWN

When the communication session is completed the NCN8024 runs a deactivation sequence by setting High $\overline{\text{CMDVCC}}$. The below power down sequence is executed:

CRD_RST is forced to Low

CRD_CLK is set Low 12 μs after CRD_RST.

CRD_IO, CRD_AUX1 and CRD_AUX2 are pulled Low

Finally CRD_V_{CC} supply can be shut ĭ off.

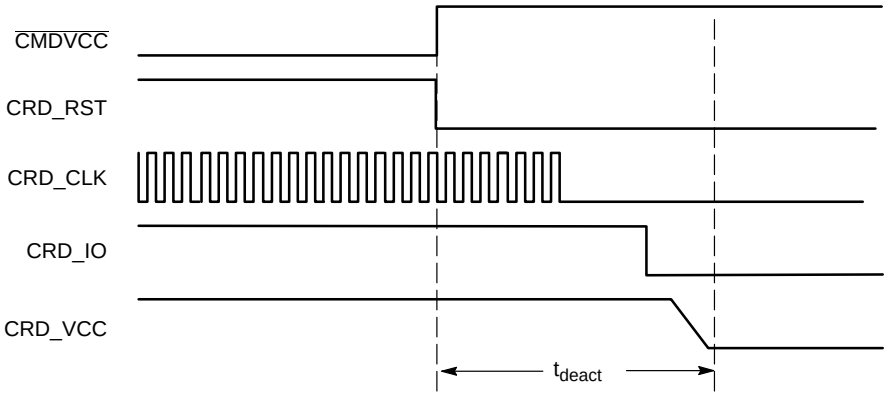


Figure 6. Deactivation Sequence

FAULT DETECTION

In order to protect both the interface and the external smart card, the NCN8024 provides security features to prevent failures or damages as depicted here after.

Card extraction detection

V_{DD} under voltage detection

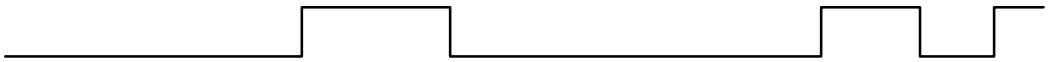
Short ĭ circuit or overload on CRD_V_{CC}

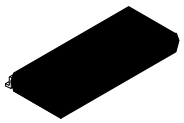
Card pin current limitation: in the case of a short circuit to ground. No feedback is provided to the external MPU.

DC/DC operation: the internal circuit continuously senses the CRD_V_{CC} voltage (in the case of either over or under voltage situation).

DC/DC operation: under ĭ voltage detection on V_{DDP} or overload on VUP

Overheating





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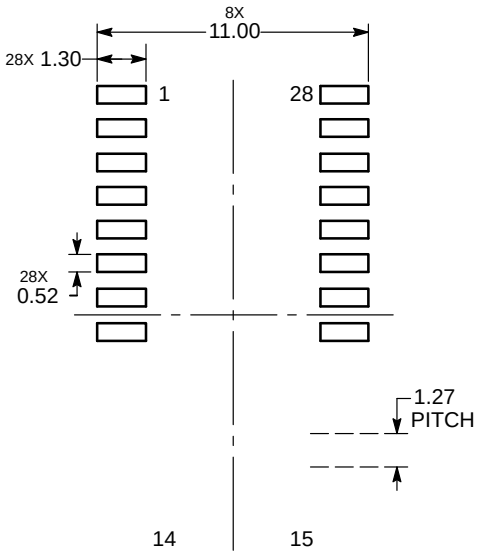

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