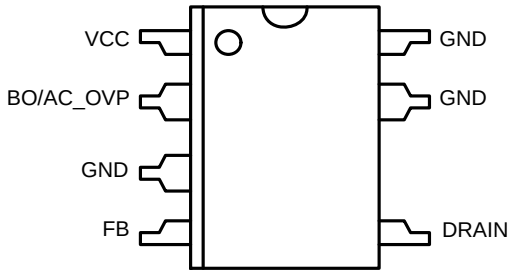
Enhanced Off-line Switcher for Robust and Highly Efficient Power Supplies

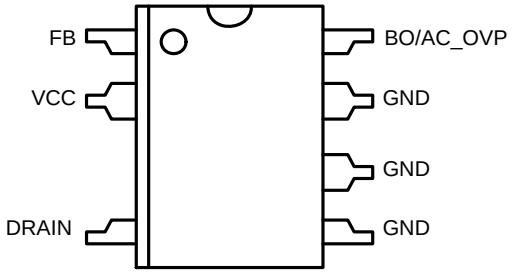
NCP1075A/B, NCP1076A/B, NCP1077A/B, NCP1079A/B

The NCP107xuz products integrate a fixed frequency current mode controller with a 700 V MOSFET. Available in a two different pinǐout of the very common PDIPǐ

PIN CONNECTIONS



(Top View)
PDIP−7
NCP107xA



(Top View)
PDIP−7
NCP107xB

PIN FUNCTION DESCRIPTION

Pin No		Pin Name	Function	Pin Description
PDIP 7 A	PDIP 7 B			
1	2	VCC	IC supply pin	This pin is connected to an external capacitor. The V_{CC} management includes an auto−recovery over−voltage protection.
2	8	BO/AC_OVP	Brown−out / Ac Line Over−voltage protection	Detects both input voltage conditions (Brown−out) and too high an input voltage (Ac line OVP). Do not leave this pin floating – if this pin is not used it should be directly connected do GND.
3	5	GND	The IC Ground	
4	1	FB	Feedback signal input	By connecting an opto−coupler to this pin, the peak current set−point is adjusted accordingly to the output power demand.
5	4	DRAIN	Drain connection	The internal drain MOSFET connection
6	3	NC		This un−connected pin ensures adequate creepage distance
7	6	GND	The IC Ground	
8	7	GND	The IC Ground	

PRODUCTS INFOS & INDICATIVE MAXIMUM OUTPUT POWER

Product	$R_{DS(ON)}$	I_{PK}	230 Vrms ±15%		85−265 Vrms	
			Adapter	Open Frame	Adapter	Open Frame
NCP1075uz	13.5 Ω	400 mA	8.5 W	14 W	6 W	10 W
NCP1076uz / NCP1077uz	4.8 Ω	800 mA	19 W	31 W	14 W	23 W
NCP1079uz	2.9 Ω	1050 mA	25 W	41 W	18 W	30 W

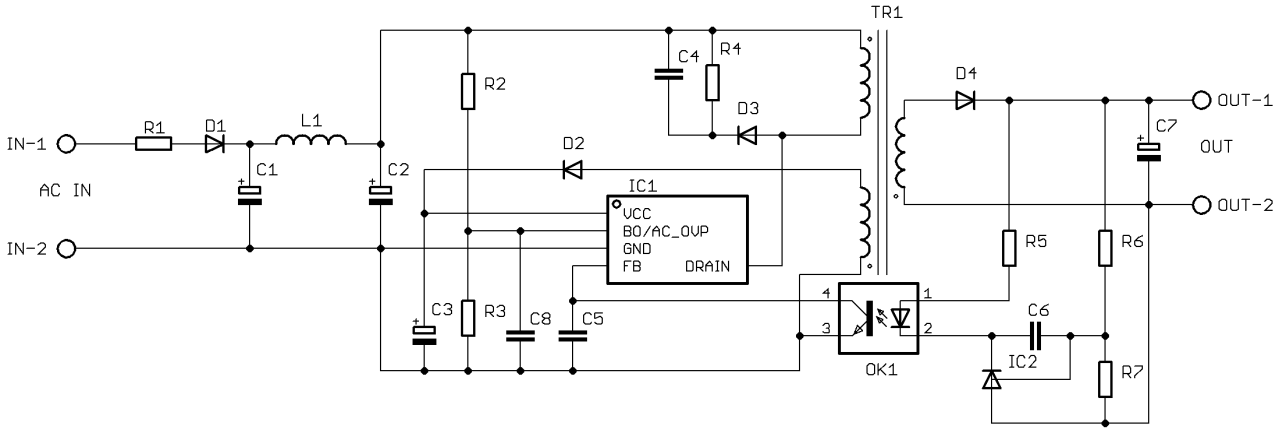


Figure 1. Typical Isolated Application (Flyback Converter), Enable Brown−out, Ac Line OVP and OPP Functions

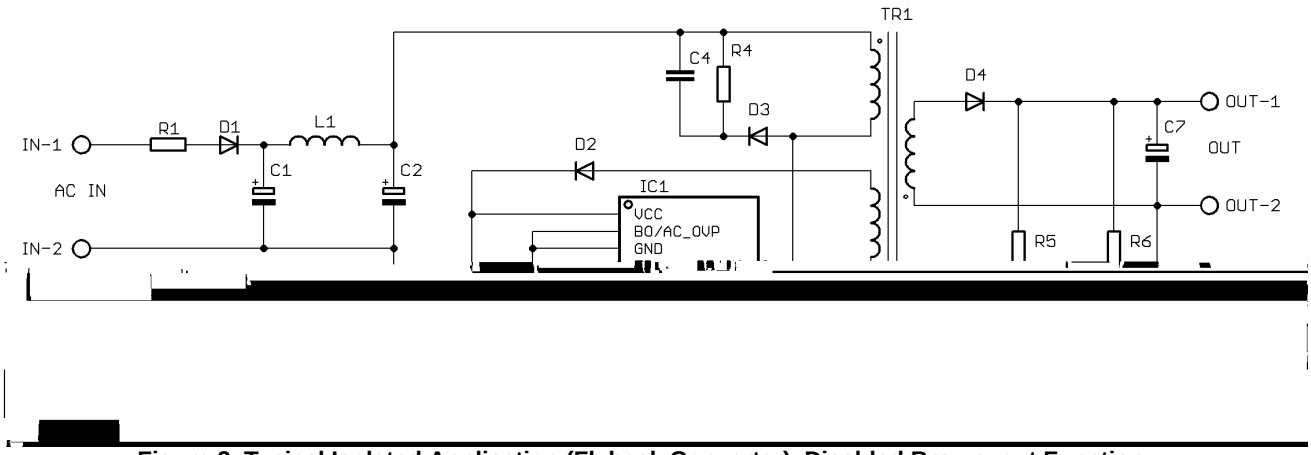


Figure 2. Typical Isolated Application (Flyback Converter), Disabled Brown−out Function – Against Line Detection

MAXIMUM RATINGS TABLE (All voltages related to GND terminal)

Rating		Symbol	Value	Unit
Power supply voltage, VCC pin, continuous voltage		V_{CC}	−0.3 to 20	V
Voltage on all pins, except DRAIN and VCC pin		Vinmax	−0.3 to 10	V
DRAIN voltage		BV_{DSS}	−0.3 to 700	V
Maximum Current into VCC pin		I_{CC}	15	mA
Drain Current Peak during Transformer Saturation (T_J = 150∀C): NCP1075uz NCP1076uz/77uz NCP1079uz Drain Current Peak during Transformer Saturation (T_J = 25∀C): NCP1075uz NCP1076uz/77uz NCP1079uz		$I_{DS(PK)}$	 0.9 2.2 3.6 1.5 3.9 6.4	A
Thermal Resistance Junction−to−Air – PDIP7	0.36 Sq. Inch	$R_{\chi J-A}$	77	∀C/W
	1.0 Sq. Inch		68	
Maximum Junction Temperature		T_{JMAX}	150	∀C
Storage Temperature Range			−60 to +150	∀C
Human Body Model ESD Capability (All pins except HV pin) per JEDEC JESD22−A114F		HBM	2	kV
Human Body Model ESD Capability (Drain pin) per JEDEC JESD22−A114F		HBM	1	kV
Charged−Device Model ESD Capability per JEDEC JESD22−C101E		CDM	1	kV
Machine Model ESD Capability per JEDEC JESD22−A115−A		MM	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.
2. Maximum drain current $I_{DS(PK)}$ is obtained when the transformer saturates. It should not be mixed with short pulses that can be seen at turn on. Figure 4 below provides spike limits the device can tolerate.

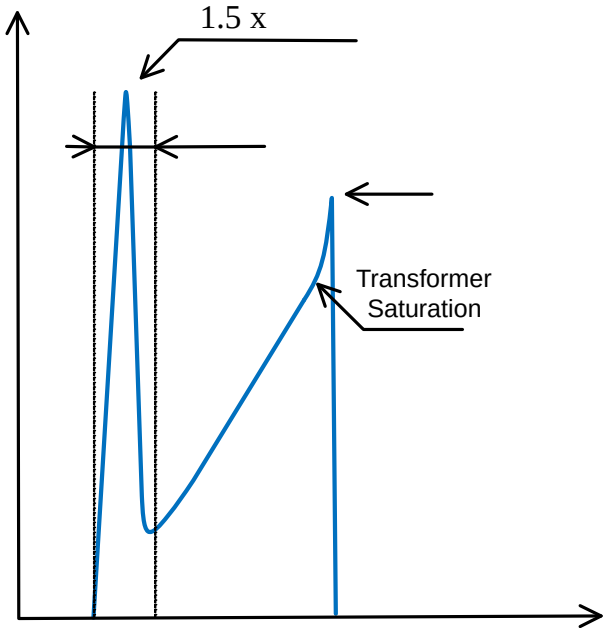


Figure 4. Spike Limits

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
CURRENT COMPARATOR						
$I_{PKSW(65)}$	Final switch current with a primary slope of 200 mA/μs, f_{SW} = 65 kHz (Note 3)					mA
	NCP1075uz	−	−	450	−	
	NCP1076uz	−	−	710	−	
	NCP1077uz	−	−	860	−	
	NCP1079uz	−	−	1100	−	
$I_{PKSW(100)}$	Final switch current with a primary slope of 200 mA/μs, f_{SW} =100 kHz (Note 3)					mA
	NCP1075uz	−	−	440	−	
	NCP1076uz	−	−	685	−	
	NCP1077uz	−	−	825	−	
	NCP1079uz	−	−	1040	−	
$I_{PKSW(130)}$	Final switch current with a primary slope of 200 mA/μs, f_{SW} =130 kHz (Note 3)					
	NCP1075uz					
	NCP1076uz					
	NCP1077uz					
	NCP1079uz					

ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
FREQUENCY FOLDBACK & SKIP						
I_{FBfold}	Start of frequency foldback FB pin current level	4 (1)	−	−68	−	μA
$I_{FBfold(END)}$	End of frequency foldback FB pin current level, $f_{SW} = f_{MIN}$	4 (1)	−	−100	−	μA
f_{MIN}	The frequency below which skip−cycle occurs, T_J = 25°C (Note 4)	−	23	27	31	kHz
$I_{FB(skip)}$	The FB pin current level to enter skip mode	4 (1)	−	−120	−	μA
I_{freeze}	Internal minimum current set−point ($I_{FB} = I_{FB(freeze)}$)					mA
	NCP1075uz	−	−	165	−	
	NCP1076uz	−	−	270	−	
	NCP1077uz	−	−	330	−	
	NCP1079uz	−	−	430	−	

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25∀C, for min/max values T_J = −40∀C to +125∀C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
TEMPERATURE MANAGEMENT						
TSD	Temperature shutdown (Guaranteed by design)	−	150	−	−	∀C
TSD_{HYST}	Hysteresis in shutdown (Guaranteed by design)	−	−	20	−	∀C

3. The final switch current is: $I_{PK(0)}$ / ($V_{in}/L_P + S_a$) x V_{in}/L_P + V_{in}/L_P x t_{prop}, with S_a the built−in slope compensation, V_{in} the input voltage, L_P the primary inductor in a flyback, and t_{prop} the propagation delay.
4. Oscillator frequency is measured with disabled jittering.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

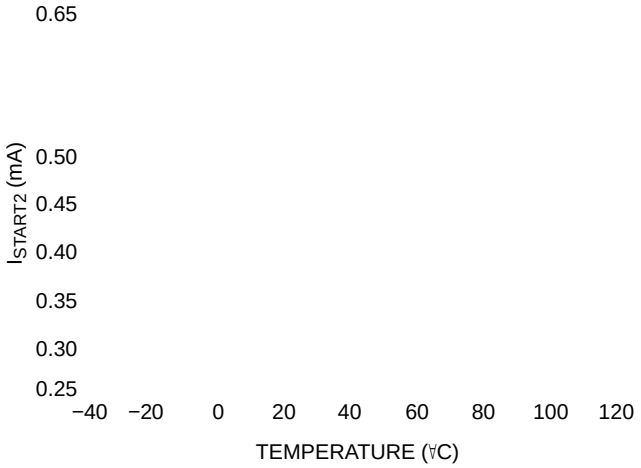


Figure 17. I_{START2} vs. Temperature

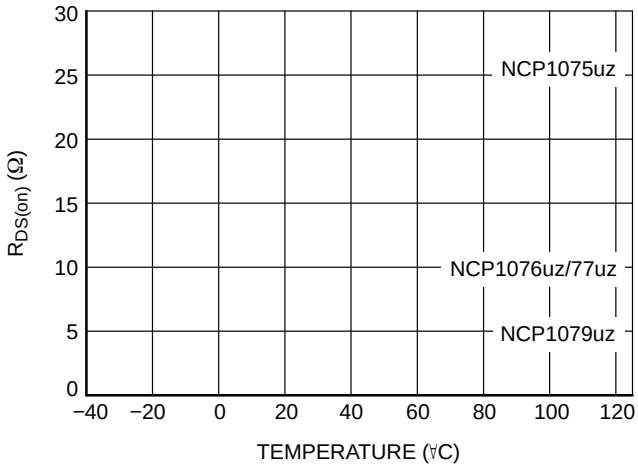


Figure 18. $R_{DS(on)}$ vs. Temperature

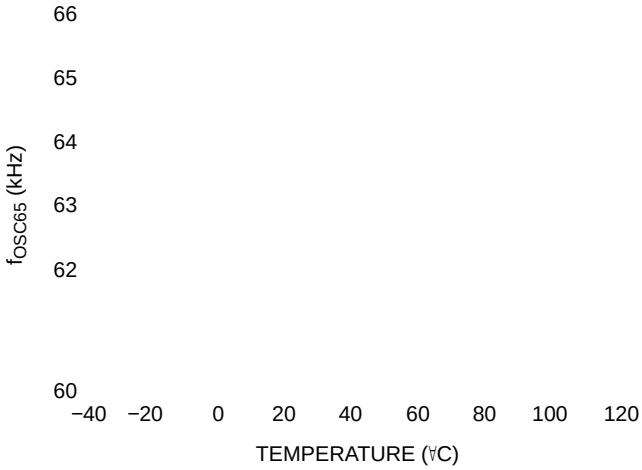


Figure 19. f_{OSC65} vs. Temperature

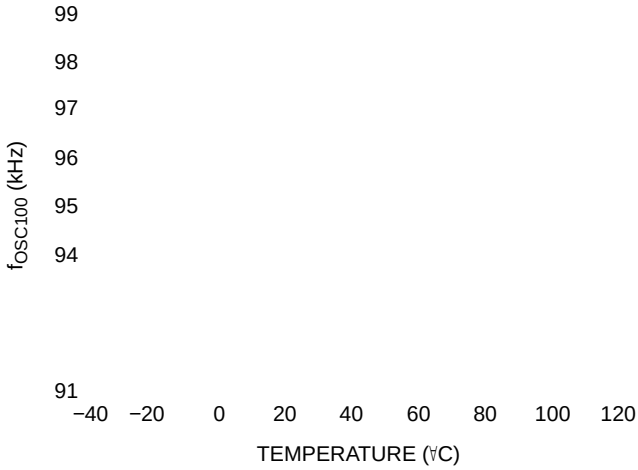


Figure 20. f_{OSC100} vs. Temperature

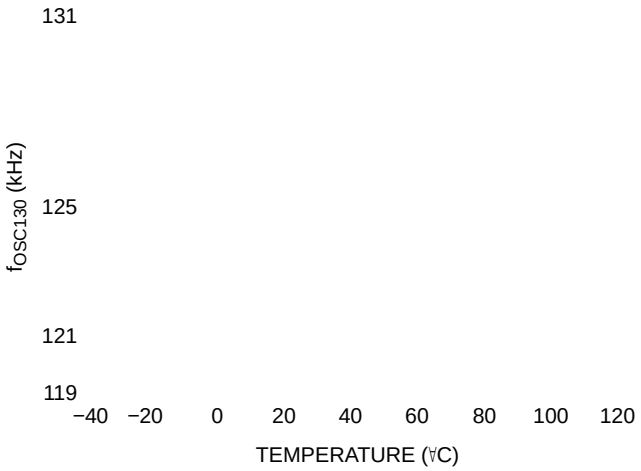


Figure 21. f_{OSC130} vs. Temperature

TYPICAL CHARACTERISTICS

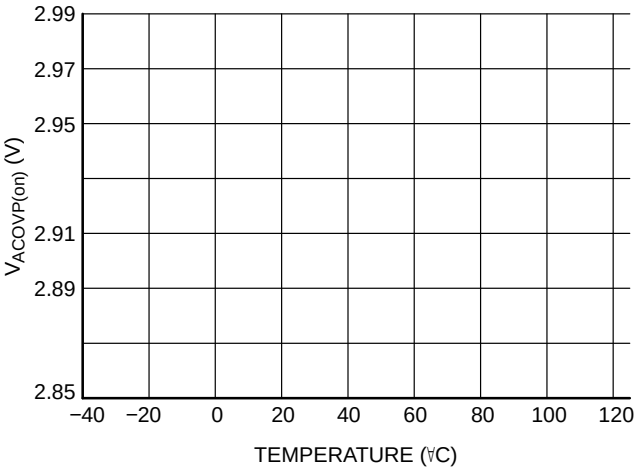


Figure 29. $V_{ACOVP(on)}$ vs. Temperature

As one can see, even if there is auxiliary winding to provide energy for V_{CC}, it happens that the device is still biased by DSS during start−up time or some fault mode when the voltage on auxiliary winding is not ready yet. The V_{CC} capacitor shall be dimensioned to avoid V_{CC} crosses $V_{CC(OFF)}$ level, which stops operation. The ΔV between $V_{CC(MIN)}$ and $V_{CC(OFF)}$ is 0.5 V. There is no current source to charge V_{CC} capacitor when driver is on, i.e. drain voltage is close to zero. Hence the V_{CC}

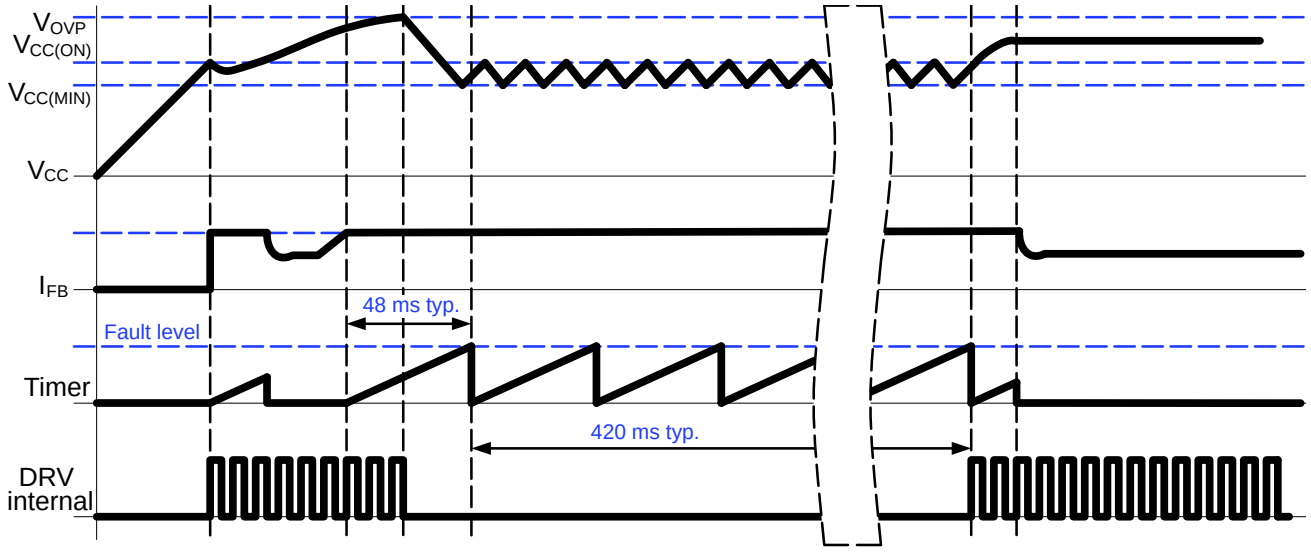


Figure 38. Describes the Main Signal Variations When the Part Operates in Auto−recovery OVP

Soft−start

The NCP107xuz features a 10 ms soft−start which reduces the power−on stress but also contributes to lower the output overshoot. Soft−start is running every time when IC starts switching. It means a first start, a new start after OVP, TSD, Brown−out, etc. Figure 39 shows a typical operating waveform. The NCP107xuz features a novel patented structure which offers a better soft−start ramp, almost ignoring the start−up pedestal inherent to traditional current−mode supplies:

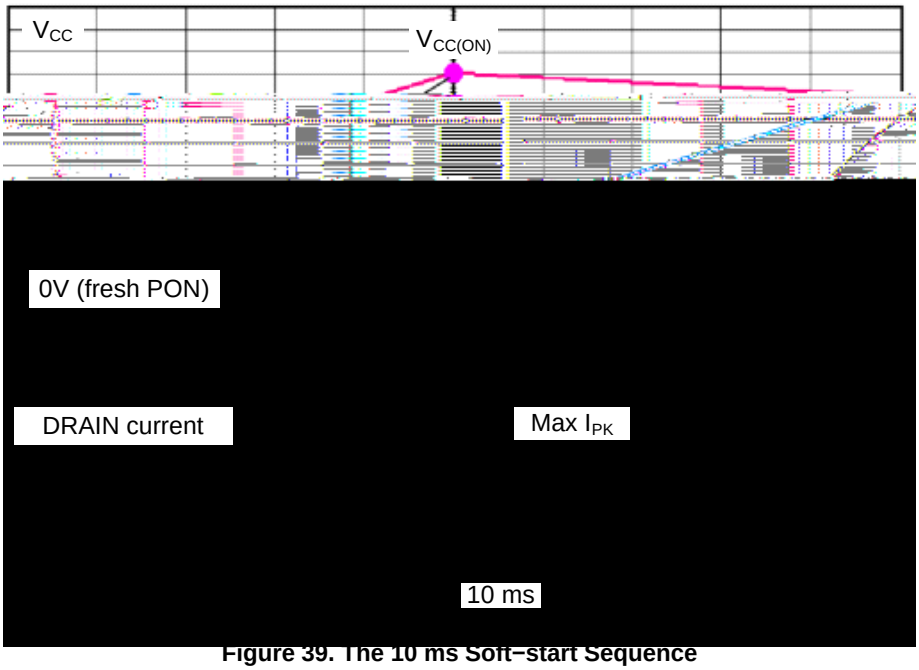
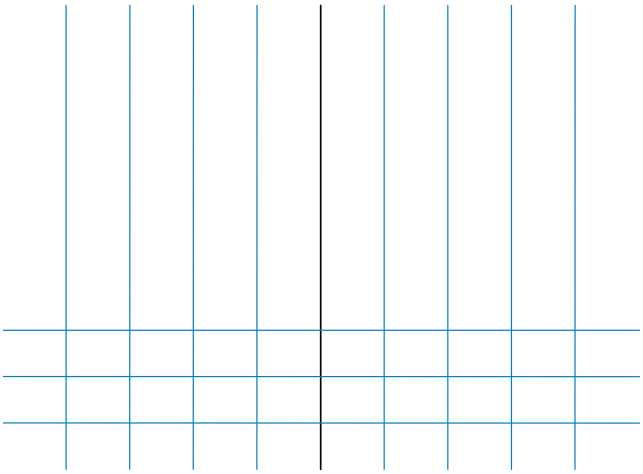


Figure 39. The 10 ms Soft−start Sequence

Jittering

Frequency jittering is a method used to soften the EMI signature by spreading the energy in the vicinity of the main switching component. The NCP107xuz offers a ∂6% deviation of the nominal switching frequency. The sweeping sawtooth is internally generated and modulates the clock up and down with a fixed frequency of 300 Hz. Figure 40 shows the relationship between the jitter ramp and the frequency deviation. It is not possible to externally disable the jitter.



A resistive divider made of R_{UPPER} and $R_{LOWER,}$ brings

The IC also includes overvoltage protection. If the voltage on BO/AC_OVP pin exceed V

Figure 45. By Observing the Current on the FB pin, the Controller Reduces its Switching Frequency for an Improved Performance at Light Load

Figure 47 depicts the skip mode block diagram. When the FB current information reaches $I_{FB(skip)}$, the internal clock to set the flip−flop is blanked and the internal consumption of the controller is decreased. The hysteresis of internal skip comparator is minimized to lower the ripple of the auxiliary voltage for VCC pin and V_{OUT} of power supply during skip mode. It easies the design of V_{CC} overload range.

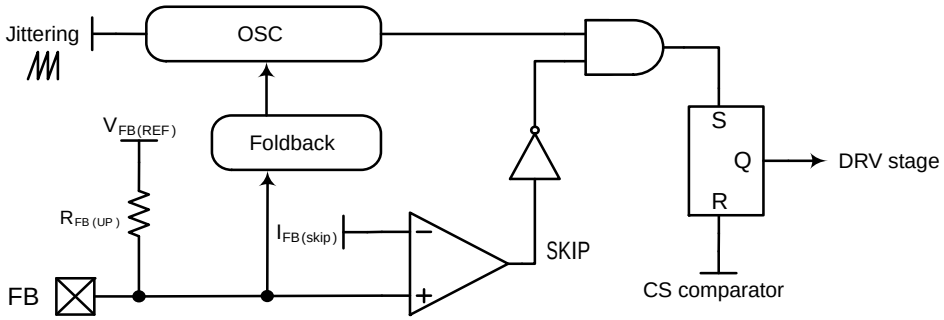
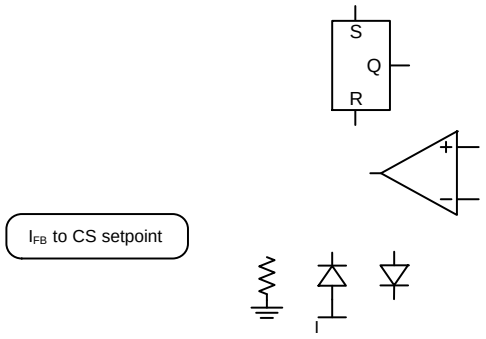


Figure 47. Skip Cycle Schematic

Over−power Protection

This function lets you limit the maximum dc output current regardless of the operating input voltage. For a correct operation, the BO/AC_OVP pin must be connected via a resistive divider to observe the bulk voltage.



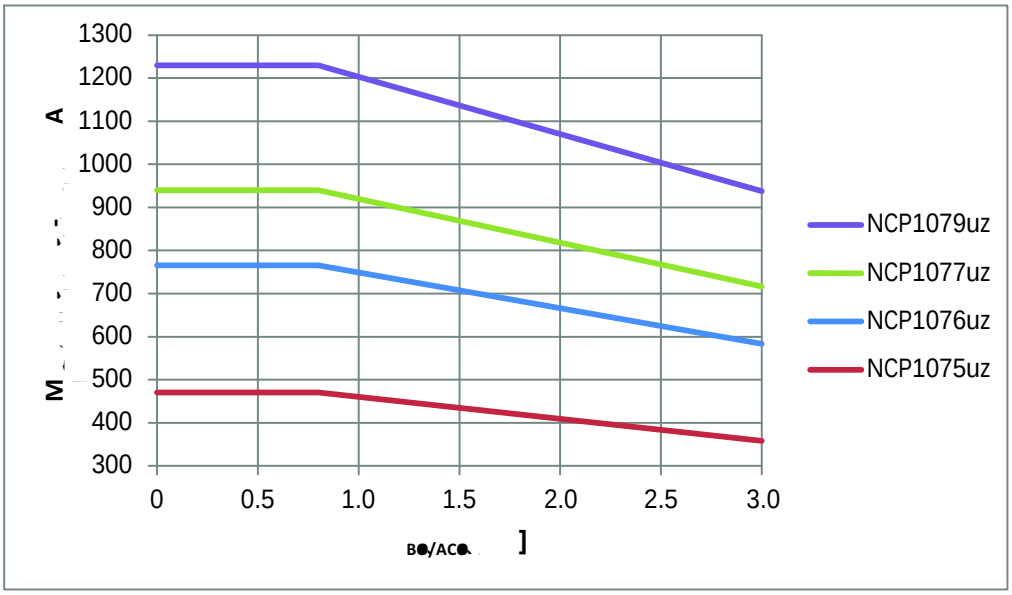


Figure 49. Current Set−point Dependence on BO/AC_OVP Pin Voltage

There are several known ways to implement Over−power Protection (OPP), all suffering from particular problems. These problems range from the added consumption burden on the converter or the skip−cycle disturbance brought by the current−sense offset. In this case is added consumption due to resistive divider (Equation 2).

Maximum peak current is reduced internally according to bulk voltage. When $V_{BO(OPP)}$ is maximum, the peak current set−point is reduced by 10%. Bulk voltage at which will be maximum current peak reduced by 20% (10% in NCP1075uz):

(eq. 5)

$$V_{BULK(OPP)} \cong V_{BO(OPP)} \cdot \frac{V_{BULK(ON)}}{V_{BO(ON)}} \cong V_{BO(OPP)} \cdot \frac{R_{LOWER} + R_{UPPER}}{R_{LOWER}} \cong 2.65 \cdot \frac{100 \cdot 10^3 + 14 \cdot 10^6}{100 \cdot 10^3} \cong 375\ Vdc \cong 265\ Vrms$$

Design Procedure

The design of an SMPS around a monolithic device does not differ from that of a standard circuit using a controller and a MOSFET. However, one needs to be aware of certain characteristics specific of monolithic devices. Let us follow the steps:

$V_{IN,MIN}$ = 90 V rms or 127 V dc once rectified, assuming a low bulk ripple

$V_{IN,MAX}$ = 265 V rms or 375 V dc

V_{OUT} = 12 V

P_{OUT} = 10 W

Operating mode is CCM

ξ = 0.8

1. The lateral MOSFET body ĭ diode shall never be forward biased, either during start ĭ up (because of a large leakage inductance) or in normal operation, depicted by Figure 51. This condition sets the maximum voltage that can be reflected during t_F As a result, the flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you thus must adopt a turn ratio which adheres to the following equation:

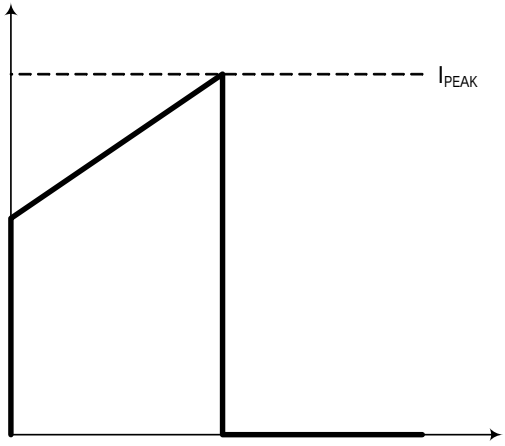
$$N \leq [V_{OUT} + V_F] + V_{IN,MIN} \quad \text{(eq. 6)}$$

2. In our case, since we operate from a 127 V dc rail while delivering 12 V, we can select a reflected voltage of 120 V dc maximum. Therefore, the turn ratio Np:Ns must be smaller than

$$\frac{V_{reflect}}{V_{OUT} + V_F} \leq \frac{120}{12 + 0.5} \leq 9.6 \text{ or } Np : Ns \leq 9.6$$

Here we choose N = 8 in this case. We will see later on how it affects the calculation.

Figure 51. The Drain−Source Wave Shall Always be Positive



design, we have selected our maximum voltage around 650 V (at = 375 V dc). This voltage is given by the clamp installed from the drain to

MOSFET Protection

As in any flyback design, it is important to limit the drain excursion to a safe value, e.g. below the MOSFET BV_{DSS} which is 700 V. Figure 53 **a−b−c** present possible implementations:

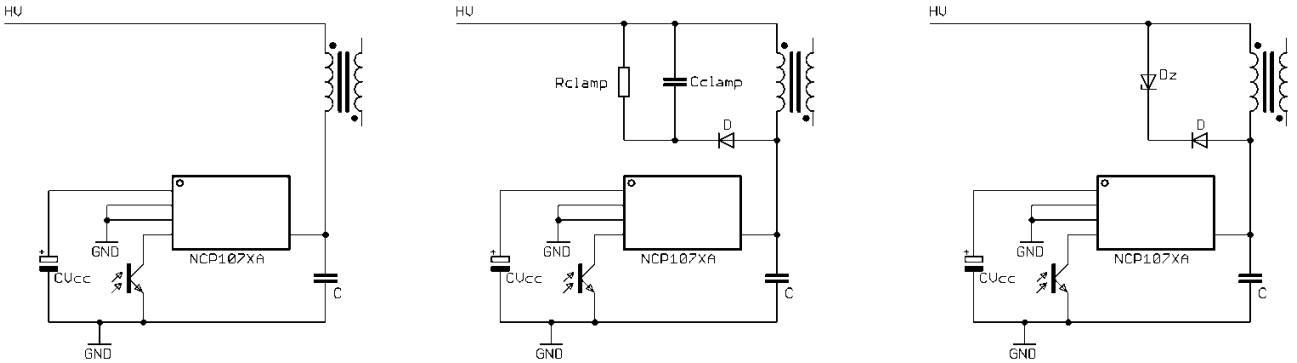


Figure 53. Different Options to Clamp the Leakage Spike

: the simple capacitor limits the voltage according to

Package Type	Shipping
PDIP8 (Less pin#6)	50 Units / Rail
PDIP8 (Less pin#6)	
PDIP8 (Less pin#3)	
PDIP8 (Less pin#3)	
PDIP8 (Less pin#3)	
PDIP8 (Less pin#6)	
PDIP8 (Less pin#6)	
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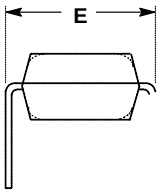
PDIP8 (Less pin#3)	

PDIP−7 (PDIP−8 LESS PIN 6)



GENERIC
MARKING DIAGRAM*