

R18

Figure 1. Typical Application Example

PIN FUNCTION DESCRIPTION

Pin #	Pin Name	Function	Pin Description
1	CSS(dis)	Soft start charge	Soft start capacitor discharge pin. Connect to the soft start capacitor to reset it before startup or during overload conditions.
2	Fmax	Maximum frequency clamp	A resistor sets the maximum frequency excursion
3	Ctimer	Timer duration	Sets the timer duration in presence of a fault
4	Rt	Minimum frequency clamp	Connecting a resistor to this pin, sets the minimum oscillator frequency reached for $V_{FB} = 1 V$.
5	BO		

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Figure 2. Internal Circuit Architecture (NCP1397A)

NCP1397A/B, NCV1397A/B

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
High Voltage bridge pin, pin 14	V_{BRIDGE}	[REDACTED]	V
Floating supply voltage, ground referenced	V_{BOOT}	0 to 20	V
High side output voltage	$V_{\text{DRV(HI)}}$	V_{BRIDGE} $V_{\text{BOOT}}+0.3$	V
Low side output voltage	$V_{\text{DRV(LO)}}$	[REDACTED] c+0.3	V
Allowable output slew rate	dV_{BRIDGE}/dt	50	V/ns
Power Supply voltage, pin 12	V_{CC}	20	V
Maximum voltage, all pins (except pin 11 and 10)	[REDACTED]	[REDACTED]	V
Thermal Resistance Junction [REDACTED] version	$R_{\theta\text{JA}}$	130	C/W
Storage Temperature Range	[REDACTED]	[REDACTED] 50	C
ESD Capability, Human Body Model (HBM) (All pins except HV pins)	[REDACTED]	2	kV
ESD Capability, Machine Model (MM)	[REDACTED]	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- This device(s) contains ESD protection and exceeds the following tests:
 Human Body Model 2000 V per JEDEC Standard JESD22 [REDACTED]
 Machine Model 200 V per JEDEC Standard JESD22 [REDACTED]
- This device meets latchup tests defined by JEDEC Standard JESD78.


NCP1397A/B, NCV1397A/B

ELECTRICAL CHARACTERISTICS

(For typical values $T_J = 25\text{ C}$, for min/max values $T_J =$ [redacted] 125 C , Max $T_J = 150\text{ C}$, $V_{CC} = 12\text{ V}$ unless otherwise noted)

Symbol

ELECTRICAL CHARACTERISTICS (continued)

(For typical values $T_J = 25\text{ C}$, for min/max values $T_J =$ )

NCP1397A/B, NCV1397A/B

TYPICAL CHARACTERISTICS

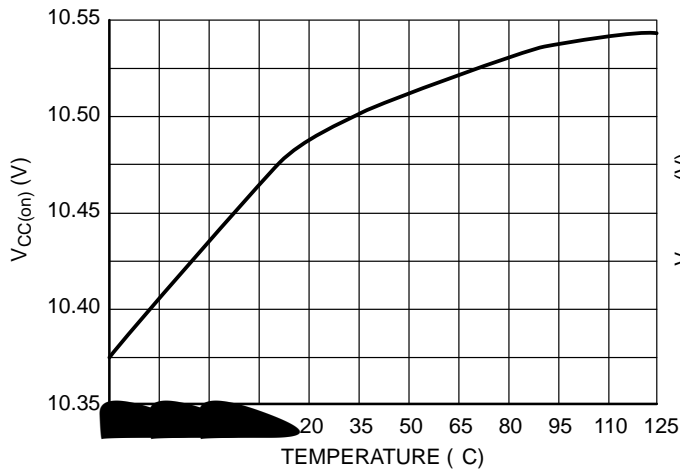


Figure 4. $V_{CC(on)}$ Threshold

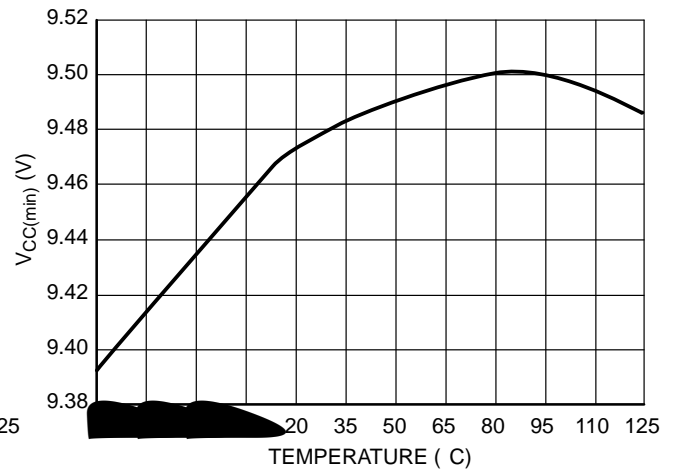


Figure 5. $V_{CC(min)}$ Threshold

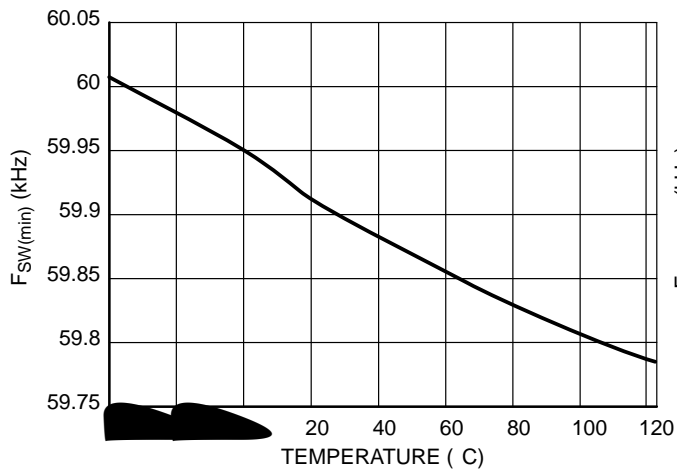


Figure 6. $F_{SW(min)}$ Frequency Clamp

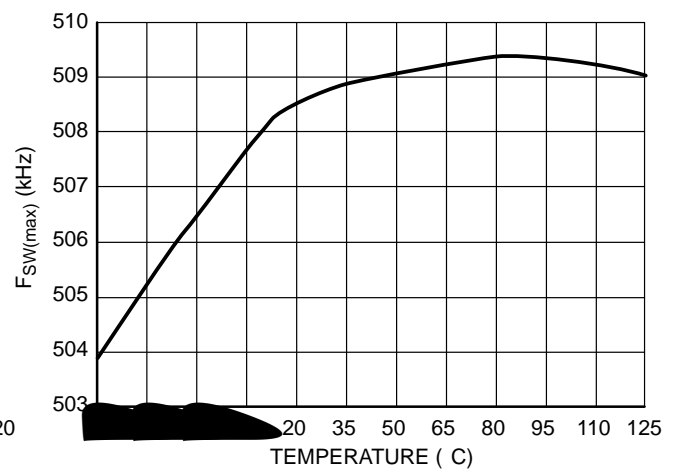


Figure 7. $F_{SW(max)}$ Frequency Clamp

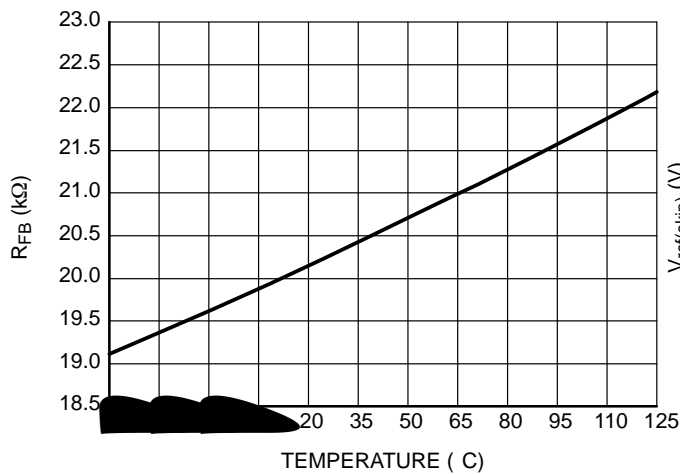


Figure 8. Pulldown Resistor (R_{FB})

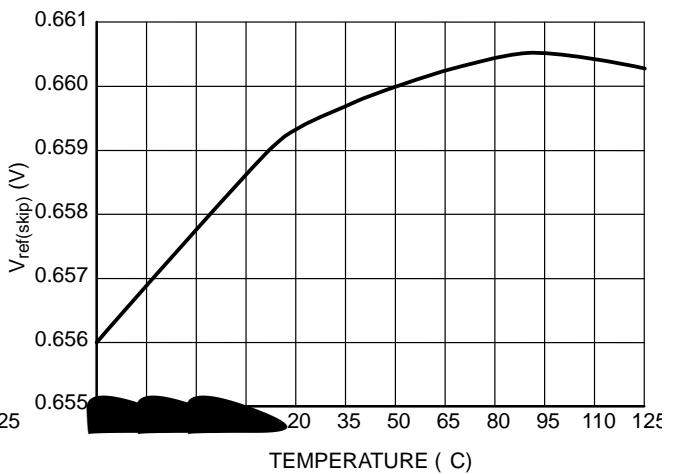


Figure 9. Skip/Disable Threshold ($V_{ref(skip)}$)

NCP1397A/B, NCV1397A/B

TYPICAL CHARACTERISTICS

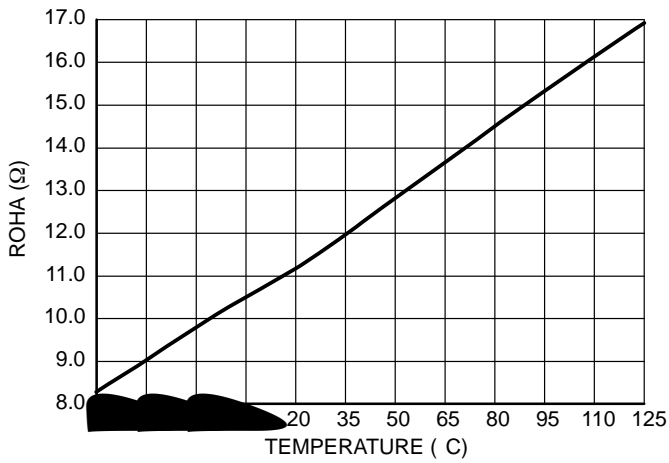


Figure 10. Source Resistance (ROH)

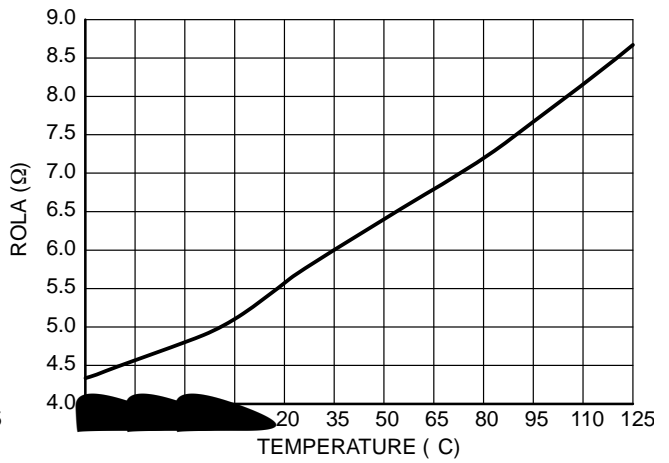


Figure 11. Sink Resistance (ROL)

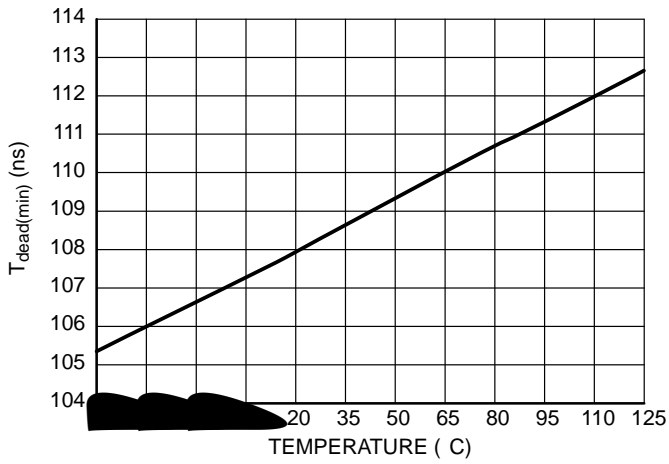


Figure 12. T_{dead}(min)

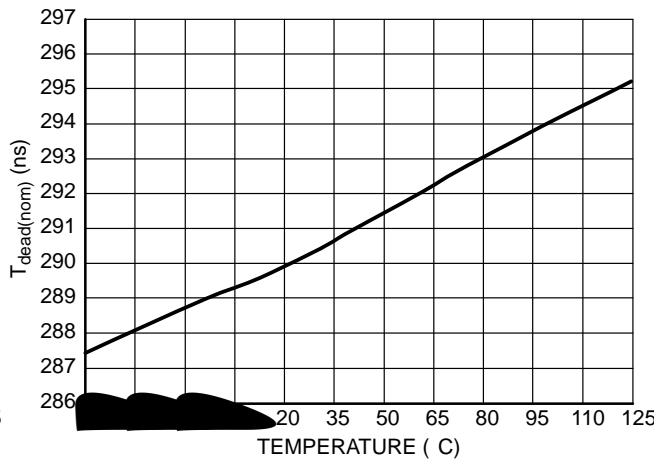


Figure 13. T_{dead}(nom)

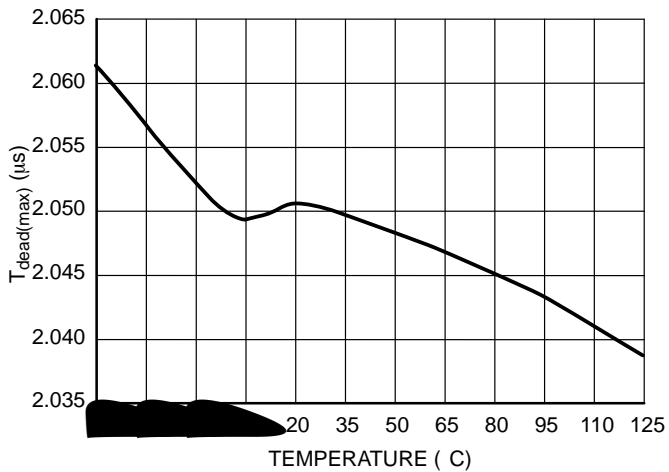


Figure 14. T_{dead}(max)

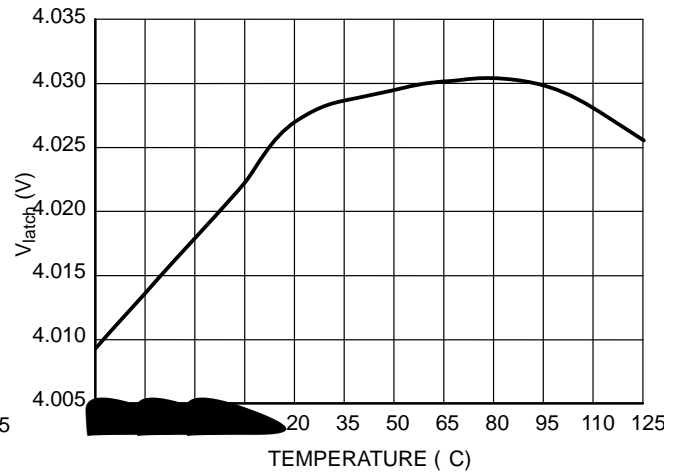


Figure 15. Latch Level (V_{latch})

NCP1397A/B, NCV1397A/B

TYPICAL CHARACTERISTICS

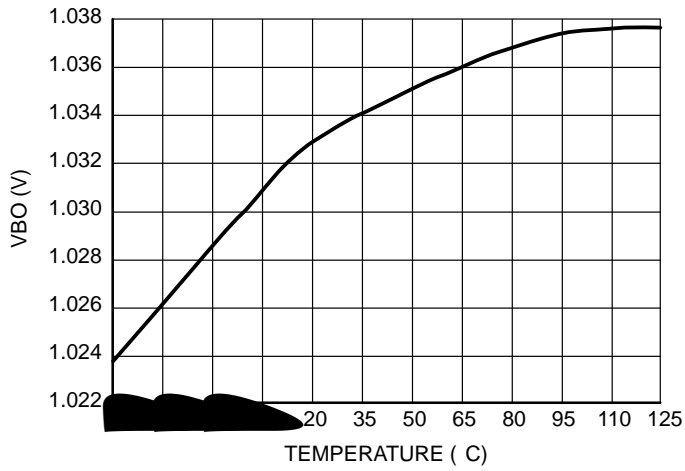


Figure 16. Brown-Out Reference (VBO)

TYPICAL CHARACTERISTICS

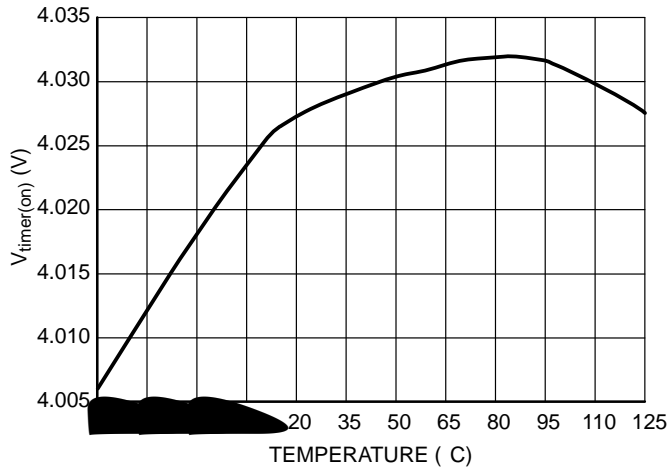


Figure 22. Fault Timer Ending Voltage
($V_{\text{timer(on)}}$)

NCP1397A/B, NCV1397A/B

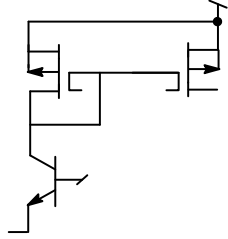


Figure 25. The Simplified VCO Architecture

This techniques allows us to detect a fault on the converter in case the FB pin cannot rise above 0.3 V (to actually close the loop) in less than a duration imposed by the programmable timer. Please refer to the fault section for detailed operation of this mode.

As shown on Figure 26, the internal dynamics of the VCO control voltage will be constrained between 0.5 V and 2.3 V, whereas the feedback loop will drive Pin 6 (FB) between 1.1 V and 5.3 V. If we take the default FB pin excursion numbers, 1.1 V = 50 kHz, 5.3 V = 500 kHz, then the VCO maximum slope will be:

$$\frac{500 \text{ k} - 50 \text{ k}}{4.2} = 107 \text{ kHz/V}$$

Figures 27 and 28 portray the frequency evolution depending on the feedback pin voltage level in a different frequency clamp combination.

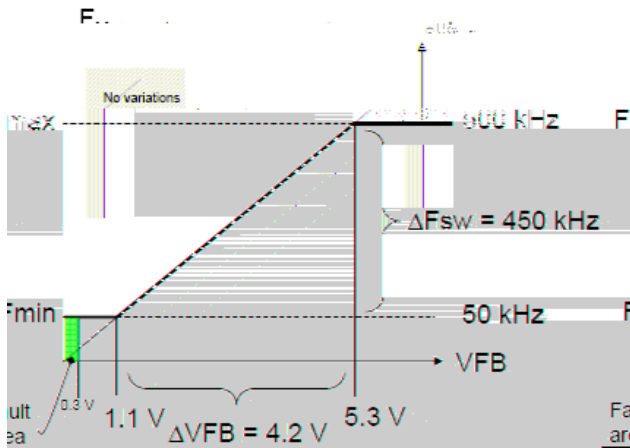


Figure 27. Maximal Default Excursion,
 $R_t = 41 \text{ k}\Omega$ on Pin 4 and $R_{F(\text{max})} = 1.9 \text{ k}\Omega$ on Pin 2

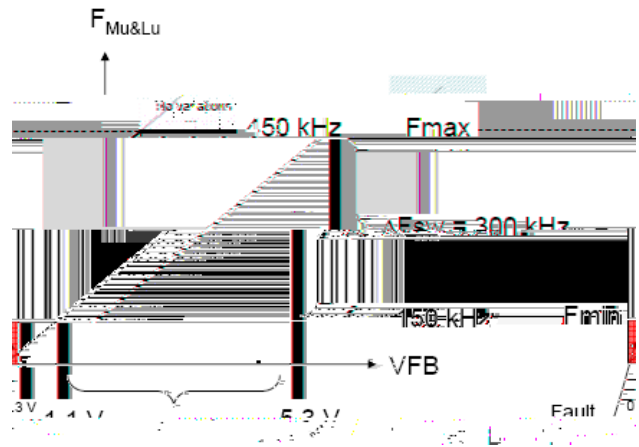


Figure 28. Here a Different Minimum Frequency was Programmed as well as a Maximum Frequency Excursion

Please note that the previous small-signal VCO slope has now been reduced to $300\text{k} / 4.1 = 71 \text{ kHz/V}$ on M_{upper} and M_{lower} outputs. This offers a mean to magnify the feedback excursion on systems where the load range does not generate a wide switching frequency excursion. Due to this option, we will see how it becomes possible to observe the feedback level and implement skip cycle at light loads. It is important to note that the frequency evolution does not have a real linear relationship with the feedback voltage. This is due to the deadtime presence which stays constant as the switching period changes.

The selection of the three setting resistors (F_{max} , F_{min} and deadtime) requires the usage of the selection charts displayed below:

NCP1397A/B, NCV1397A/B

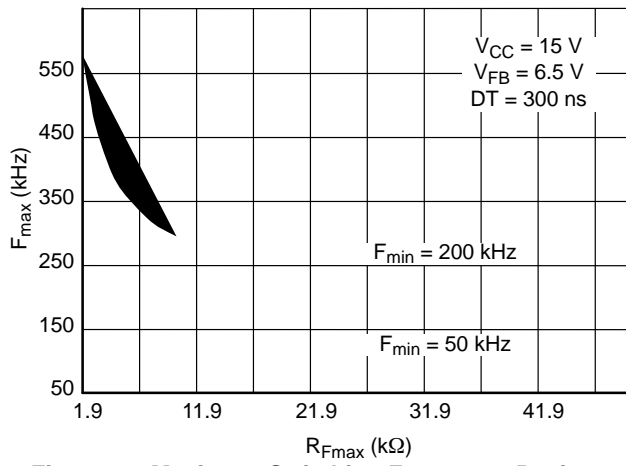


Figure 29. Maximum Switching Frequency Resistor Selection Depending on the Adopted Minimum Switching Frequency

NCP1397A/B, NCV1397A/B

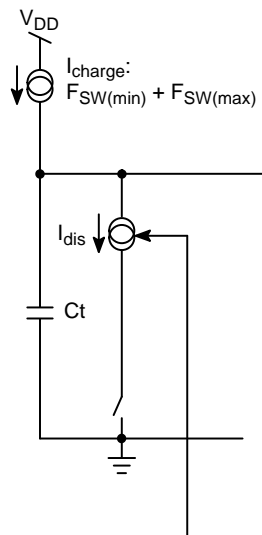


Figure 36. Dead-time Generation

NCP1397A/B, NCV1397A/B

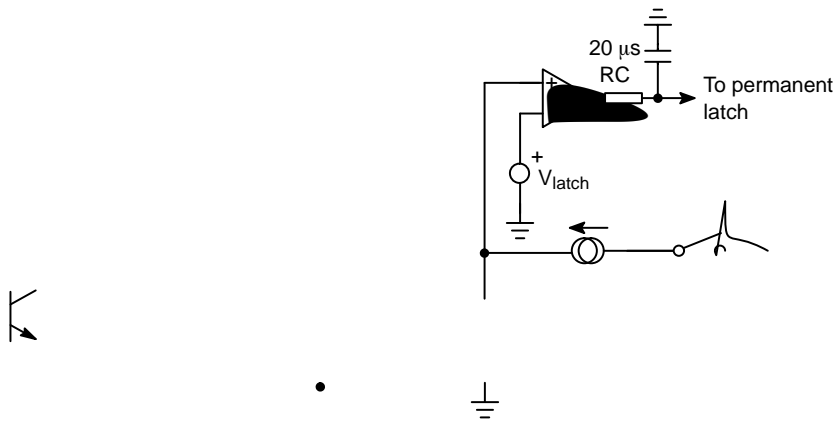


Figure 42. Adding a Comparator on the BO Pin Offers a way to Latch-off the Controller

NCP1397A/B, NCV1397A/B

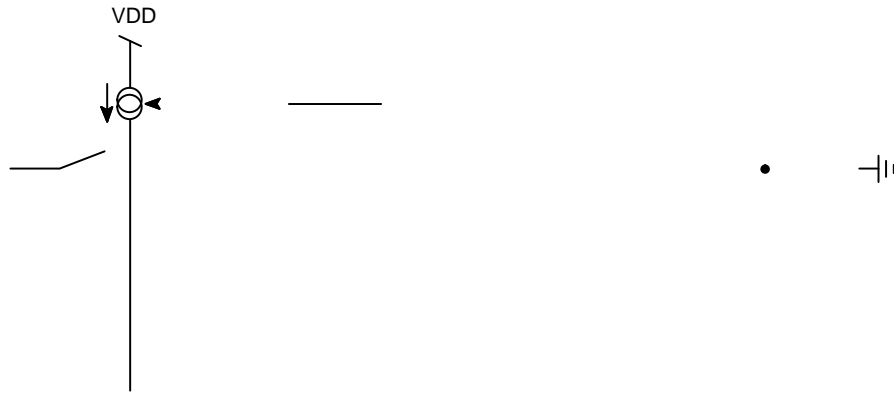


Figure 44. Fault Input Logic for NCP1397B

NCP1397A/B, NCV1397A/B

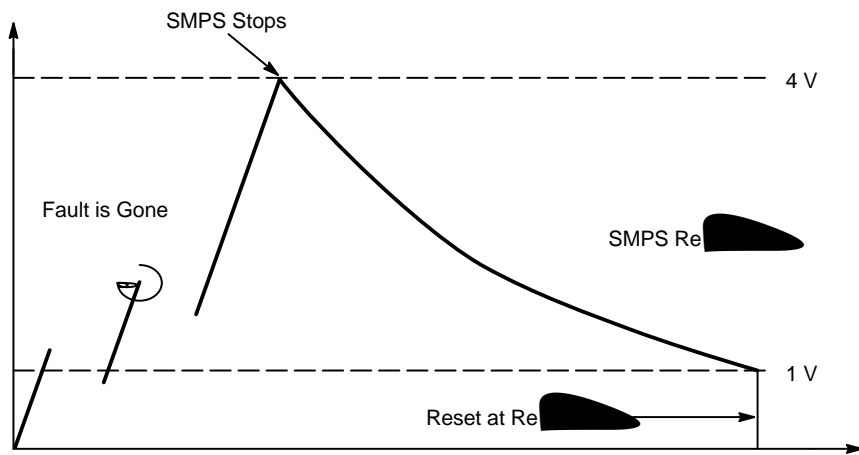


Figure 45. A Resistor Can Easily Program the Capacitor Discharge Time

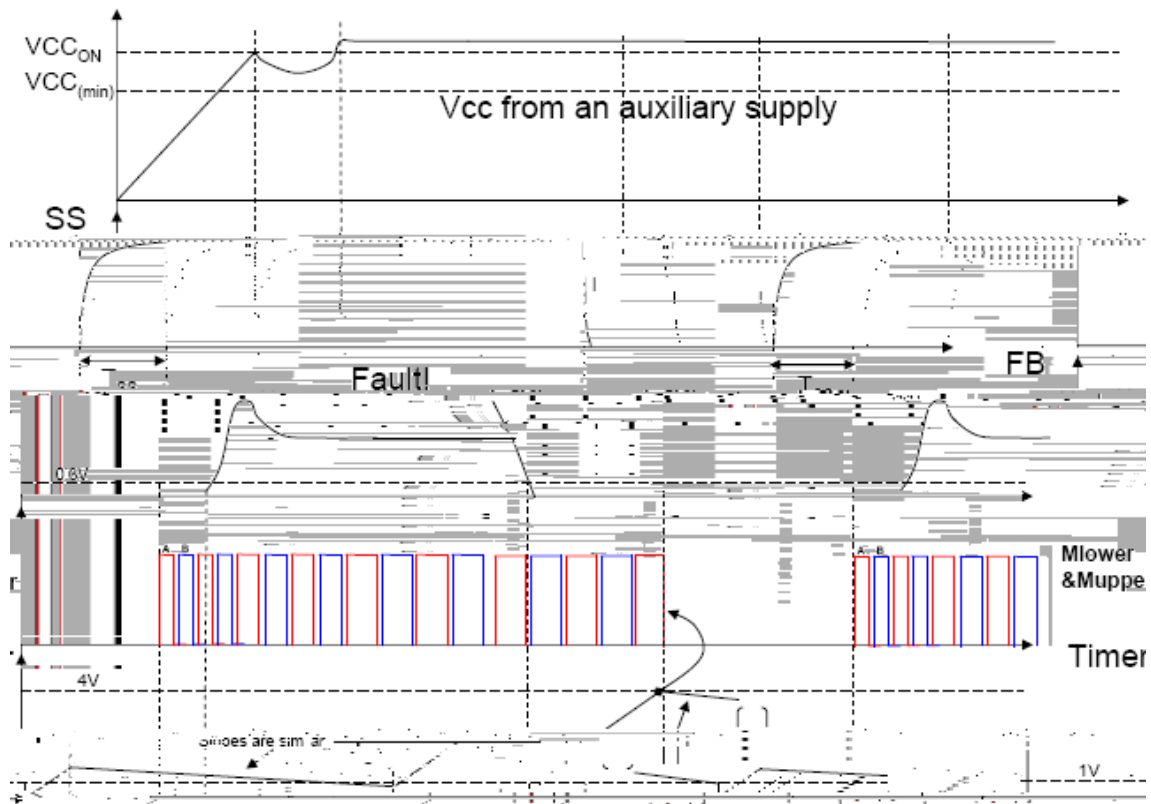


Figure 47. At Power On, Output A is First Activated and the Frequency Slowly Decreases Based on the Soft-Start Capacitor Voltage



Figure 47 depicts an auto-recovery situation, where the timer has triggered the end of output pulses. In that case, the V_{CC} level was given by an auxiliary power supply, hence its stability during the hiccup. A similar situation can arise if the user selects a more traditional startup method, with an auxiliary winding. In that case, the $V_{CC(min)}$

NCP1397A/B, NCV1397A/B


The device incorporates an upper UVLO circuitry that makes sure enough V_{gs} is available for the upper side MOSFET. The B and A outputs are delivered by the internal logic, as Figure 43 testifies. A delay is inserted in the lower rail to ensure good matching between these propagating signals.

As stated in the maximum rating section, the floating portion can go up to 600 VDC and makes the IC perfectly suitable for offline applications featuring a 400 V PFC front-end stage.

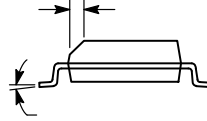
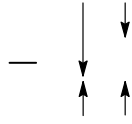
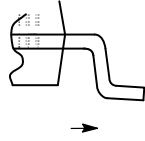
ORDERING INFORMATION

Device	Package	Shipping†
NCP1397ADR2G	SOIC  Pin 13 (Pb )	2500 / Tape & Reel
NCV1397ADR2G*		
NCP1397BDR2G		
NCV1397BDR2G*		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC  alified and PPAP Capable.

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