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# 1632

The NCP1632 integrates a dual MOSFET driver for interleaved PFC applications. Interleaving consists of paralleling two small stages in lieu of a bigger one, more difficult to design. This approach has several merits like the ease of implementation, the use of smaller components or a better distribution of the heating.

Also, Interleaving extends the power range of Critical Conduction Mode that is an efficient and cost−effective technique (no need for low $t_{rr}$ diodes). In addition, the NCP1632 drivers are 180° phase shifted for a significantly reduced current ripple.

Housed in a SOIC16 package, the circuit incorporates all the features necessary for building robust and compact interleaved PFC stages, with a minimum of external components.

### General Features

- Near−Unity Power Factor
- Substantial 180° Phase Shift in All Conditions Including Transient Phases
- Frequency Clamped Critical Conduction Mode (**FCCrM**

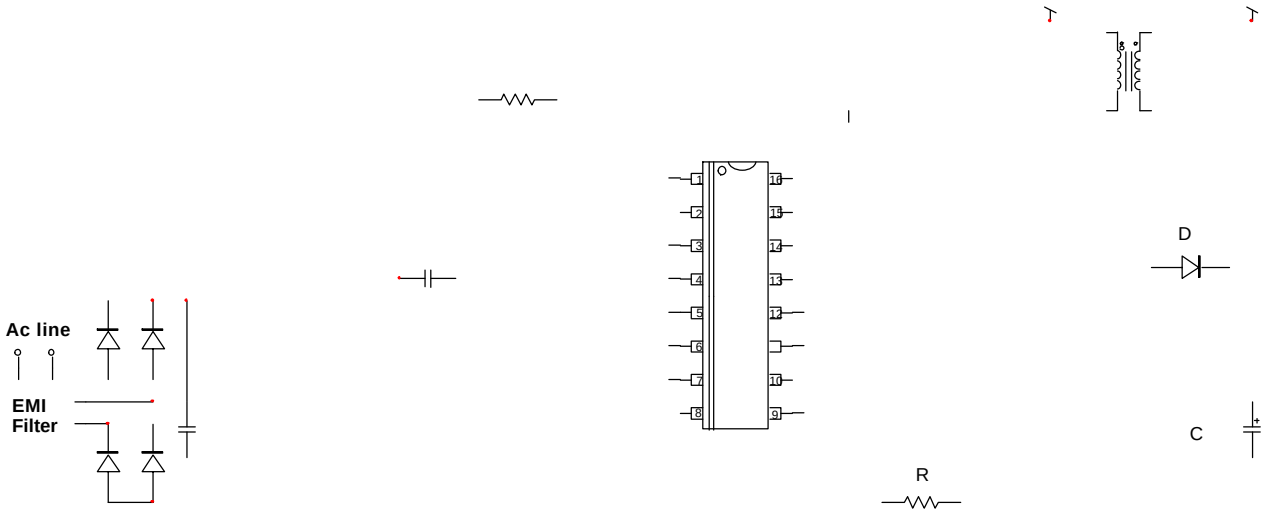



**Figure 1. Typical Application Schematic**

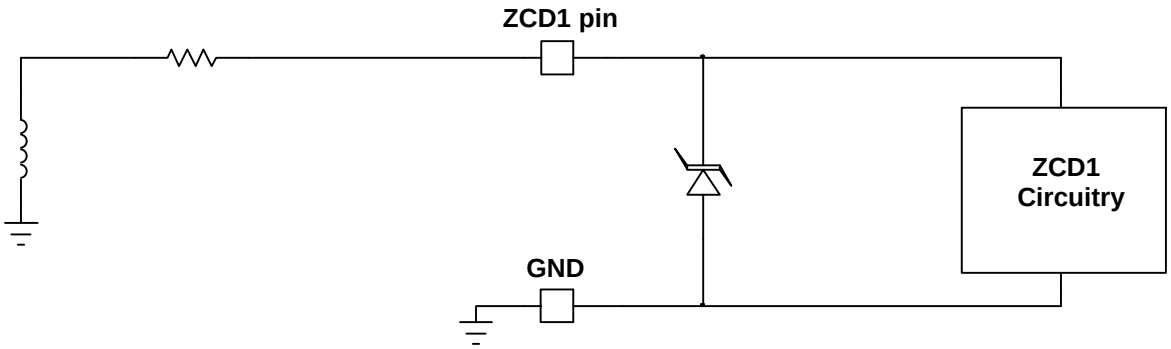

ZCD1 pin
ZCD1
Circuitry
GND

**Table 2. TYPICAL ELECTRICAL CHARACTERISTICS TABLE**

(Conditions: $V_{CC}$ = 15 V, $V_{pin7}$ = 2 V, $V_{pin10}$ = 0 V, $T_J$ from −40°C, to +125°C, unless otherwise specified)

| Characteristics | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **STARTUP AND SUPPLY CIRCUITS** | | | | | | |
| Supply Voltage | | | | | | V |
| Startup Threshold | $V_{CC}$ increasing | $V_{CC(on)}$ | 11 | 12 | 13 | |
| Minimum Operating Voltage | $V_{CC}$ decreasing | $V_{CC(off)}$ | 9.4 | 10 | 10.4 | |
| Hysteresis $V_{CC(on)} - V_{CC(off)}$ | | $V_{CC(hyst)}$ | 1.5 | 2.0 | − | |
| Internal Logic Reset | $V_{CC}$ decreasing | $V_{CC(reset)}$ | 4.0 | 6.0 | 7.5 | |
| Startup current | $V_{CC}$ = 9.4 V | $I_{CC(start)}$ | − | 50 | 100 | μA |
| Supply Current<br>Device Enabled/No output load on pin6<br>Current that discharges $V_{CC}$ | | | | | | |

**Table 2. TYPICAL ELECTRICAL CHARACTERISTICS TABLE** (continued)
(Conditions: $V_{CC}$ = 15 V, $V_{pin7}$ = 2 V, $V_{pin10}$ = 0 V, $T_J$ from −40°C, to +125°C, unless otherwise specified)

| Characteristics | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **GATE DRIVE (Note 8)** | | | | | | |
| Drive Current Capability (Note 6) | | | | | | mA |
| DRV1 Sink | $V_{DRV1}$ = 10 V | $I_{SNK1}$ | − | 800 | − | |
| DRV1 Source | $V_{DRV1}$ = 0 V | $I_{SRC1}$ | − | 500 | − | |
| DRV2 Sink | $V_{DRV2}$ = 10 V | $I_{SNK2}$ | − | 800 | − | |
| DRV2 Source | $V_{DRV2}$ = 0 V | $I_{SRC2}$ | − | 500 | − | |
| Rise Time | | | | | | ns |
| DRV1 | $C_{DRV1}$ = 1 nF, $V_{DRV1}$ = 1 to 10 V | $t_{r1}$ | − | 40 | − | |
| DRV2 | $C_{DRV2}$ = 1 nF, $V_{DRV2}$ = 1 to 10 V | $t_{r2}$ | − | 40 | − | |
| Fall Time | | | | | | ns |
| DRV1 | $C_{DRV1}$ = 1 nF, $V_{DRV1}$ = 10 to 1 V | $t_{f1}$ | – | 20 | – | |
| DRV2 | $C_{DRV2}$ = 1 nF, $V_{DRV2}$ = 10 to 1 V | $t_{f2}$ | – | 20 | – | |
| **REGULATION BLOCK** | | | | | | |
| Feedback Voltage Reference | | $V_{REF}$ | 2.44 | 2.50 | 2.56 | V |
| Error Amplifier Source Current Capability | @ $V_{pin2}$ = 2.4 V | $I_{EA(SRC)}$ | | −20 | | μA |
| Error Amplifier Sink Current Capability | @ $V_{pin2}$ = 2.6 V | $I_{EA(SNK)}$ | | +20 | | |
| Error Amplifier Gain | | $G_{EA}$ | 115 | 200 | 285 | μS |
| Pin 5 Source Current when ($V_{out(low)}$ Detect) is activated | pfcOK high<br>pfcOK low | $I_{Control(boost)}$ | 175<br>55 | 220<br>70 | 265<br>85 | μA |
| Pin2 Bias Current | $V_{pin2}$ = 2.5 V | $I_{FB(bias)}$ | −500 | | 500 | nA |
| Pin 5 Voltage: | @ $V_{pin2}$ = 2.4 V<br>@ $V_{pin2}$ = 2.6 V | $V_{Control(clamp)}$<br>$V_{Control(MIN)}$<br>$V_{Control(range)}$ | −<br>−<br>2.8 | 3.6<br>0.6<br>3 | −<br>−<br>3.5 | V |
| Ratio ($V_{out(low)}$ Detect Threshold / $V_{REF}$) (Note 6) | FB falling | $V_{out(low)}/V_{REF}$ | 95.0 | 95.5 | 96.0 | % |
| Ratio ($V_{out(low)}$ Detect Hysteresis / $V_{REF}$) (Note 6) | FB rising | $H_{out(low)}/V_{REF}$ | − | − | 0.5 | % |
| **SKIP MODE** | | | | | | |
| Duty Cycle | $V_{FB}$ = 3 V | $D_{MIN}$ | − | − | 0 | % |
| **RAMP CONTROL (valid for the two phases)** | | | | | | |
| Maximum DRV1 and DRV2 On−Time (FB pin grounded) | $V_{pin7}$ = 1.1 V, $I_{pin3}$ = 50 μA (Note 6)<br>$V_{pin7}$ = 1.1 V, $I_{pin3}$ = 200 μA<br>$V_{pin7}$ = 2.2 V, $I_{pin3}$ = 100 μA<br>$V_{pin7}$ = 2.2 V, $I_{pin3}$ = 400 μA | $t_{on1}$<br>$t_{on2}$<br>$t_{on3}$<br>$t_{on4}$ | 14.5<br>1.10<br>4.00<br>0.34 | 19.5<br>1.35<br>5.00<br>0.41 | 22.5<br>1.60<br>6.00<br>0.50 | μs |
| Pin 3 voltage | $V_{BO}$ = $V_{pin7}$ = 1.1 V, $I_{pin3}$ = 50 μA<br>$V_{BO}$ = $V_{pin7}$ = 1.1 V, $I_{pin3}$ = 200 μA<br>$V_{BO}$ = $V_{pin7}$ = 2.2 V, $I_{pin3}$ = 50 μA<br>$V_{BO}$ = $V_{pin7}$ = 2.2 V, $I_{pin3}$ = 200 μA | $V_{Rt1}$<br>$V_{Rt2}$<br>$V_{Rt3}$<br>$V_{Rt4}$ | 1.068<br>1.068<br>2.165<br>2.165 | 1.096<br>1.096<br>2.196<br>2.196 | 1.126<br>1.126<br>2.228<br>2.228 | V |
| Maximum $V_{ton}$ Voltage | Not tested | $V_{ton(MAX)}$ | | 5 | | V |
| Pin 3 Current Capability | | $I_{Rt(MAX)}$ | 1 | − | − | mA |
| Pin 3 sourced current below which the controller is OFF | | $I_{Rt(off)}$ | | 7 | | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. DRV1 and DRV2 pulsating at half this frequency, that is, 65 kHz.
6. Not tested. Guaranteed by design.
7. Not tested. Guaranteed by design and characterization.
8. Guaranteed by design, the VCC pin can handle the double of the DRV peak source current, that is, 1 A typically.

**Table 2. TYPICAL ELECTRICAL CHARACTERISTICS TABLE**

**Table 3. DETAILED PIN DESCRIPTION**

| Pin number | Name | Function |
|---|---|---|
| 1 | ZCD2 | This is the zero current detection pin for phase 2 of the interleaved PFC stage. It is designed to monitor the voltage of an auxiliary winding to detect the inductor core reset and the valley of the MOSFET drain source voltage |
| 2 | FB | This pin receives the portion of the PFC stage output voltage for regulation. $V_{FB}$ is also monitored by the dynamic response enhancer (DRE) which drastically speeds−up the loop response when the output voltage drops below 95.5 % of the wished level. |
| 3 | $R_T$ | The resistor placed between pin 3 and ground adjusts the maximum on−time in both phases, and hence the maximum power that can be delivered by the PFC stage. |
| 4 | OSC | Oscillator pin. The oscillator sets the maximum switching frequency, particularly in medium− and light−load conditions when frequency foldback is engaged. |
| 5 | $V_{CONTROL}$ | The error amplifier output is available on this pin for loop compensation. The capacitors and resistor connected between this pin and ground adjusts the regulation loop bandwidth that is typically set below 20 Hz to achieve high Power Factor ratios. Pin5 is grounded when the circuit is off so that when it starts operation, the power increases gradually (soft−start). |
| 6 | FFOLD (Freq. Foldback) | This pin sources a current proportional to the input current. Placing a resistor and a capacitor between the FFOLD pin and GND, we obtain the voltage representative of the line current magnitude necessary to control the frequency foldback characteristics. |
| 7 | BO (Brown−out Protection) | Apply an averaged portion of the input voltage to detect brown−out conditions when $V_{BO}$ drops below 1 V. A 500−ms internal delay blanks short mains interruptions to help meet hold−up time requirements. When it detects a brown−out condition, the circuit stops pulsing and grounds the “pfcOK” pin to disable the downstream converter. Also an internal 7−μA current source is activated to offer a programmable hysteresis.<br>The pin2 voltage is internally re−used for feed−forward.<br>Ground pin 2 to disable the part. |
| 8 | OVP / UVP | The circuit turns off when $V_{pin8}$ goes below $V_{UVP}$ (300 mV typically – UVP protection) and disables the drive when the pin voltage exceeds $V_{OVP}$ (2.5 V typically − OVP protection). |
| 9 | CS (current sense) | The CS pin monitors a negative voltage proportional to the input current to limit the maximum current flowing in the phases. The NCP1632 also uses the CS information to prevent the PFC stage from starting operation in presence of large in−rush currents. |
| 10 | Latch | Apply a voltage higher than $V_{STDWN}$ (166 mV typically) to latch−off the circuit. The device is reset by unplugging the PFC stage (practically when the circuit detects a brown−out detection) or by forcing the circuit $V_{CC}$ below $V_{CC}$RST (4 V typically). Operation can then resume when the line is applied back. |
| 11 | DRV2 | This is the gate drive pin for phase 2 of the interleaved PFC stage. The high−current capability of the totem pole gate drive (+0.5/−0.8A) makes it suitable to effectively drive high gate charge power MOSFETs. |
| 12 | $V_{CC}$ | This pin is the positive supply of the IC. The circuit starts to operate when $V_{CC}$ exceeds 12 V and turns off when $V_{CC}$ goes below 10 V (typical values). After start−up, the operating range is 10.5 V up to 20 V. |
| 13 | GND | Connect this pin to the pre−converter ground. |
| 14 | DRV1 | This is the gate drive pin for phase 1 of the interleaved PFC stage. The high−current capability of the totem pole gate drive (+0.5/−0.8A) makes it suitable to effectively drive high gate charge power MOSFETs. |
| 15 | REF5V / pfcOK | The pin15 voltage is high (5 V typically) when the PFC stage is in a normal, steady state situation and low otherwise. This signal serves to “inform” the downstream converter that the PFC stage is ready and that hence, it can start operation. |
| 16 | ZCD1 | This is the zero current detection pin for phase 1 of the interleaved PFC stage. It is designed to monitor the voltage of an auxiliary winding to detect the inductor core reset and the valley of the MOSFET drain source voltage |

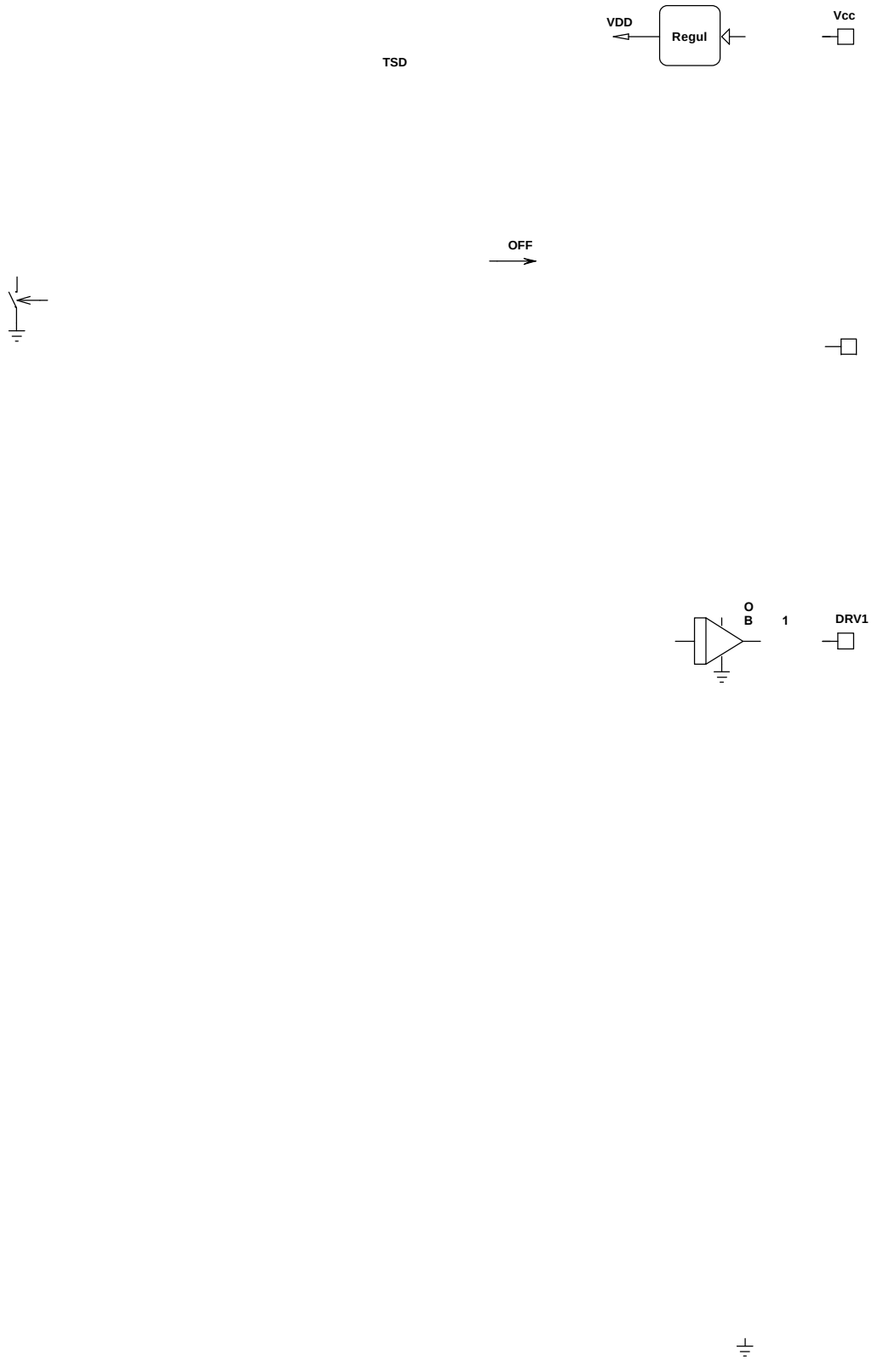



**Figure 3. Block Diagram**

Furthermore, if the two channels are properly operated out−of−phase, a large part of the switching−frequency ripple currents generated by each individual branch cancel when they add within the EMI filter and the bulk capacitors. As a result, EMI filtering is significantly eased and the bulk capacitor rms current is drastically reduced. Interleaving therefore extends the CrM power range by sharing the task between the two phases and by allowing for a reduced input current ripple and a minimized bulk capacitor rms current.

This is why this approach which at first glance, may appear more costly than the traditional 1−phase solution can actually be extremely cost−effective and efficient for powers above 300 watts. And even less for applications like LCD and Plasma TV applications where the need for smaller components, although more numerous, helps meet the required low−profile form−factors.

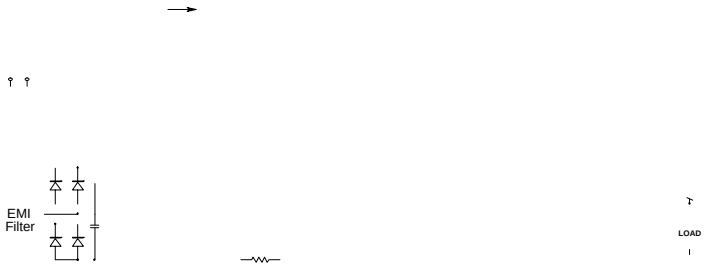



**Figure 4. Interleaved PFC Stage**

$V_{REGUL}$ is the signal derived from the regulation block which adjusts the on−time. This **onsemi** proprietary technique makes the NCP1632 able to support the Frequency Clamped Critical conduction mode of operation, that is, to operate in discontinuous− or in critical−conduction mode according to the conditions, without degradation of the power factor. Critical conduction mode is naturally obtained when the inductor current cycle is longer than the minimum period controlled by the oscillator. Discontinuous conduction mode is obtained in the opposite situation. In this case, the switching frequency is clamped.

Hence, the averaged current absorbed by one of the phase of the PFC converter:

$$I_{in(phase1)} = I_{in(phase2)} = \frac{V_{in}}{2L} \cdot \frac{C_t \cdot V_{REGUL}}{I_t} \quad \text{(eq. 4)}$$

Given the regulation low bandwidth of PFC systems, ($V_{CONTROL}$) and then ($V_{REGUL}$) are slow varying signals. Hence, the line current absorbed by each phase is:

$$I_{in(phase1)} = I_{in(phase2)} = k \cdot V_{in} \quad \text{(eq. 5)}$$

Where k is a constant ( $k = \left\lceil \frac{C_t \cdot V_{REGUL}}{2 \cdot L \cdot I_t} \right\rceil$ ).

Hence, the input current is then proportional to the input voltage and the ac line current is properly shaped.

This analysis is valid for DCM but also CrM which is just a particular case of this functioning where ($t_3$ = 0). As a result, the NCP1632 automatically adapts to the conditions and jumps from DCM and CrM (and vice versa) without power factor degradation and without discontinuity in the power delivery.

The total current absorbed by the two phases is then:

$$I_{in(total)} = \frac{C_t \cdot V_{REGUL}}{L \cdot I_t} \cdot V_{in} \quad \text{(eq. 6)}$$

This leads to the following line rms current and average input power:

$$I_{in(rms)} = \frac{C_t \cdot V_{REGUL}}{L \cdot I_t} \cdot V_{in(rms)} \quad \text{(eq. 7)}$$

$$P_{in(avg)} = \frac{C_t \cdot V_{REGUL}}{L \cdot I_t} \cdot V_{in(rms)}^{2} \quad \text{(eq. 8)}$$

*Feedforward:*

The $C_t$ timing capacitors (one per phase) are internal and are well matched for an optimal current balancing between the two branches of the interleaved converter.

As detailed in the brown−out section, the $I_t$ current is internally processed to be proportional to the square of the voltage applied to the BO pin (pin 7). Since the BO pin is designed to receive a portion of the average input voltage, the $I_t$ current is proportional to the square of the line magnitude which provides feedforward.

In a typical application, the BO pin voltage is hence:

$$V_{pin7} = \frac{2\sqrt{2}V_{in(rms)}}{\pi} \frac{R_{bo2}}{R_{bo1} + R_{bo2}} \quad \text{(eq. 9)}$$

where $R_{bo1}$ and $R_{bo2}$ are the scaling down resistors for BO sensing (see brown−out section)

In addition, $I_t$ is programmed by the pin 3 resistor so that the maximum on−time obtained when $V_{REGUL}$ is max (1.66 V) is given by:

$$T_{on,max}(\mu s) \cong 50 \cdot 10^{-9} \cdot \frac{R_t^{2}}{V_{pin7}^{2}} \quad \text{(eq. 10)}$$

### Regulation Block and Low Output Voltage Detection

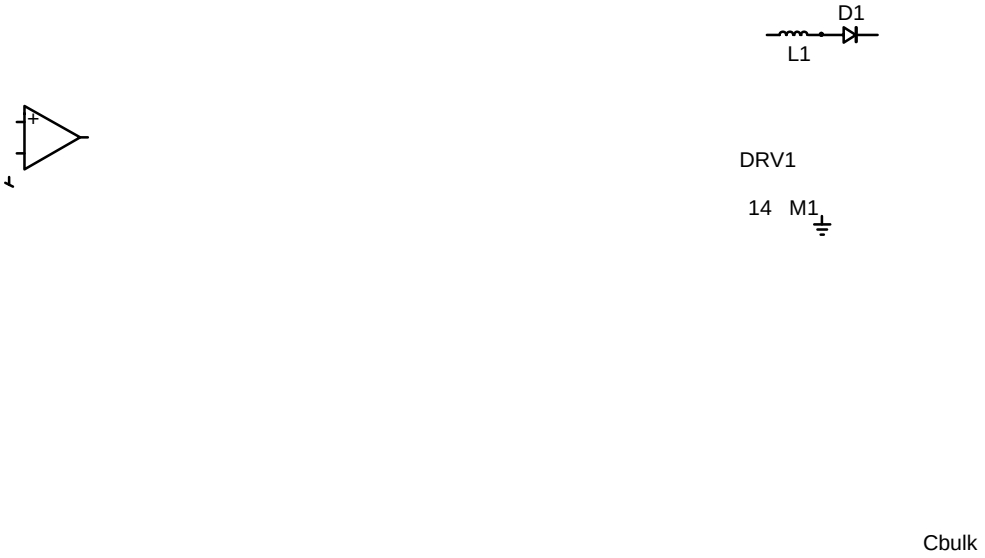
A trans−conductance error amplifier with access to the inverting input and output is provided. It features a typical trans−conductance gain of 200 μS and a typical capability of ±20 μA. The output voltage of the PFC stage is typically scaled down by a resistors divider and monitored by the inverting input (feed−back pin – pin2). The bias current is minimized (less than 500 nA) to allow the use of a high impedance feed−back network. The output of the error

zero. The NCP1632 detects this falling edge and prevents any new current cycle until it is detected.

Figure 9 shows how it is implemented.

For each phase, a ZCD comparator detects when the voltage of the ZCD winding exceeds its upper threshold (0.5 V typically). When this is the case, the coil is in demagnetization phase and the latch $L_{ZCD}$ is set. This latch is reset when the next driver pulse occurs. Hence the output of this latch ($Q_{ZCD}$) is high during the whole off−time (demagnetization time + any possible dead time). The output of the comparator is also inverted to form a signal which is AND'd with the $Q_{ZCD}$ output so that the AND gate output ($V_{ZCD}$) turns high when the $V_{AUX}$ voltage goes below zero (below the 0.25 V lower threshold of the ZCD comparator to be more specific). As a result, the ZCD circuitry detects the $V_{AUX}$ falling edge.

It is worth noting that as portrayed by Figure 10, $V_{AUX}$ is also representative of the MOSFET drain−source voltage ("$V_{DS}$"). More specifically, when $V_{AUX}$ is below zero, $V_{DS}$ is minimal (below the input voltage $V_{IN}$). That is why $V_{ZCD}$ is used to enable the driver so that the MOSFET turns on when its drain−source voltage is low. Valley switching reduces the losses and interference.



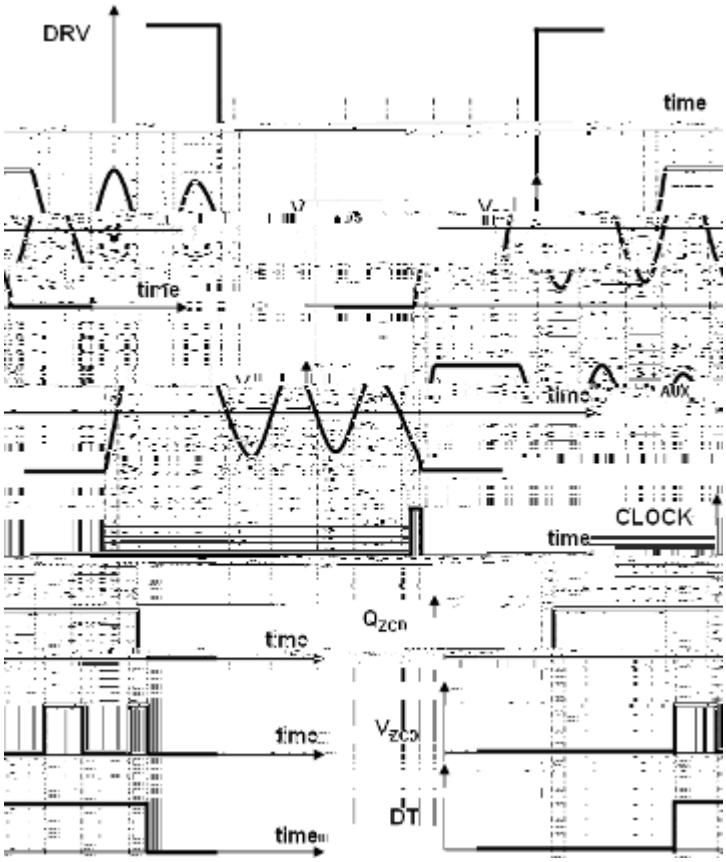



**Figure 10. Zero Current Detection Timing Diagram ($V_{AUX}$ is the Voltage Provided by the ZCD Winding)**

### Current Sense

The NCP1632 is designed to monitor a negative voltage proportional to the input current, i.e., the current drawn by the two interleaved branches ($I_{in}$). As portrayed by Figure 11, a current sense resistor ($R_{CS}$) is practically inserted in the return path to generate a negative voltage ($V_{CS}$) proportional to $I_{in}$.


**Figure 11. Current Sense Block**

voltage near zero. By inserting a resistor $R_{OCP}$ between the CS pin and $R_{CS}$, we adjust the current that is sourced by the CS pin ($I_{CS}$) as follows:

$$-\left(R_{CS} \cdot I_{in}\right) + \left(R_{OCP} \cdot I_{CS}\right) \cong 0 \quad \text{(eq. 13)}$$

Which leads to:

$$I_{CS} = \frac{R_{CS}}{R_{OCP}} I_{in} \quad \text{(eq. 14)}$$

In other words, the CS pin sources a current ($I_{CS}$) which is proportional to the input current.

Two functions use $I_{CS}$: the over current protection and the in−rush current detection.

The double feed−back configuration (Figure 13) offers some up−graded safety level as it protects the PFC stage even if there is a failure of one of the two feed−back arrangements. In this case:

The bulk regulation voltage (“$V_{out(nom)}$”) is:

$$V_{out(nom)} = \frac{R_{out1} + R_{out2}}{R_{out2}} \cdot V_{ref} \quad \text{(eq. 17)}$$

The OVP level (“$V_{out(ovp)}$”) is:

$$V_{out(ovp)} = \frac{R_{ovp1} + R_{ovp2}}{R_{ovp2}} \cdot V_{ref} \quad \text{(eq. 18)}$$

Where $V_{ref}$ is the internal reference voltage (2.5 V typically)

Now, if wished, one single feed−back arrangement is possible as portrayed by Figure 12. The regulation and OVP blocks having the same reference voltage ($V_{ref}$), the resistance ratio $R_{out2}$ over $R_{out3}$ adjusts the OVP threshold. More specifically,

The bulk regulation voltage (“$V_{out(nom)}$”) is:

$$V_{out(nom)} = \frac{R_{out1} + R_{out2} + R_{out3}}{R_{out2} + R_{out3}} \cdot V_{ref} \quad \text{(eq. 19)}$$

The OVP level (“$V_{out(ovp)}$”) is:

$$V_{out(ovp)} = \frac{R_{out1} + R_{out2} + R_{out3}}{R_{out2}} \cdot V_{ref} \quad \text{(eq. 20)}$$

The ratio OVP level over regulation level is:

$$\frac{V_{out(ovp)}}{V_{out(nom)}} = 1 + \frac{R_{out3}}{R_{out2}} \quad \text{(eq. 21)}$$

For instance, ($V_{out(nom)}$ = 105% · $V_{out(nom)}$) leads to: ($R_{out3}$ = 5% · $R_{out2}$).

When the circuit detects that the output voltage exceeds the OVP level, it maintains the power switch open to stop the power delivery.

**Oscillator Section – Phase Management**

The oscillator generates the clock signal that dictates the maximum switching frequency ($f_{osc}$) of the interleaved PFC stage. In other words, each of the two interleaved branches cannot operate above half the oscillator frequency ($f_{osc}$/2). The oscillator frequency ($f_{osc}$) is adjusted by the capacitor applied to OSC pin (pin 4). Typically, a 220 pF capacitor approximately leads to a 260 kHz oscillator operating frequency, i.e., to a 130 kHz clamp frequency for each branch.

As shown by Figure 14, a current source $I_{CH}$ (140 μA typically) charges the OSC pin capacitor until its voltage exceeds $V_{OSC(high)}$ (5 V typically). At that moment, the oscillator enters a discharge phase for which $I_{DISCH}$ (105 μA typ.) discharges the OSC pin capacitor. This sequence lasts until $V_{OSC}$ goes below the oscillator low threshold $V_{OSCL}$ and a new charging phase starts*. An internal signal (“*SYNC*” of Figure 19) is high during the discharge phase. A divider by two uses the *SYNC* information to manage the phases of the interleaved PFC: the first *SYNC* pulse sets “phase 1”, the second one, “phase 2”, the third one phase 1 again… etc.

According to the selected phase, *SYNC* sets the relevant “Clock generator latch” that will generate the clock signal (“*CLK*1” for phase 1, “*CLK*2” for phase 2) when *SYNC* drops to zero.

Actually, the drivers cannot turn on at this very moment if the inductor demagnetization is not complete. In this case, the clock signal is maintained high and the discharge time is prolonged although $V_{OSC}$ is below $V_{OSCL}$, until when the core being reset, the drive pin turns high. The prolonged OSC discharge ensures a substantial 180−degree phase shift in CrM, out−of−phase operation being in essence, guaranteed in DCM. In the two conditions (CrM or DCM), the interleaved operation is stable and robust.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**Figure 14. FFOLD Mode Management**

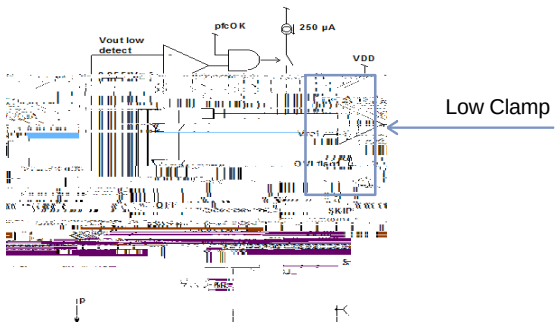



**Figure 21. $V_{CONTROL}$ Low Clamp**

The circuit consumption is minimized (below 1 mA) for a skipping period of time.

### PfcOK / REF5V Signal

The NCP1632 can communicate with the downstream converter. The signal “pfcOK/REF5V” is high (5 V) when the PFC stage is in nominal operation and low otherwise.

More specifically, “pfcOK/REF5V” is low:

- Whenever a major fault condition is detected which turns off the circuit, i.e.:
  - Incorrect feeding of the circuit (“UVLO” high). The UVLO signal turns high when $V_{CC}$ drops below $V_{CC(OFF)}$ (10 V typically) and remains high until $V_{CC}$ exceeds $V_{CC(ON)}$ (12 V typically).
  - Excessive die temperature detected by the thermal shutdown.
  - Under−Voltage Protection (“UVP” high)
  - Brown−out situation (“BONOK” high)
  - Latching−off of the circuit by an external signal applied to pin 10 and exceeding 166 mV (“STDWN” of the block diagram turns high).
  - Too low the current sourced by the $R_t$ pin (“$R_{t(open)}$”)
- During the PFC stage start−up, that is, until the output voltage reaches its regulation level. The start−up phase is detected by the latch “$L_{STUP}$” of the block diagram. “$L_{STUP}$” is in high state when the circuit enters or recovers operation after one of above major faults and resets when the error amplifier stops charging its output capacitor, that is, when the output voltage of the PFC stage has reached its desired regulation level. At that moment, “STUP” falls down to indicate the end of the start−up phase.

Finally, “pfcOK/REF5V” is high when the PFC output voltage is properly and safely regulated. “pfcOK/REF5V” should be used to allow operation of the downstream converter.

### Brown−Out Protection

The brown−out pin is designed to receive a portion of the input voltage ($V_{IN}$). As $V_{IN}$ is a rectified sinusoid, a capacitor must be applied to the BO pin so that $V_{BO}$ is proportional to the average value of $V_{IN}$.

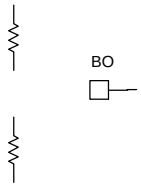



**Figure 22. Brown−out Block**

The BO pin voltage is used by two functions (refer to Figure 22):

- Feedforward. Generation of an internal current proportional to the input voltage average value ($I_{Rt}$). $V_{BO}$ is buffered and made available on the $R_t$ pin (pin 3). Hence, placing a resistor between pin 3 and ground, enables to adjust a current proportional to the average input voltage. This current ($I_{Rt}$) is internally copied and squared to form the charge current for the internal timing capacitor of each phase. Since this current is proportional to the square of the line magnitude, the conduction time is made inversely proportional to the line magnitude. This feed−forward feature makes the transfer function and the power delivery independent of the ac line level. Only the regulation output ($V_{REGUL}$) controls the power amount. Note that if the $I_{Rt}$ current is too low (below 7 μA typically), the controller goes in OFF mode to avoid damaging the MOSFETs with too long conduction time. In particular, this addresses the case when the $R_t$ pin is open.
- Brown−out protection. A 7 μA current source lowers the BO pin voltage when a brown−out condition is detected. This is for hysteresis purpose as required by this function. In traditional applications, the monitored voltage can be very different depending on the phase:
  - Before operation, the PFC stage is off and the input bridge acts as a peak detector (refer to Figure 23). As a consequence, the input voltage is approximately flat and nearly equates the ac line amplitude: $v_{in}(t) = \sqrt{2} \cdot V_{in,rms}$, where $V_{in,rms}$ is the rms voltage of the line. Hence, the voltage applied to the BO pin (pin 7) is:
    $$V_{BO} = \sqrt{2} \cdot V_{in,rms} \cdot \frac{R_{bo2}}{R_{bo1} + R_{bo2}}$$
  - After the PFC stage has started operation, the input voltage becomes a rectified sinusoid and the voltage applied to pin7 is:
    $$V_{BO} = \frac{2\sqrt{2} \cdot V_{in,rms}}{\pi} \cdot \frac{R_{bo2}}{R_{bo1} + R_{bo2}}$$, i.e., about 64% of the previous value. Therefore, the same line magnitude leads to a $V_{BO}$ voltage which is 36% lower when the PFC is working than when it is off. That is why a large hysteresis (in the range of 50% of the upper threshold) is required.

Other applications may require a different hysteresis amount. That is why the hysteresis is made programmable and dependent on the internal 7 μA current source. More specifically, re−using the components of Figure 22:

- The line upper BO threshold is:
  $$(V_{in,rms})_{boH} = \frac{1}{\sqrt{2}} \cdot \frac{R_{bo1} + R_{bo2}}{R_{bo2}} \left( V_{BO(th)} + \frac{R_{bo1} \cdot R_{bo2} \cdot I_{BO}}{R_{bo1} + R_{bo2}} \right)$$
  where $V_{BO(th)}$ is the BO comparator threshold (1 V typically) and $I_{BO}$, the 7 μA current source.
- The line lower threshold is:
  $$(V_{in,rms})_{boL} = \frac{\pi}{2\sqrt{2}} \cdot \frac{R_{bo1} + R_{bo2}}{R_{bo2}} \cdot V_{BO(th)}$$

Hence the ratio upper over lower threshold is:
$$\frac{(V_{in,rms})_{boH}}{(V_{in,rms})_{boL}} = \frac{2}{} \cdot \left( 1 + \frac{R_{bo1} \cdot R_{bo2} \cdot BO}{(bo1 + bo2) \cdot BO(th)} \right)$$

- If the output of OPAMP remains low for the duration of the second delay, no fault is detected.

In any case, the $L_{BO}$ latch and the two delays are reset at the end of the second delay.

When the “BO_NOK” signal is high, the driver is disabled, the “$V_{control}$” pin is grounded to recover operation with a soft−start when the fault has gone and the “pfcOK” voltage turns low to disable the downstream converter. In addition, the 500 ms and 50 ms timers are reset, the 980 mV clamp is removed ($S_2$ is off) and $I_{BO}$, the 7 μA current source, is enabled to lower the pin7 voltage for hysteresis purpose (as explained above).

A pnp transistor ensures that the BO pin voltage remains below the 1 V threshold until $V_{CC}$ reaches $V_{CC(on)}$. This is to guarantee that the circuit starts operation in the right state, that is, “BONOK” high. When $V_{CC}$ exceeds $V_{CC(on)}$, the pnp transistor turns off and the circuit enables the 7 μA current source. The 7 μA current source remains on until the BO pin voltage exceeds the 1 V BO threshold.

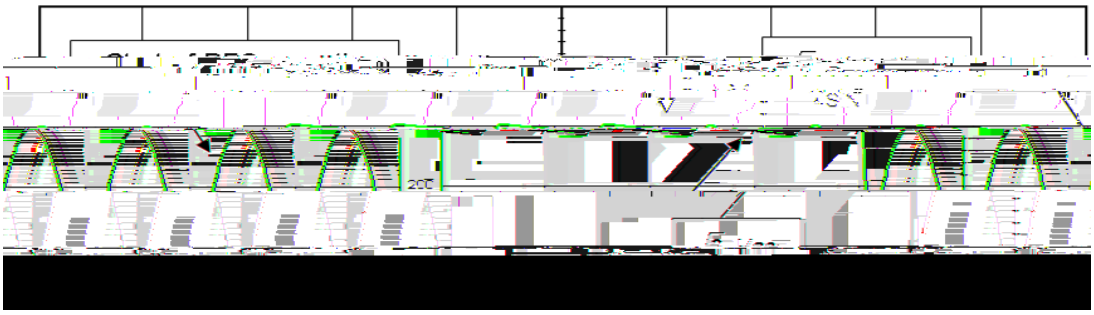


**Figure 23. Typical Input Voltage of a PFC Stage**

### Thermal Shutdown (TSD)

An internal thermal circuitry disables the circuit gate drive and then keeps the power switch off when the junction temperature exceeds 140°C typically. The output stage is then enabled once the temperature drops below about 80°C (60°C hysteresis).

The temperature shutdown keeps active as long as the circuit is not reset, that is, as long as $V_{CC}$ keeps higher than $V_{CC}$RESET. The reset action forces the TSD threshold to be the upper one (140°C). This ensures that any cold start−up will be done with the right TSD level.

### Under−Voltage Lockout Section

The NCP1632 incorporates an Under−Voltage Lockout block to prevent the circuit from operating when the power supply is not high enough to ensure a proper operation. An

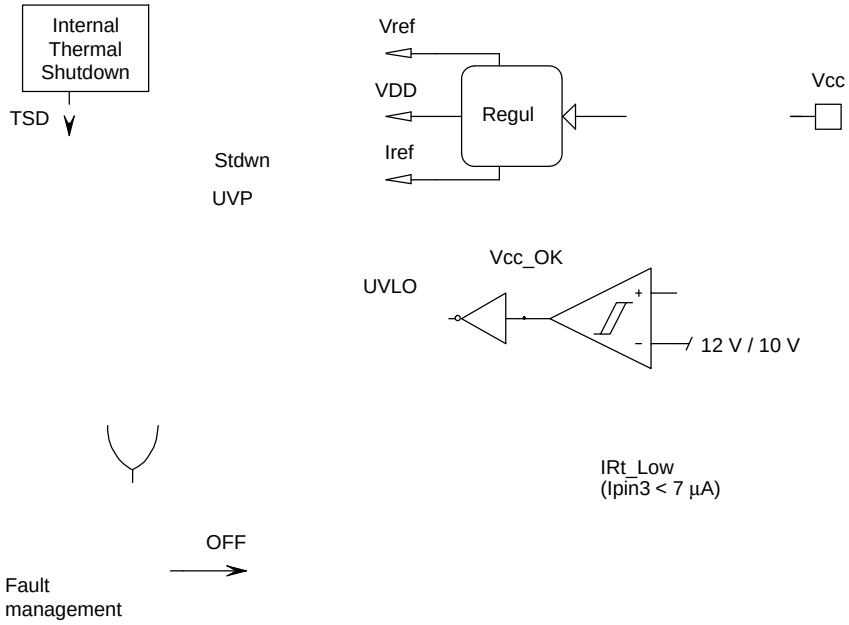



**Figure 24. Fault Management Block**

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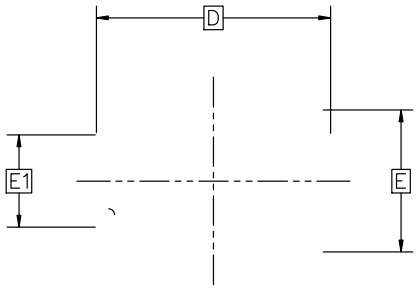
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.1[illegible]

nm TOTAL IN EXCESS OF THE

b DIMENSION AT MAXIMUM MATE




TOP VIEW

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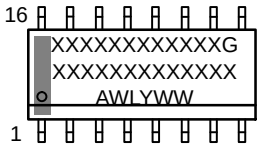
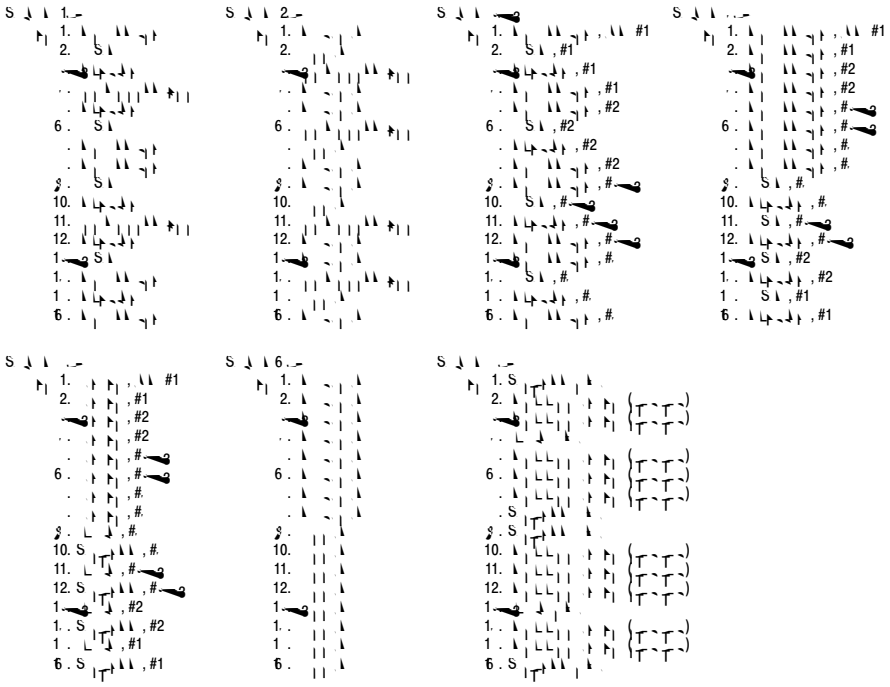
## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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