C 302040

I ' D
' V FE

Description

The NCP302040 integrates a MOSFET driver, high-side MOSFET and low-side MOSFET into a single package.

The driver and MOSFETs have been optimized for high-current DC−DC buck power conversion applications. The NCP302040 integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

Features

- Capable of Average Currents up to 40 A
- Capable of Switching at Frequencies up to 2 MHz
- Capable of Peak Currents up to 75 A
- Compatible with 3.3 V or 5 V PWM Input
- Responds Properly to 3-level PWM Inputs
- Option for Zero Cross Detection with 3-level PWM
- Internal Bootstrap Diode
- Undervoltage Lockout
- Supports Intel®

September, 2017 − Rev. 2
Publication Order Number:
NCP302040/D

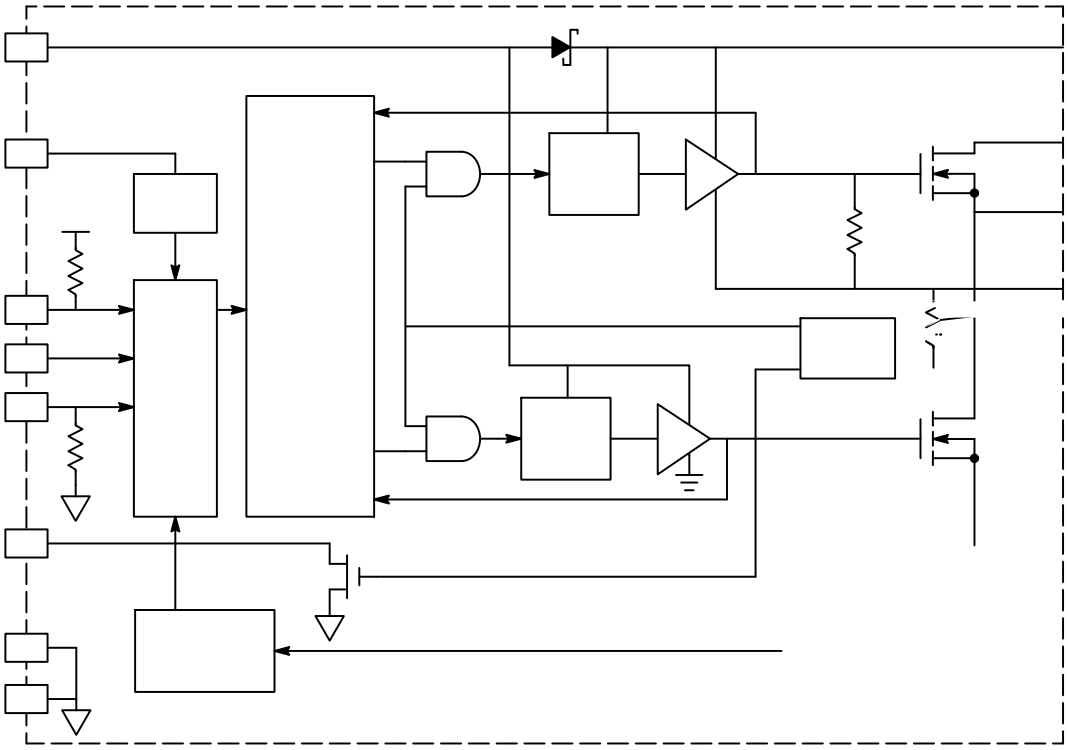


Figure 2. Block Diagram

Table 5. ELECTRICAL CHARACTERISTICS

(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC SUPPLY CURRENT						
Operating		DISB# = 5 V, PWM = 400 kHz	−	1	2	mA
No switching		DISB# = 5 V, PWM = 0 V	−	−	2	mA
Disabled		DISB# = 0 V, SMOD# = VCC	−	0.4	1	μA
		DISB# = 0 V, SMOD# = GND	−	6	13	μA
UVLO Start Threshold	V_{UVLO}	VCC Rising	2.9	−	3.3	V
UVLO Hysteresis			150	−	−	mV
VCCD SUPPLY CURRENT						
Enabled, No Switching		DISB# = 5 V, PWM = 0 V, V_{PHASED} = 0 V	−	175	300	μA
Disabled		DISB# = 0 V	−	0.4	1	μA
Operating		DISB# = 5 V, PWM = 400 kHz	−	−	20	mA
DISB# INPUT						
Input Resistance		To Ground	−	467	−	kΩ
Upper Threshold	V_{UPPER}		−	−	2.0	V
Lower Threshold	V_{LOWER}		0.8	−	−	V
Hysteresis		V_{UPPER} – V_{LOWER}	200	−	−	mV
Enable Delay Time		Time from DISB# transitioning HI to when VSW responds to PWM.	−	−	40	μ

Table 5. ELECTRICAL CHARACTERISTICS (continued)
(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PWM INPUT						
Input Resistance	R_{PWM_BIAS}	SMOD# = $V_{SMOD\#\_MID}$	−	68	−	kΩ
PWM Input Bias Voltage	V_{PWM_BIAS}	SMOD# = $V_{SMOD\#\_MID}$	−	1.7	−	V
Non-overlap Delay, Leading Edge	T_{NOL_L}	GL Falling = 1 V to GH−VSW Rising = 1 V	−	13	−	ns
Non-overlap Delay, Trailing Edge	T_{NOL_T}	GH−VSW Falling = 1 V to GL Rising = 1 V	−	12	−	ns
PWM Propagation Delay, Rising	T_{PWM,PD_R}	PWM = High to GL = 90%	−	13	35	ns
PWM Propagation Delay, Falling	T_{PWM,PD_F}	PWM = Low to VSW = 90%	−	47	52	ns
Exiting PWM Mid-state Propagation Delay, Mid-to-Low	$T_{PWM\_EXIT\_L}$					

Table 6. LOGIC TABLE

INPUT TRUTH TABLE				
DISB#	**PWM**	**SMOD#** (Note 4)	**GH (Not a Pin)**	**GL**
L	X	X	L	L
H	H	X	H	L

TYPICAL PERFORMANCE CHARACTERISTICS

(Test Conditions: V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V, V_{OUT} = 1 V, L_{OUT} = 250 nH, T_A = 25°C and natural convection cooling, unless otherwise noted.)

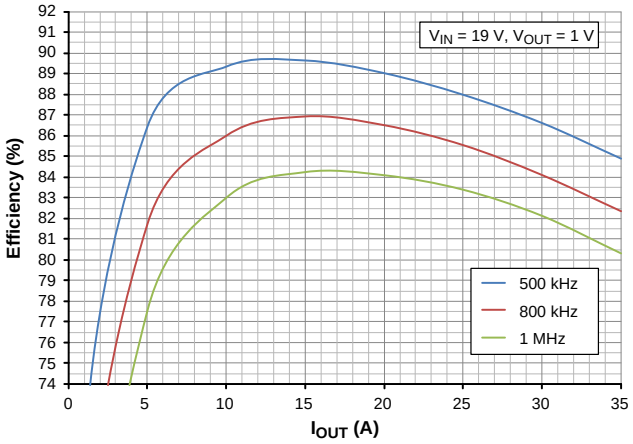


Figure 3. Efficiency − 19 V Input, 1.0 V Output

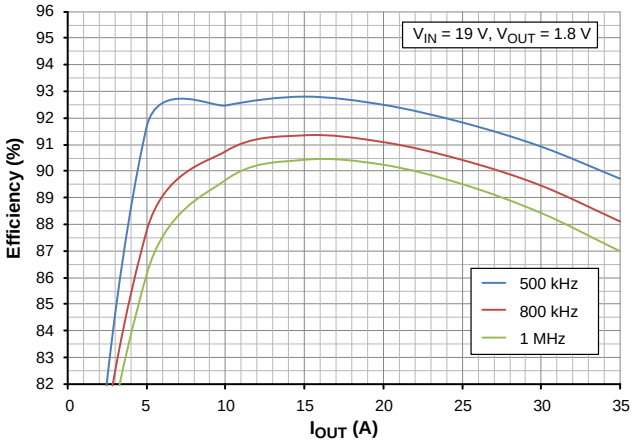


Figure 4. Efficiency − 19 V Input, 1.8 V Output

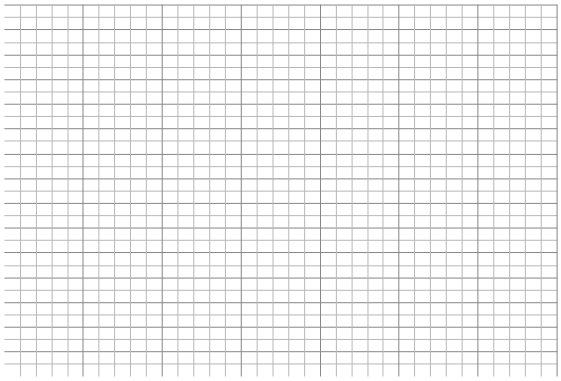


Figure 5. Efficiency − 12 V Input, 1.0 V Output

Figure 6. Efficiency − 12 V Input, 1.8 V Output

Figure 7. Power Losses vs. Output Current, 12 V_{IN}

Figure 8. Power Losses vs. Output Current, 19 V_{IN}

TYPICAL PERFORMANCE CHARACTERISTICS

(Test Conditions: V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V, V_{OUT} = 1 V, L_{OUT} = 250 nH, T_A = 25°C and natural convection cooling, unless otherwise noted.)

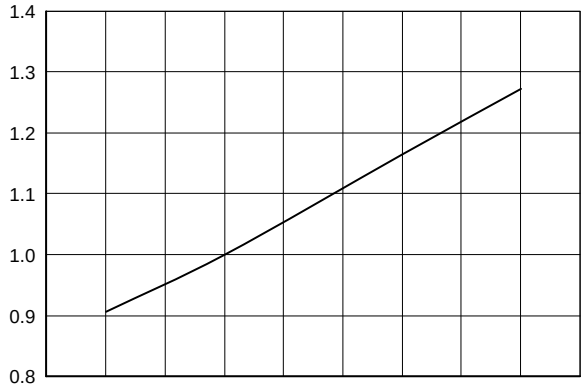


Figure 9. Power Loss vs. Switching Frequency

Figure 10. Power Loss vs. Input Voltage

Figure 11. Power Loss vs. Driver Supply Voltage

Figure 12. Power Loss vs. Output Voltage

Figure 13. Driver Supply Current vs. Switching Frequency

Figure 14. Driver Supply Current vs. Driver Supply Voltage

Disable Input (DISB#)

For Use with Controllers with 3-state PWM and Zero

RECOMMENDED PCB LAYOUT

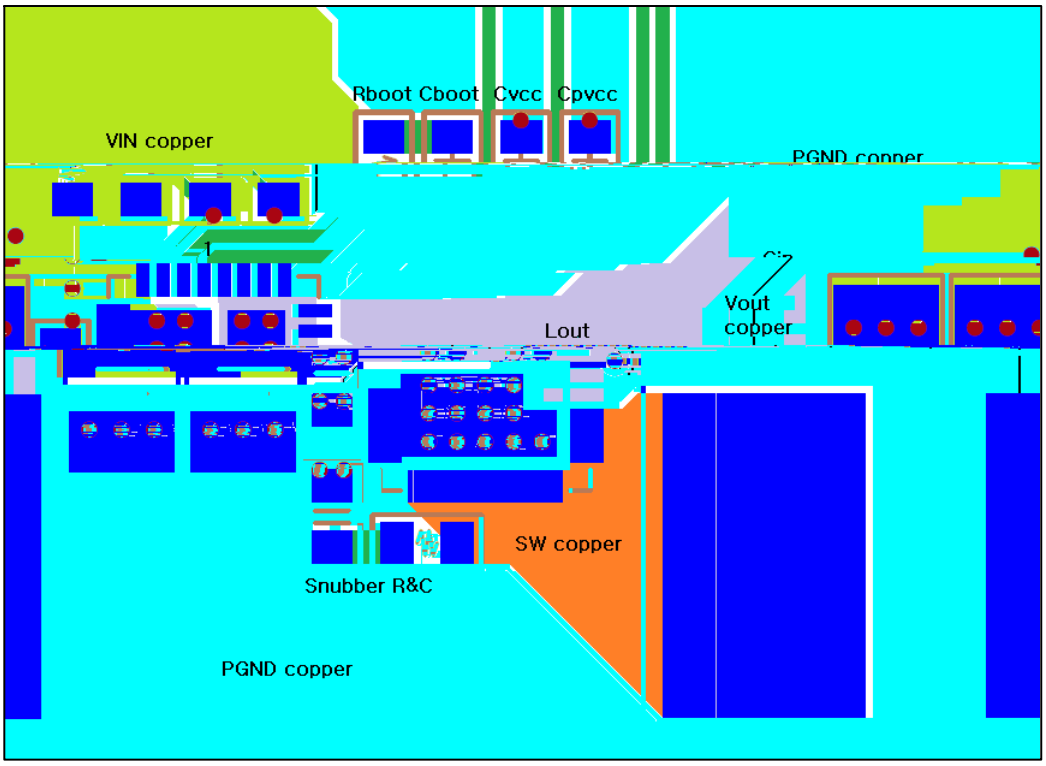


Figure 18. Top Copper Layer (Viewed from Top)

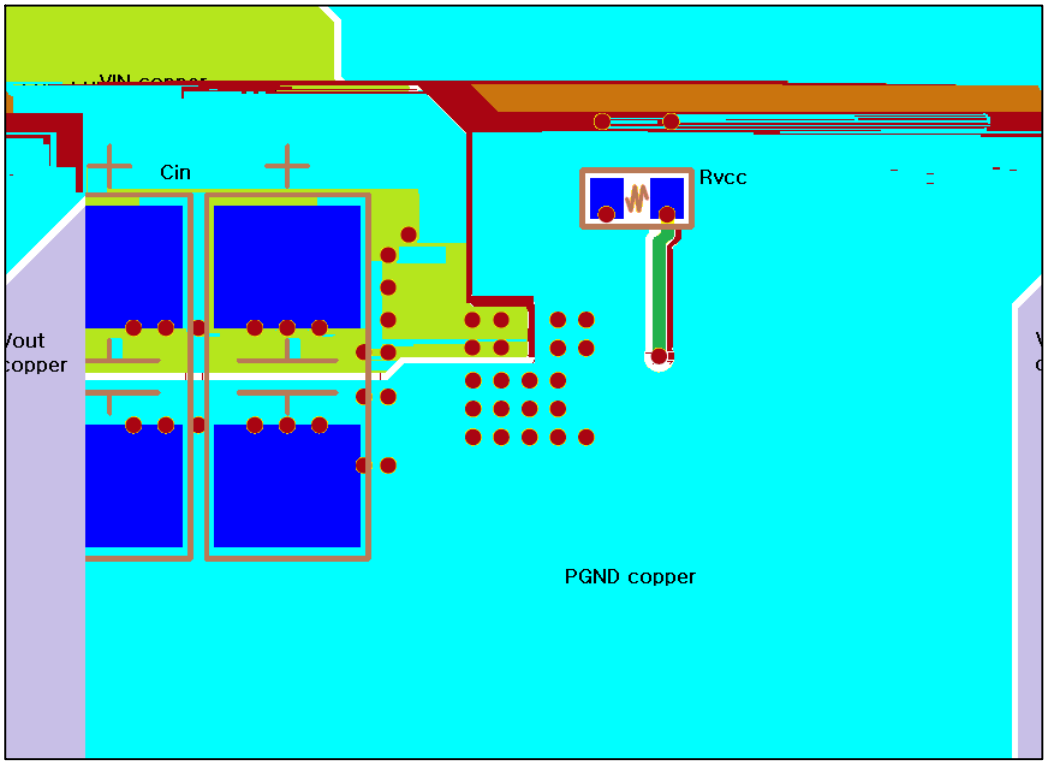


Figure 19. Bottom Copper Layer (Viewed from Top)

RECOMMENDED PCB FOOTPRINT (OPTION 1)

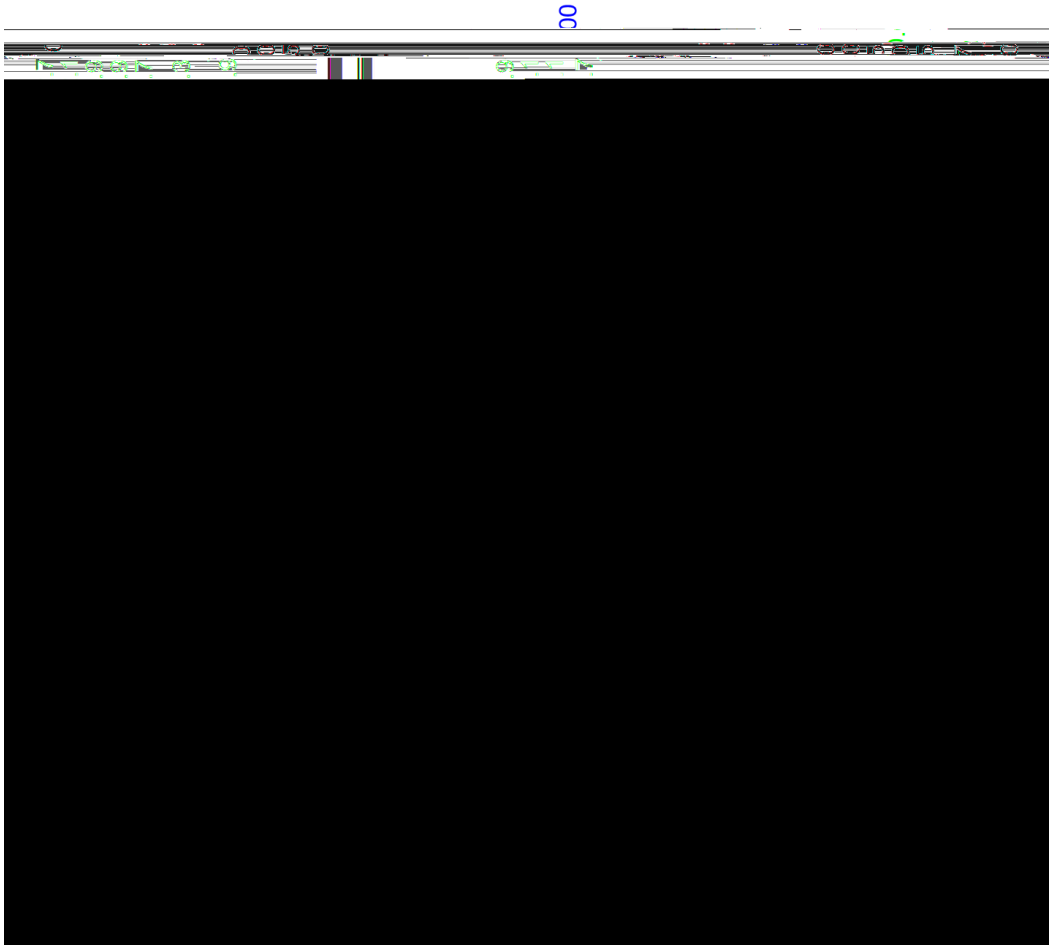
LAND PATTERN RECOMMENDATION

RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Figure 20. Recommended PCB Footprint (Option 1)

RECOMMENDED PCB FOOTPRINT (OPTION 2)



LAND PATTERN RECOMMENDATION

RECOMMENDED MOUNTING FOOTPRINT

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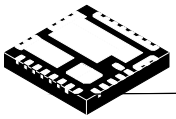
Figure 21. Recommended PCB Footprint (Option 2)



CASE 483BR
ISSUE D

DATE 13 FEB 2023

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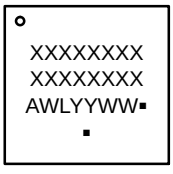
RECOMMENDED MOUNTING FOOTPRINT*
(2X SCALE)

* For additional informatior



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.