Integrated Synchronous Buck Converter

3 A

NCP3133A

NCP3133A is a fully integrated synchronous buck converter for 3.3 V and 5 V step−down applications. It can provide up to 3 A load

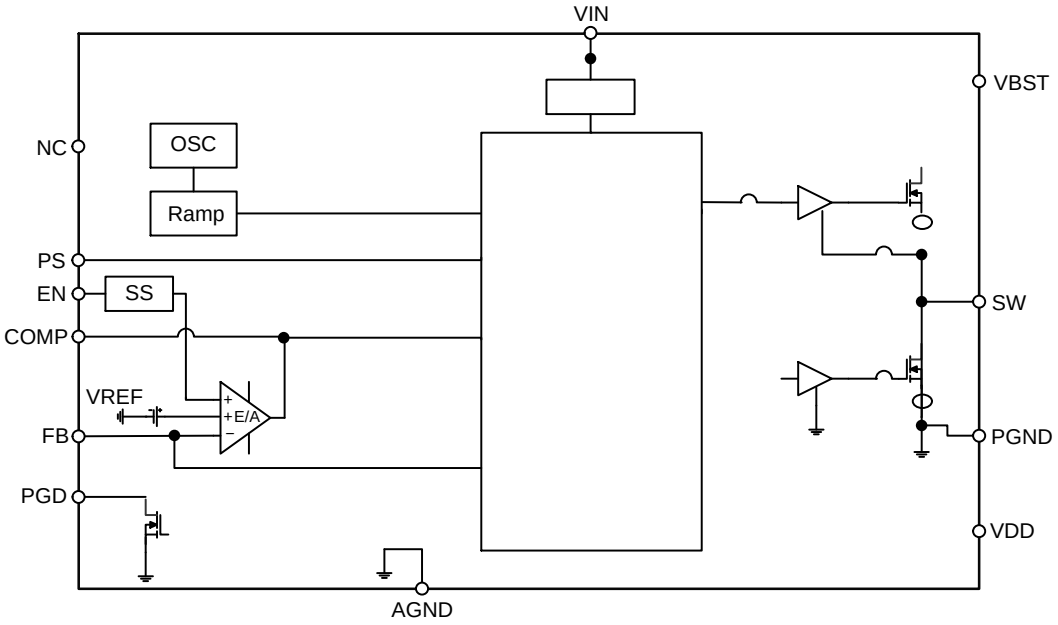

Figure 1. Block Diagram

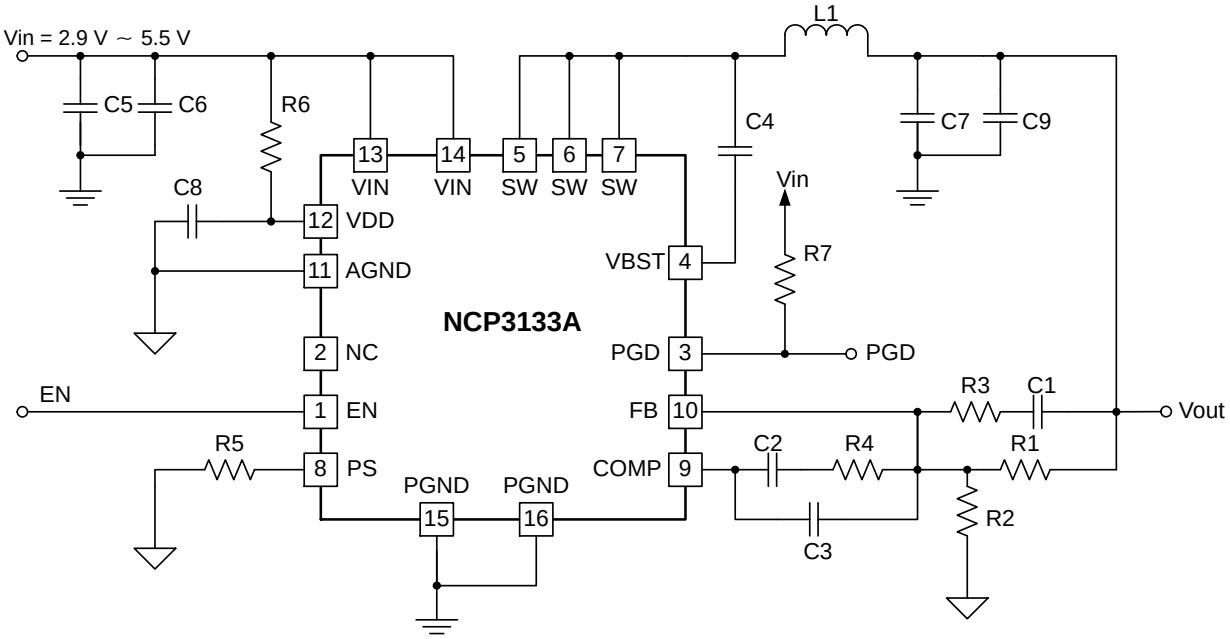

Figure 2. NCP3133A Single Voltage Rail for V_{IN} and V_{DD}

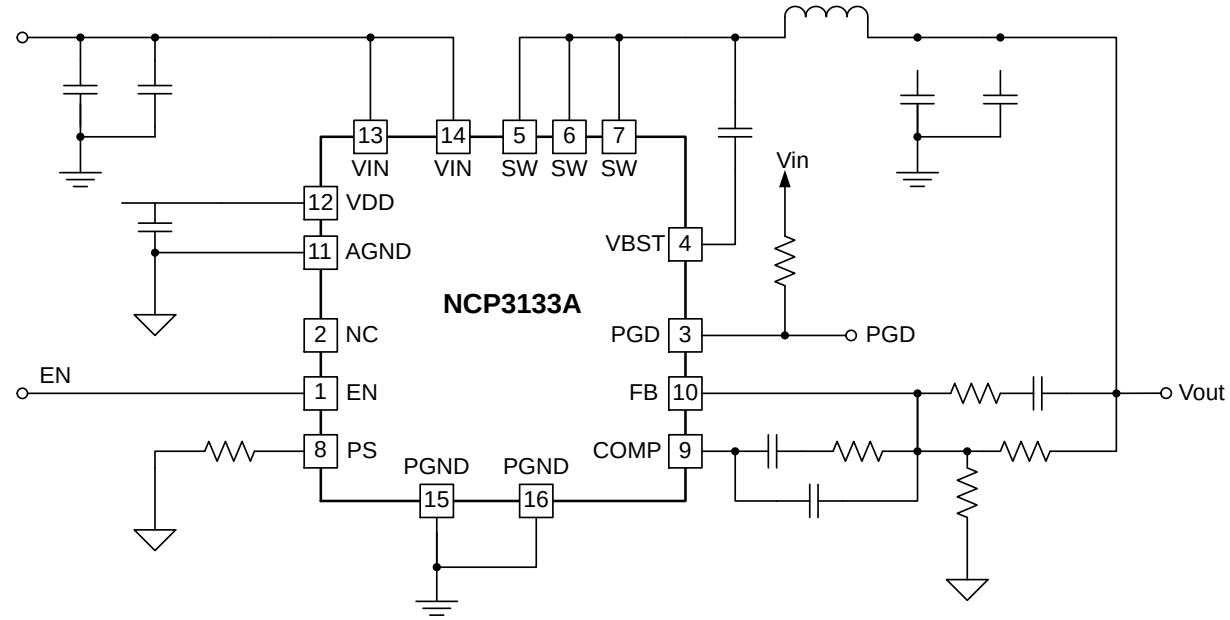

Figure 3. NCP3133A Dual Voltage Rail for V_{IN} and V_{DD}

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol		Value		Units
			Min	Max	
Input Voltage Range	VIN, VDD		−0.3	6.5	V
	VBST		−0.3	17	
	VBST (with respect to SW)		−0.3	7	
	FB, PS, EN		−0.3	VDD+0.3V	
Output Voltage Range	SW	DC	−1	7	V
		Pulse < 20 ns, E = 5 μJ	−3	10	
	PGD		−0.3	7	
	COMP		−0.3	3.7	
	PGND		−0.3	0.3	
Operation ambient temperature	T_A		−40	85	C
Storage temperature	T_S		−55	150	
Junction temperature	T_J		−40	150	
Electrostatic Discharge					

Table 5. ELECTRICAL CHARACTERISTICS
(V_{DD} = V_{IN} = 3.3 V and V_{DD} = V_{IN} = 5.0 V, over recommended free air temperature range, PGND = GND unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ

Table 5. ELECTRICAL CHARACTERISTICS
(V_{DD} = V_{IN} = 3.3 V and V_{DD} = V_{IN} = 5.0 V, over recommended free air temperature range, PGND = GND unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
LOGIC PINS: I/O VOLTAGE AND CURRENT						
EN high threshold voltage			1.1	1.18	1.30	V
EN hysteresis				0.18	0.24	V
EN input pull up resistor				1.35		MΩ
PS mode threshold voltage		Level 1 to Level 2		2.2		V
PS source		10 μA pull−up current when enabled	8	10	12	μA
INTERNAL BST DIODE						
Reverse−bias leakage current		V_{BST} = 6.6 V, V_{in} = 3.3 V, T_A = 25 C			1	μA
SOFT STOP						
Output discharge on−resistance		EN = 0, V_{IN} = 3.3 V, V_{out} = 0.5 V		20		Ω
TIMERS: SOFT START						
Soft start ramp−up time	T_{SS}	Rising from Vss = 0 V to Vss = 0.6 V		0.4		ms
Delay after EN asserting		EN = 'HI'		0.2		ms
Switching frequency control		Forced CCM mode	0.99	1.1	1.21	MHz
PWM						
Minimum OFF time		FCCM mode or Automatic CCM/DCM mode		100	140	ns
PWM ramp amplitude (Note1)		2.9 V < V_{IN} < 0.6 V		VIN/4		V
Maximum duty cycle, FCCM mode or Automatic CCM/DCM mode		Fs_W = 1.1 MHz, 0 C < T_A < 85 C	84%	89%		
THERMAL SHUTDOWN						
Thermal shutdown threshold (Note 1)			130	140	150	

TYPICAL CHARACTERISTICS

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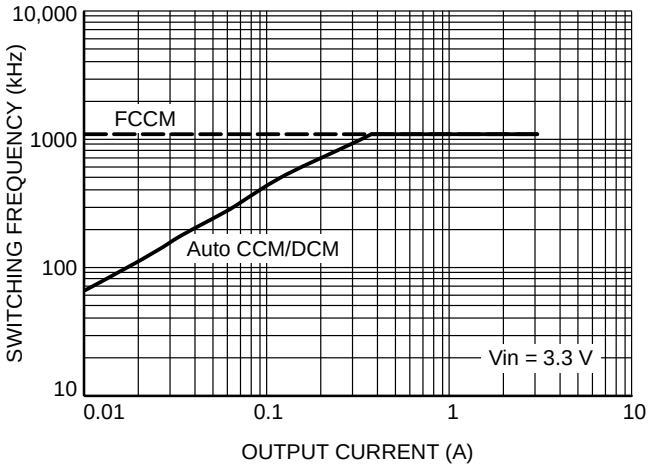


Figure 10. Switching Frequency vs. Output Current at Vin = 3.3 V

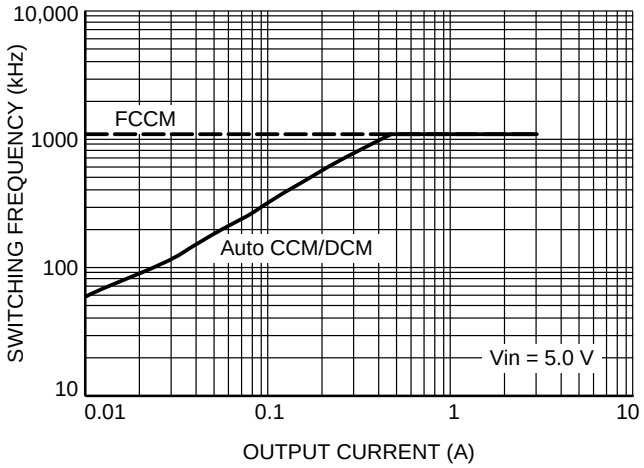


Figure 11. Switching Frequency vs. Output Current at Vin = 5.0 V

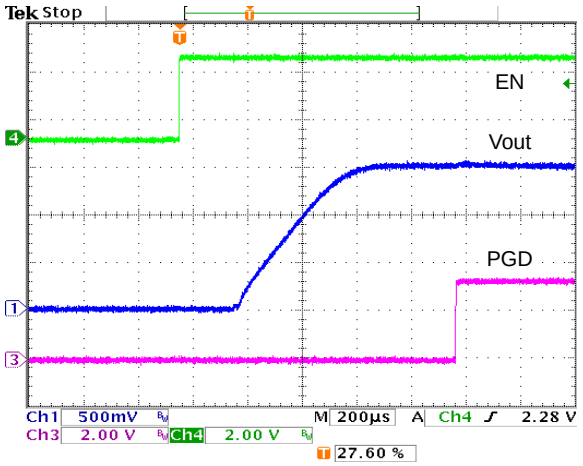


Figure 12. Soft Start−up at Auto CCM/DCM Mode Vin = 3.3 V, No Load

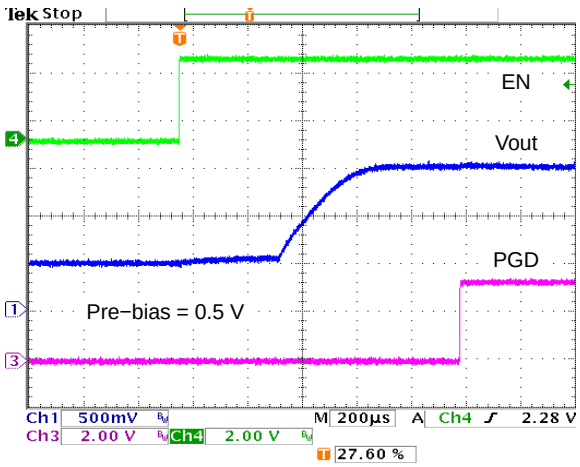


Figure 13. Pre−bias Start−up at Auto CCM/DCM Mode Vin = 3.3 V, No Load

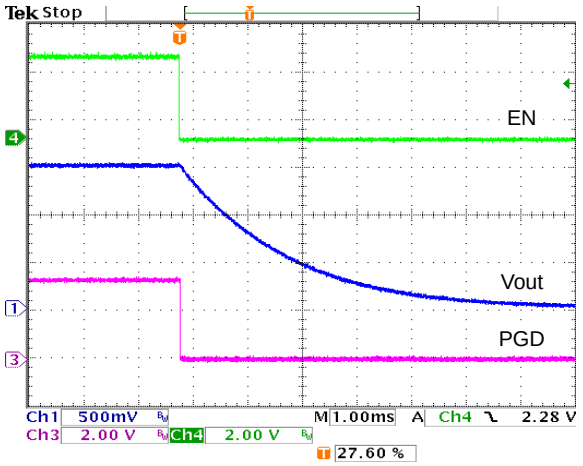


Figure 14. Soft Stop at Auto CCM/DCM Mode Vin = 3.3 V, No Load

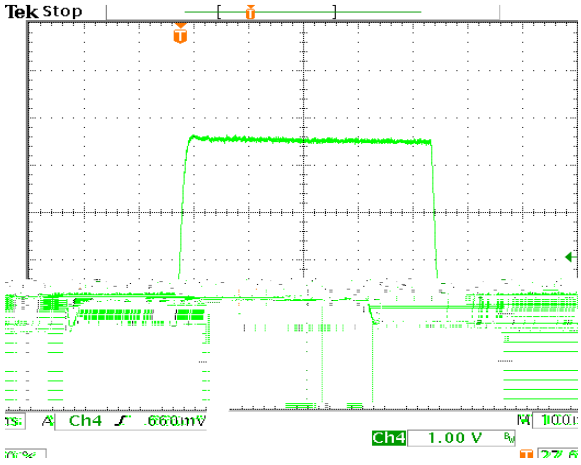


Figure 15. Switching Node Waveform at Auto CCM/DCM Mode Vin = 3.3 V, Full Load

TYPICAL CHARACTERISTICS

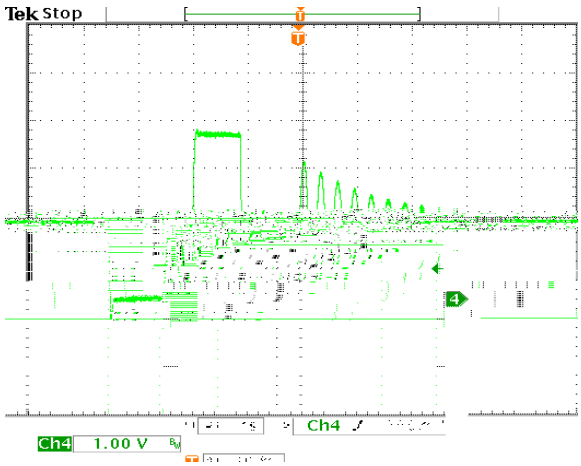


Figure 16. Switching Node Waveform at Auto CCM/DCM Mode Vin = 3.3 V, No Load

PROTECTIONS

Under Voltage Lockout (UVLO)

There is under-voltage lock out protection (UVLO) for both VIN and VDD in NCP3133A, which has a typical trip threshold voltage 2.8 V and trip hysteresis 75 mV for VDD and 130 mV for VIN. If UVLO is triggered, the device resets and waits for the voltage to rise up over the threshold voltage and restart the part. Please note this protection function DOES NOT trigger the fault counter to latch off the part.

Over Voltage Protection (OVP)

When feedback voltage is above 17% (typical) of nominal voltage for over 1.7 μs blanking time, an OV fault is set. In this case, the converter de−asserts the PGD signal and performs the over−voltage protection function. The top gate drive is turned off and the bottom gate drive is turned on to discharge the output. The bottom gate drive will be turned off until VFB drops below the UVP threshold. The device enters a high−impedance state. This protection is latched.

Under Voltage Protection (UVP)

Output under−voltage protection works in conjunction with the current protection described in the Over−current Protection sections. An UVP circuit monitors the feedback voltage to detect under−voltage event. The under−voltage limit is 17% (typical) below of nominal voltage at FB pin. If the feedback voltage is below this threshold over 11 μs, an UV fault is set and both the high−side and the low−side FETs turn off. This protection is latched.

Power Good Monitor (PGD)

NCP3133A provides window comparator to monitor the output voltage at FB pin. When the output voltage is within 17% of regulation voltage, the power good pin outputs a high signal. Otherwise, PGD stays low. The PGD pin is open drain 5 mA pull down output. During startup, PGD stays low until the feedback voltage is within the specified range for about 0.4 ms. If feedback voltage falls outside the tolerance band, the PG pin goes low after 10 μs delay.

The PGD pin de−asserts as soon as the EN pin is pulled low or an under−voltage event on VDD is detected.

Over Current Protection (OCP)

NCP3133A provides both high−side and low−side MOSFET current limiting. When the current through the high−side FET exceeds 4.8 A, the high−side FET turns off and the low−side FET turns on until next PWM cycle. An over−current counter is triggered and starts to increment each occurrence of an over−current event. Both the high−side and the low−side FETs turn off when the OC counter reaches four. The OC counter resets if the detected current is less than 4.8 A after an OC event.

Another set of over−current circuitry monitors the current flowing through the low−side FET. If the current through the low−side FET exceeds 5.1 A, the over−current protection is enabled and immediately turns off both the high−side and the low−side FETs. The device is fully protected against over−current during both on−time and off−time. This protection is latched.

Pre−Bias Startup

In some applications the controller will be required to start switching when its output capacitors are charged anywhere from slightly above 0 V to just below the regulation voltage. This situation occurs for a number of reasons: the converter's output capacitors may have residual charge on them or the converter's output may be held up by a low current standby power supply. NCP3133A supports pre−bias start up by holding low−side FETs off until soft start ramp reaches the FB pin voltage.

Thermal Shutdown

The NCP3133A protects itself from over heating with an internal thermal monitoring circuit. When the die temperature goes beyond a threshold value 135 C, both the high−side and the low−side FETs turn off until the temperature falls 40 C below of the threshold value. Then the converter restarts.

Application Note

For higher output voltage application cases (Vout = --.00 0 0-0 0 0-.0

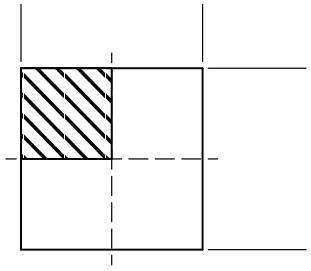
ORDERING INFORMATION

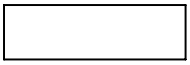
Device	Marking	Package	Shipping†
NCP3133AMNTXG	3133A		

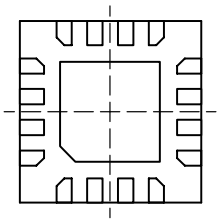
QFN16 3x3, 0.5P
CASE 485DA
ISSUE A

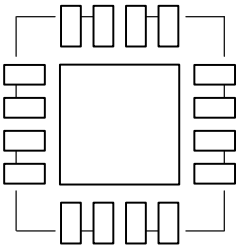
SCALE 2:1

DATE 22 SEP 2015









NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.