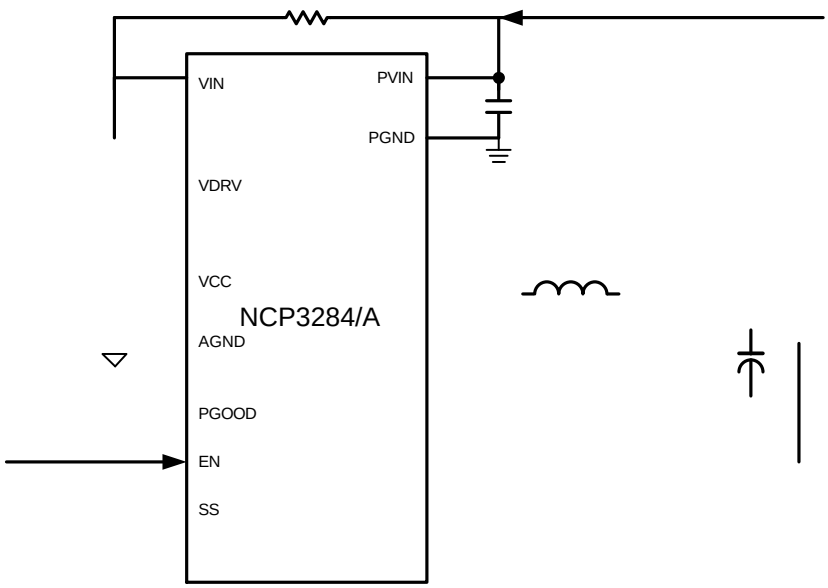

Figure 1. Typical Application Circuit with Single Input Power Supply (LDO Enabled)

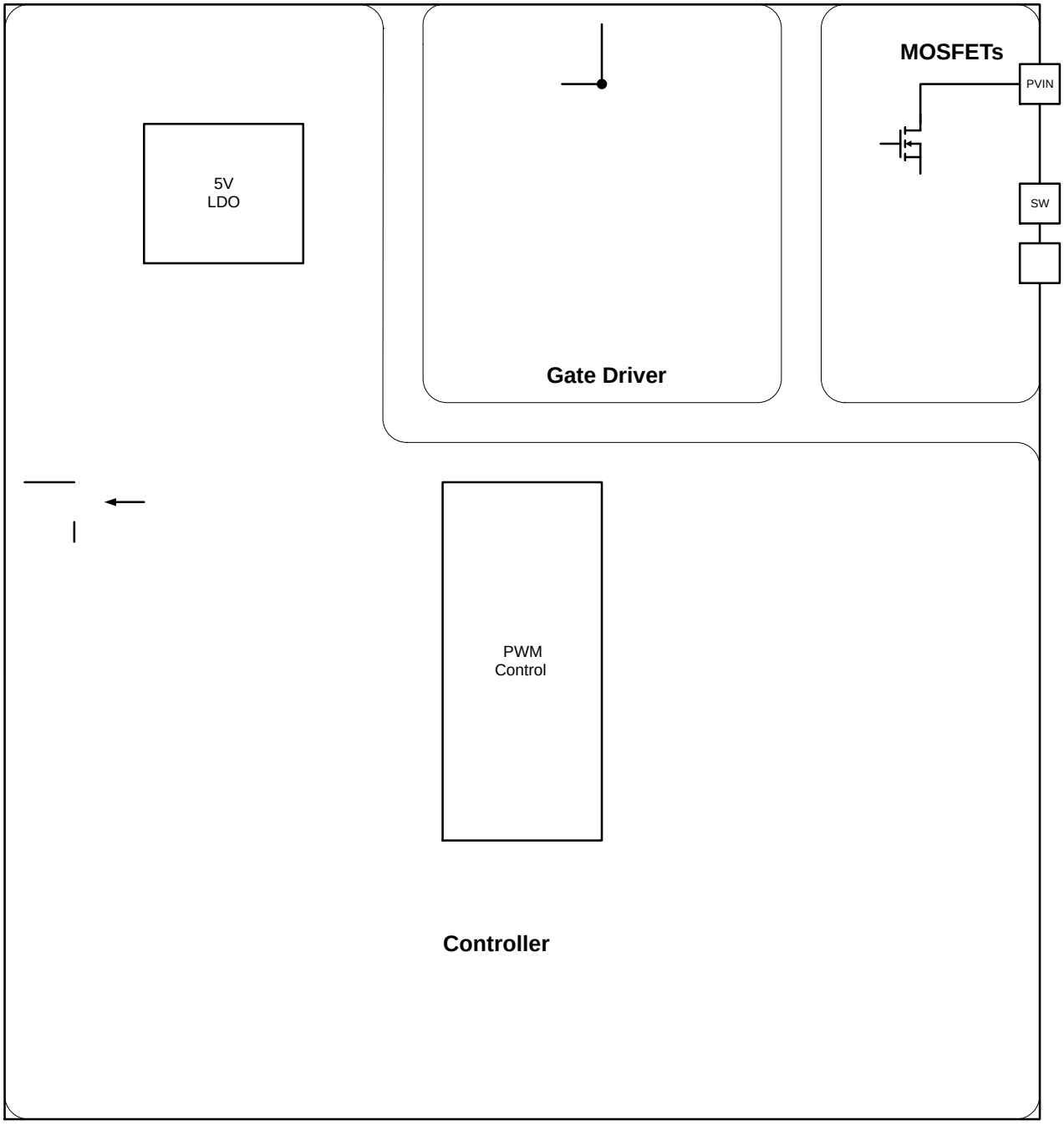

Figure 3. Functional Block Diagram

PIN DESCRIPTION

Pin	Name	Type	Description
1	ILIM	Analog Output	Current Limit. A resistor between this pin and AGND to program current limit.
2	PGOOD	Logic Output	Power Good. Open drain output. Provides a logic high valid power good output signal, indicating the regulator's output is in regulation window.
3	VIN	Power Input	Power Supply Input of LDO. Power supply input pin of internal 5 V LDO. A 1.0 μF or more ceramic capacitor must bypass this input to power ground. The capacitor should be placed as close as possible to this pin. A direct short from this pin to VDRV (pin 5) disables the internal LDO for applications with an external 5 V supply as power of VDRV and VCC.
4	VCC	Analog Power	Supply Voltage Input of Controller. A 2.2 μF or larger ceramic capacitor bypasses this input to GND. This capacitor should be placed as close as possible to this pin.
5	VDRV	Analog Power	Output of LDO and Supply Voltage Input of Gate Drivers. Output of integrated 5.0 V LDO and power supply input of gate drivers. A 4.7 μF/25 V or larger ceramic capacitor bypasses this pin to PGND. The capacitor should be placed as close as possible to this pin.
6	GL	Analog Output	Gate of Low Side MOSFET. Internally connected to the gate of the low side power MOSFET. No external connection required.
7~10,19	PGND	Power Ground	Power Ground. These pins are the power supply ground pins of the device, which are connected to source of internal low side power MOSFET. Must be connected to the system ground.
11~18	SW	Power Bidirectional	Switch Node. Pins to be connected to an external inductor. These pins are interconnection between internal high side MOSFET and low side MOSFET.
20~24	PVIN	Power Input	Power Supply Input. These pins are the power supply input pins of the device, which are connected to drain of internal high side power MOSFET. A 22 μF or more ceramic capacitor must bypass this input to PGND. The capacitors should be placed as close as possible to these pins.
25	PHASE	Power Return	Phase Node. Provides a return path for integrated high side gate driver. It is internally connected to source of high side MOSFET.
26	BOOT	Power Bidirectional	Bootstrap. Provides bootstrap voltage for high side gate driver. A 0.22 μF/25 V ceramic capacitor is required from this pin to PHASE (pin 25).
27	EN	Logic Input	Enable. Logic high enables controller while logic low disables controller. Input supply UVLO can be programmed at this pin.
28	VOS	Analog Input	Voltage Sense. Remote output voltage sense. Connect to VOUT through 1 kΩ series resistor.
29	SS	Analog Input	Soft Start. A resistor between this pin and GND to program the soft start slew rate and options.
30	FB	Analog Input	Feedback. Inverting input to error amplifier.
31	VSNS	Analog Input	Voltage Sense Negative Input. Connect this pin to remote voltage negative sense point.
32	AGND	Analog Ground	Analog Ground. Ground of controller. Must be connected to the system ground.
33~34	NC		No Connection.
35	HICCUP#	Analog Input	Latch Off / Hiccup#. Float this pin to enable latch off mode protections (OCP/ UVP/OVP); Ground this pin to ground to enable hiccup mode protections.
36	MODE/FSET	Analog Input	Mode and Frequency Set. A resistor between this pin and AGND to program operation mode and nominal switching frequency.

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		MIN	MAX	
Power Supply Voltage to PGND	V_{PVIN}, V_{VIN}		25	V
PHASE/SW to PGND	V_{PHASE}, V_{SW}	0.6 5 (<50 ns)	25 28 (<10 ns)	V
PVIN to SW/PHASE	V_{PVIN_SW}	0.3 5 (<10 ns)	25 33 (<10 ns)	V
Driver Supply Voltage to PGND	V_{VDRV}	0.3	5.5	V
Analog Supply Voltage to AGND	V_{VCC}	0.3	6.5	V
BOOT to PGND	BOOT_PGND	0.3	30 33 (<10 ns)	V
BOOT to PHASE/SW	BOOT_PHASE/SW	0.3	6.5	V
GL to PGND	GL	0.3 2 (<200 ns)	VDRV+0.3	V
VSNS to AGND	VSNS	0.2	0.2	V
PGND to AGND	PGND	0.3	0.3	V
Other Pins		0.3	VCC+0.3	V
ESD, Human Body Model per ANSI/ESDA/JEDEC JS 001 (Note 1)	ESD_{HBM}	2.0		kV
ESD, Charge Device Model per ANSI/ESDA/JEDEC JS 002 (Note 1)	ESD_{CDM}	1.5		kV
Maximum Latch up Current Rating. 150°C, per JEDEC JESD78 (Note 2)	I_{LU}			

ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, typical values are referenced to $T_A = T_J$ = 25°C, Min and Max values are referenced to $T_A = T_J$ = 40°C to 125°C. unless other noted.)

Characteristics	Test Conditions		Symbol	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE MONITOR							
VCC Under Voltage (UVLO) Threshold	VCC falling		V_{DDUV}	4.0			V
VCC OK Threshold	VCC rising		V_{DDOK}			4.5	V
VCC UVLO Hysteresis			V_{DDHYS}		200		mV
SUPPLY CURRENT							
PVIN Shutdown Current	EN low		I_{SDPVIN}		4.8	20	μA
V_{IN} Quiescent Supply Current (VCC Current Included)	EN high, no switching	LDO enabled, VIN = 18 V, VCC = VDRV					

ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, typical values are referenced to $T_A = T_J$ = 25°C, Min and Max values are referenced to $T_A = T_J$ = 40°C to 125°C. unless other noted.)

Characteristics	Test Conditions		Symbol	MIN	TYP	MAX	UNITS
SOFT START							
Soft Start Time	1% Resistor from SS Pin to AGND	0 or 4.53k	T_{SS}		1.0	1.1	ms
		1.5k or 5.76k			2.0		

DETAILED DESCRIPTION

General

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Operation Modes

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Table 1. MODE AND SWITCHING FREQUENCY CONFIGURATION

Resistance @ MODE/FSET Pin (Ω, ±1%)	Frequency (kHz)	Operation Mode
0	600	FCCM
2.49k	1000	FCCM
4.99k	500	Auto CCM/DCM
7.5k	500	FCCM
10.5k	600	Auto CCM/DCM
12.1k	800	Auto CCM/DCM
14.0k	1000	Auto CCM/DCM
Float	800	FCCM

Current Mode RPM Operation

Enable and Input UVLO

$$V_{EN\_H} = V_{EN\_TH} + V_{EN\_HYS} \quad \text{(eq. 1)}$$

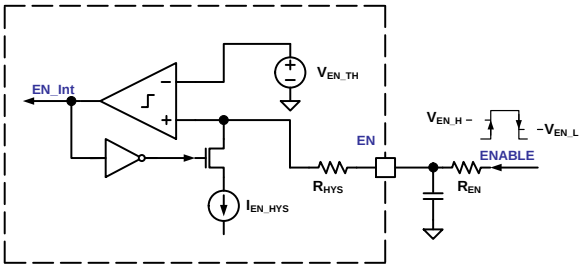

Figure 5. Enable and Hysteresis Programming

$$V_{EN\_L} = V_{EN\_TH} \quad \text{(eq. 2)}$$

$$V_{EN\_HYS} = I_{EN\_HYS} \times (R_{HYS} + R_{EN}) \quad \text{(eq. 3)}$$

$$V_{IN\_L} = \left(\frac{R_{EN1}}{R_{EN2}} + 1\right) \times V_{EN\_TH} \quad \text{(eq. 4)}$$

$$V_{IN\_H} = V_{IN\_L} + V_{IN\_HYS} \quad \text{(eq. 5)}$$

$$V_{IN\_HYS} = I_{EN\_HYS} \times \left(R_{HYS}\left(1 + \frac{R_{EN1}}{R_{EN2}}\right) + R_{EN1}\right) \quad \text{(eq. 6)}$$

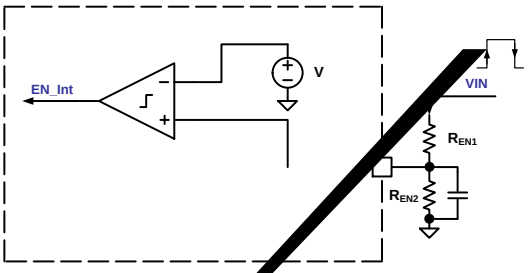

Figure 6. Enable and Input Supply UVLO Circuit

Thermal Shutdown (TSD)

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Power Good (PGOOD)

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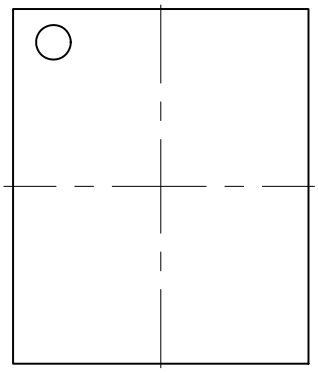
LAYOV27/UIDELINES



TOP VIEW