NC 347

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The NCP347 is able to disconnect the systems from its output pin in case wrong input operating conditions are detected. The system is positive overvoltage protected up to +28 V.

Due to this device using internal NMOS, no external device is necessary, reducing the system cost and the PCB area of the application board.

The NCP347 is able to instantaneously disconnect the output from the input, due to integrated Low R_{ON} Power NMOS (65 m Ω), if the input voltage exceeds the overvoltage threshold (OVLO) or undervoltage threshold (UVLO).

At powerup (\overline{EN} pin = low level), the V_{out} turns on 50 ms after the V_{in} exceeds the undervoltage threshold.

The NCP347 provides a negative going flag (FLAG) output, which alerts the system that a fault has occurred.

In addition, the device has ESD-protected input (15 kV Air) when by passed with a 1.0 μF or larger capacitor.

Features

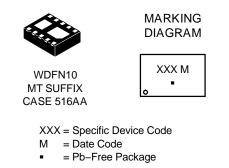
- Overvoltage Protection up to 28 V
- On–Chip Low $R_{DS(on)}$ NMOS Transistor: 65 m Ω
- Internal Charge Pump
- Overvoltage Lockout (OVLO)
- Undervoltage Lockout (UVLO)
- Internal 50 ms Startup Delay
- Alert FLAG Output
- Shutdown EN Input
- Compliance to IEC61000–4–2 (Level 4) 8.0 kV (Contact) 15 kV (Air)
- ESD Ratings: Machine Model = B Human Body Model = 3
- 10 Lead WDFN 2.5x2 mm Package
- This is a Pb-Free Device

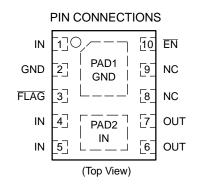
Applications

- Cell Phones
- Camera Phones
- Digital Still Cameras
- Personal Digital Applications
- MP3 Players



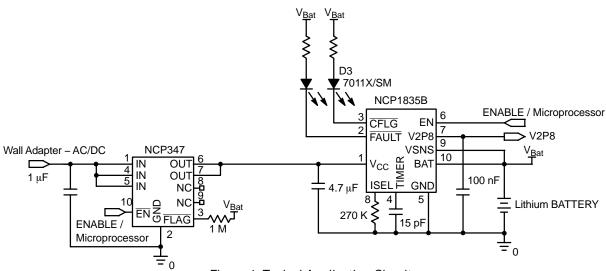
http://onsemi.com





ORDERING INFORMATION

${\ensuremath{{ \odot} }}$ Semiconductor Components Industries, LLC, 2010 May, 2010 Rev. 4





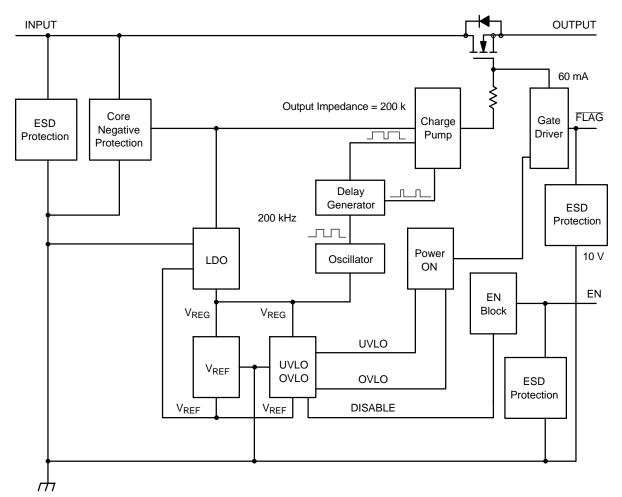


Figure 2. Functional Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Function	Description	
1	IN	POWER	Input Voltage Pin.	
4			This pin is connected to the power supply.	
5			The device system core is supplied by this input.	
			A 1 μF low ESR ceramic capacitor, or larger, must be connected between this pin and GND. The three IN pins must be hardwired to common supply.	
2	GND	POWER	Ground	
3	FLAG	OUTPUT	Fault Indication Pin.	
			This pin allows an external system to detect a fault on IN pin.	
			The FLAG pin goes low when input voltage exceeds OVLO threshold or drop below UVLO threshold.	
			Since the $\overline{\text{FLAG}}$ pin is open drain functionality, an external pull up resistor to V _{CC} must be added.	
6	OUT	OUTPUT	Output Voltage Pin.	
7			This pin follows IN pin when "no fault" is detected.	
			The output is disconnected from the V_{in} power supply when the input voltage is under the UVLO threshold or above OVLO threshold.	
			The two OUT pins must be hardwired to common supply.	
8	NC	OPEN	No Connect	
9	NC	OPEN	No Connect	
10	EN	INPUT	Enable Pin.	
			The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input.	
			To allow normal functionality, the EN pin shall be connected to GND to a pull down or to a I/O pin.	
			This pin does not have an impact on the fault detection.	
PAD1			PAD1, under the device. See PCB recommendations page 10.	
			Can be shorted to GND.	
PAD2			The PAD2 is electrically connected to the internal NMOS drain and connected to Pins 4 and 5. See PCB recommendations page 10.	

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage (IN to GND)	Vmin _{in}	-0.3	V
Minimum Voltage (All others to GND)	Vmin	-0.3	V
Maximum Voltage (IN to GND)	Vmax _{in}	30	V

Maximum Voltage (All others to GND)

ELECTRICAL CHARACTERISTICS (Min/Max limits values ($-40^{\circ}C < T_A < +85^{\circ}C$) and V_{in} = +5.0 V. Typical values are T_A = +25°C,

TIMING DIAGRAMS

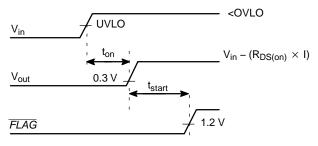


Figure 3. Startup

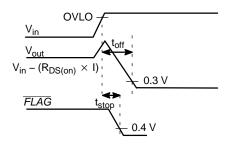
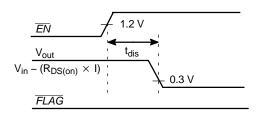
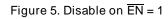


Figure 4. Shutdown on Overvoltage Detection





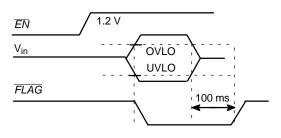
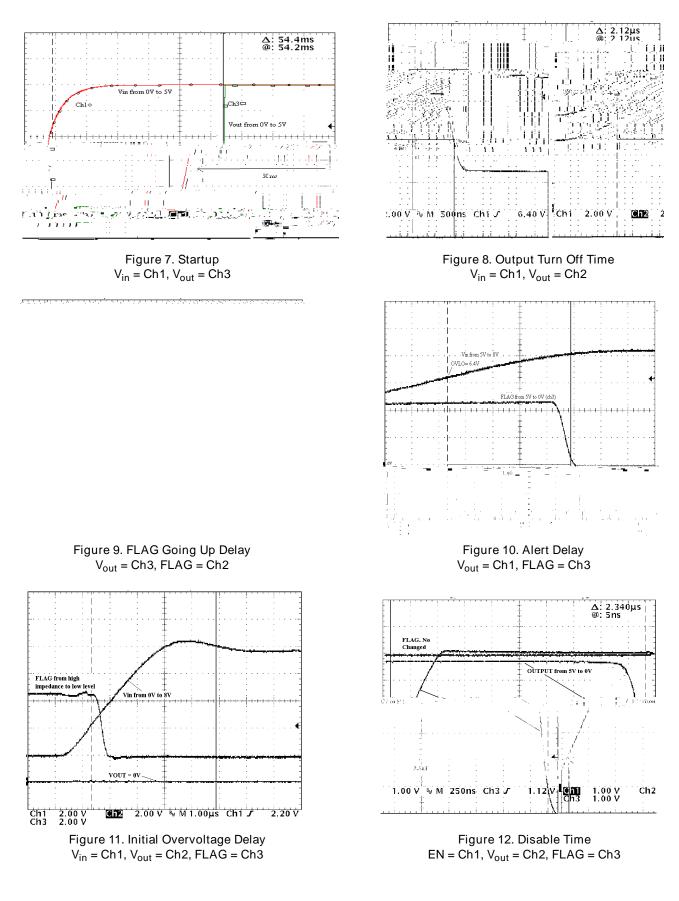
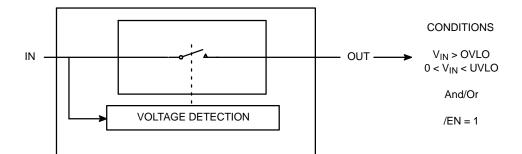


Figure 6. \overline{FLAG} Response with $\overline{EN} = 1$

TYPICAL OPERATING CHARACTERISTICS







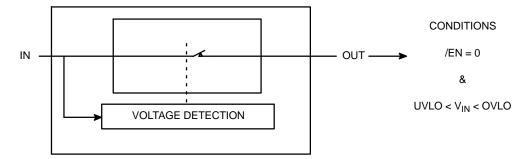


Figure 17. Simplified Diagram

Operation

The NCP347 provides overvoltage protection for positive voltage, up to 28 V. A Low $R_{DS(on)}$ NMOS FET protects the systems (i.e.: charger) connected on the Vout pin, against positive overvoltage. At powerup, with \overline{EN} pin = low, the output is rising up 50 ms after the input

overtaking undervoltage UVLO (Figure 3). The NCP347 provides a FLAG output, which alerts the system that a fault has occurred. A 50 ms additional delay, regarding available output (Figure 3) is added between output signal rising up and to FLAG signal rising up. FLAG pin is an open drain output.

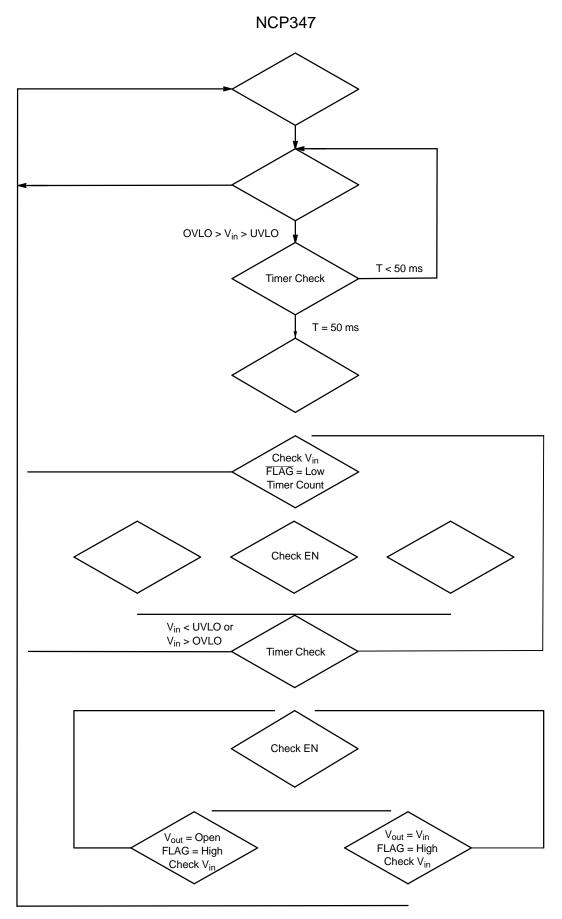


Figure 18. State Machine

Undervoltage Lockout (UVLO)

To ensure proper operation under any conditions, the device has a built-in undervoltage lockout (UVLO) circuit. During V_{in} positive going slope, the output remains disconnected from input until V_{in} voltage is below 2.92 V, plus hysteresis, nominal. The FLAG output is tied to low as long as V_{in} does not reach UVLO threshold. This circuit has a 60 mV hysteresis to provide noise immunity to transient condition. Additional UVLO thresholds ranging from UVLO can be manufactured. (See Selection Guide on page 12) Contact your ON Semiconductor representative for availability.

Overvoltage Lockout (OVLO)

To protect connected systems on V_{out} pin from overvoltage, the device has a built-in overvoltage lockout (OVLO) circuit. During overvoltage condition, the output remains disabled as long as the input voltage exceeds 5.675 V typical (NCP347MTAE). Additional OVLO thresholds ranging from OVLO can be manufactured. (See Selection Guide on page 12) Contact your ON Semiconductor representative for availability.

FLAG output is tied to low until V_{in} is higher than OVLO. This circuit has a 90 mV hysteresis to provide noise immunity to transient conditions.

FLAG Output

The NCP347 provides a FLAG output, which alerts external systems that a fault has occurred.

This pin is tied to low as soon the OVLO threshold is exceeded or when the V_{in} level is below the UVLO threshold. When V_{in} level recovers normal condition, FLAG is held high, keeping in mind that an additional 50 ms delay has been added between available output and FLAG = high. The pin is an open drain output, thus a pull up resistor (typically 1 M Ω , minimum 10 k Ω) must be added to V_{bat}. Minimum V_{bat} supply must be 2.5 V. The FLAG level will always reflects V_{in} status, even if the device is turned off ($\overline{EN} = 1$).

EN Input

To enable normal operation, the EN pin shall be forced to low or connected to ground. A high level on the pin, disconnects OUT pin from IN pin. EN does not overdrive an OVLO or UVLO fault.

Internal NMOS FET

The NCP347 includes an internal Low $R_{DS(on)}$ NMOS FET to protect the systems, connected on OUT pin, from positive overvoltage. Regarding electrical characteristics, the $R_{DS(on)}$, during normal operation, will create low losses on V_{out} pin.

As example: $R_{load} = 8.0 \Omega$, $V_{in} = 5.0 V$ Typical $R_{DS(on)} = 65 m\Omega$, $I_{out} = 618 mA$

 $V_{out} = 8 \times 0.618 = 4.95 V$

NMOS losses = $R_{DS(on)} \times lout^2 = 0.065 \times 0.618^2 = 25 \text{ mW}$

ESD Tests

The NCP347 input pin fully supports the IEC61000–4–2. 1.0 μ F (minimum) must be connected between V_{in} and GND, close to the device.

That means, in Air condition, V_{in} has a \pm 15 kV ESD protected input. In Contact condition, V_{in} has \pm 8.0 kV ESD protected input.

Please refer to Figure 19 to see the IEC 61000-4-2 electrostatic discharge waveform.

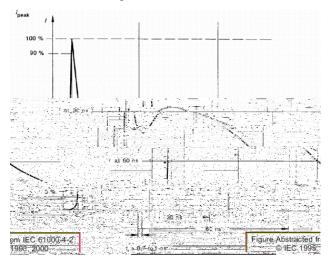
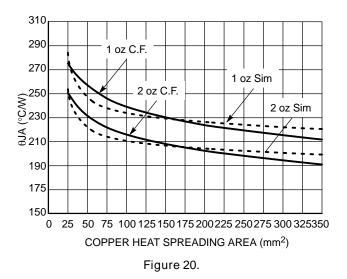


Figure 19. Electrostatic Discharge Waveform

PCB Recommendations

The NCP347 integrates a 2 amperes rated NMOS FET,



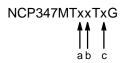
ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NCP347MTAETBG	BAL		
NCP347MTAFTBG	BAM	WDFN-10	3000 / Tape & Reel
NCP347MTAHTBG	BAK	(Pb-Free) S0007 Tape & Kee	
NCP347MTAITBG	ACJ		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SELECTION GUIDE

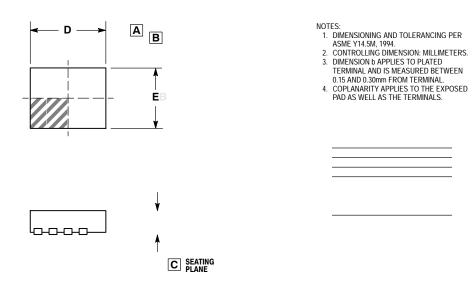
The NCP347 can be available in several undervoltage and overvoltage thresholds versions. Part number is designated as follows:



Code	Contents
а	UVLO Typical Threshold a: A = 2.95 V
b	OVLO Typical Threshold b: E = 5.63 V b: F = 5.90 V b: H = 7.20 V b: I = 5.85 V
с	Tape & Reel Type c: B = 3000

WDFN10 2.5x2, 0.5P CASE 516AA ISSUE C

DATE 06 FEB 2007



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