Fixed Current-Limiting Power-Distribution Switches

NCP382

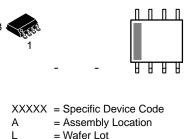
The NCP382 is a single input dual outputs high side power–distribution switch designed for applications where heavy capacitive loads and short–circuits are likely to be encountered. The device includes an integrated 80 m Ω , P–channel MOSFET. The device limits the output current to a desired level by switching into a constant–current mode when the output load exceeds the current–limit threshold or a short is present. The current–limit threshold is internally fixed. The power–switches rise and fall times are controlled to minimize current ringing during switching.

The $\overline{\text{FLAG}}$ logic output asserts low during overcurrent or overtemperature conditions. The switch is controlled by a logic enable input active high or low.

Features

- 2.5 V 5.5 V Operating Range
- 80 mΩ High–Side MOSFET
- Current Limit: Fixed 500 mA, 1 A and 1.5 A
- Undervoltage Lock–Out (UVLO)
- Soft-Start Prevents Inrush Current
- Thermal Protection
- Soft Turn–Off
- Enable Active High or Low (EN or \overline{EN})
- Compliance to IEC61000–4–2 (Level 4)
 - 8.0 kV (Contact)
 - 15 kV (Air)
- UL Listed for SOIC package (NCP382xDxxxx) File No. E343275
- IEC60950 -

dimensions section on page 10 of this data sheet.



- = Year
- W = Work Week

Υ

= Pb–Free Package

ORDERING INFORMATION

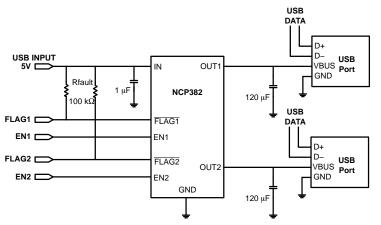
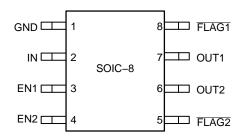
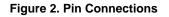


Figure 1. Typical Application Circuit





PIN FUNCTION DESCRIPTION

Pin Name	Туре	Description
EN1	I	Enable 1 input, logic low/high (i.e. EN or EN) turns on power switch.
EN2	I	Enable 2 input, logic low/high (i.e. EN or EN) turns on power switch.
GND	Р	Ground connection.
IN	Р	Power–switch input voltage; connect a 1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.
FLAG1	0	Active–low open–drain output 1, asserted during overcurrent or overtemperature conditions. Connect a 10 k Ω or greater resistor pull–up, otherwise leave unconnected.
FLAG2	0	Active–low open–drain output 2, asserted during overcurrent or overtemperature conditions. Connect a 10 k Ω or greater resistor pull–up, otherwise leave unconnected.
OUT1	0	Power–switch output1; connect a 1 μ F ceramic capacitor from OUT1 to GND, as close as possible to the IC. This minimum value is recommended for USB requirement in terms of load transient response and strong short circuits.
OUT2	0	Power–switch output2; connect a 1 μ F ceramic capacitor from OUT2 to GND, as close as possible to the IC. This minimum value is recommended for USB requirement in terms of load transient response and strong short circuits.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
From IN to OUT1, From IN to OUT2 Supply Voltage (Note 1)	V _{IN} , V _{OUT1} , V _{OUT2}	-7.0 to +7.0	V
IN, OUT1,OUT2, EN1, EN2, FLAG1, FLAG2 (Note 1)	V _{IN,} V _{OUT1,} V _{OUT2,} V _{EN1,} V _{EN2,} Vflag1, Vflag2	-0.3 to +7.0	V
FLAG1, FLAG2 sink current	I _{SINK}	1.0	mA

ESD Withstand Voltage (IEC 61000–4–2) (output only, when bypassed with 1.0 μF capacitor minimum)

NCP382

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between $-40^{\circ}C$ to $+85^{\circ}C$ and T_J up to $+125^{\circ}C$ for V_{IN} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^{\circ}C$ and $V_{IN} = 5$ V.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
POWER S	POWER SWITCH						
R _{DS(on)}	Static drain-source on-state resistance	$T_J = 25^{\circ}C$, $V_{IN} = 3.6$ V to 5 V		80	110	mΩ	
		$V_{IN} = 5 V -40^{\circ}$					

NCP382

IN	OUT1								
NCP382									
	GND								

_

Enable Input

Enable pin must be driven by a logic signal (CMOS or TTL compatible) or connected to the GND or VIN. A logic low on $\overline{\text{ENX}}$ or high on ENX turns–on the device. A logic high on $\overline{\text{ENX}}$ or low on ENX turns off device and reduces the current consumption down to I_{INOFF}.

Blocking Control

The blocking control circuitry switches the bulk of the power MOS. When the part is off, the body diode limits the

APPLICATION INFORMATION

Power Dissipation

The junction temperature of the device depends on different contributing factors such as board layout, ambient temperature, device environment, etc... Yet, the main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$\mathsf{P}_{\mathsf{D}} = \mathsf{R}_{\mathsf{DS}(\mathsf{on})} \times \left(\left(\mathsf{I}_{\mathsf{OUT1}} \right)^2 + \left(\mathsf{I}_{\mathsf{OUT2}} \right)^2 \right) \quad (\mathsf{eq. 2})$$

 P_{D}

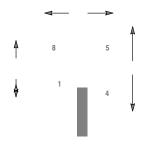
leakage current I_{REV} from OUTX to IN. In this mode, anode of the body diode is connected to IN pin and cathode is connected to OUTX pin. In operating condition, anode of the body diode is connected to OUTX pin and cathode is connected to IN pin preventing the discharge of the power supply. NCP382

ORDERING INFORMATION

Marking	Active Enable Level	Over Current Limit	Evaluation Board	UL 236 7	IEC60950 Ed2 (CB Scheme)	IEC60950 Ed2 Ad1, Ad2	Package	Shipping [†]
382L05		0.5 A	NCP382LD 05AAGEVB	Y	Y	Y		
	ENx Low	•	•		•			
							SOIC-8	2500 /
							(Pb-Free)	2000 /
	•	Marking Enable Level	MarkingEnable LevelCurrent Limit382L050.5 AENx	MarkingEnable LevelCurrent LimitEvaluation Board382L050.5 ANCP382LD 05AAGEVBENxNCP382LD 05AAGEVB	MarkingEnable LevelCurrent LimitEvaluation Board236 7382L050.5 ANCP382LD 05AAGEVBYENx	MarkingEnable LevelCurrent LimitEvaluation Board236 7Ed2 (CB Scheme)382L050.5 ANCP382LD 05AAGEVBYYENx	MarkingEnable LevelCurrent LimitEvaluation Board236 7Ed2 (CB Scheme)Ed2 Ad1, Ad2382L050.5 ANCP382LD 05AAGEVBYYYENx	MarkingEnable LevelCurrent LimitEvaluation Board236 7Ed2 (CB Scheme)Ed2 Ad1, Ad2Package382L050.5 ANCP382LD 05AAGEVBYYYSACENx Low



DATE 16 FEB 2011



SEATING PLANE



onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. Onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or incruit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi