The NCP4302 is a full featured controller and driver that provide all the control and protection functions necessary for implementing a synchronous rectifier operation in a flyback converter. With the use of the NCP4302, the space conscious flyback applications such as Adaptors, chargers, set top boxes can achieve significant efficiency improvements at minimal extra cost. In addition to the synchronous rectifier control, the IC incorporates an accurate TL431 type shunt regulator, current monitoring circuit and optocoupler driver to provide a single IC secondary solution. The NCP4302 works with any type of flyback topology (continuous mode, Quasi−resonant mode or discontinuous mode) – providing a high level of versatility.

Features

- Self−contained Control of Synchronous Rectifier in CCM, DCM, and QR Flyback Applications
- Interface to External Signal for CCM Mode
- True Secondary Zero Current Detection
- High Gate Drive Currents (2.5 A Source/Sink)
- High Voltage Operation
- Current Sense Flexibility (MOSFET $R_{DS(on)}$ OR CS Resistor)
- Accurate Low Voltage Reference
  − NCP4302A 2.55 V, 1%
  − NCP4302B 1.275 V, 1%
- Programmable Independent Secondary Side t_{on} and t_{off} Delays
- Maximum Frequency of Operation up to 250 kHz
- These are Pb−Free Devices

Typical Applications

- Notebook Adapters
- LCD TV Adapters
- Consumer Appliances such as DVD, VCR
- Power Over Ethernet Applications (IP phones, Wireless Access Points)
- Battery Chargers

PIN CONFIGURATION

PIN DESCRIPTION

Pin Number	Symbol	Description
1	SYNC/CS	Connected to the flyback winding. The current on this pin is sensed and used to turn on the Synchronous Rectification MOSFET (SRFET). This pin is also used to sense the zero crossing of the MOSFET current either using the $R_{DS(on)}$ of the SRFET or using an external current sense resistor connected between drain of the SRFET and the flyback winding.
2	TRIG	Input pin for direct turn−off of the MOSFET. Typically connected to a signal from primary controller (for CCM mode) or a signal derived from the transformer (for QR mode). Has very short propagation delay to output (<50 ns).
3	CATH	Feedback compensation pin for the TL431 shunt regulator. Has the capability to sinking 10 ma of opto current.
4	V_{REF}	Output voltage feedback through resistive divider connected to this pin. Regulated at 1.28 V (option B) or 2.55 V (option A).
5	D_{LYADJ}	A resistive divider between the power supply output and ground with the center point tied to the D_{LYADJ} input pin allows for independent adjustment of the minimum t_{on} and t_{off} delay time. The maximum external capacitance from this pin to ground is 25 pF.
6	GND	Return pin for the controller – connected to the output return.
7	DRV	Drive output for external MOSFET – 2.5 A peak drive capability, internally clamped to 13.5 V (Maximum)
8	V_{CC}	Bias voltage for the controller. Maximum voltage is 28 V.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Current	V_{CC} I_{CC}	−0.3 to 28 100	V mA
Drive Voltage Current	V_{DRV}	−0.3 to 18 100	V mA
Drive Current Source Sink	I_{DRV}	 2.5 −2.5	Apk
Analog and Logic Inputs	TRIG, V_{REF}, D_{LYADJ}	−0.3 to 10 100	V mA
Maximum Voltage Current	SYNC/CS	− 10 to 95 100	V mA
Operating Junction Temperature Range	T_J	−40 to 125	°C
Maximum Junction Temperature	T_{Jmax}	150	°C
Storage Temperature Range	T_{Smax}	−65 to 150	°C
Lead Temperature (Soldering, 10 s)	T_{Lmax}	300	°C
Reference input Current, continuous	I_{REF}	−0.05 to 10	mA
Total Power Dissipation	P_D	225	mW
Thermal Resistance Junction−to−Ambient	θ_{JA}	178	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Pin 1−8: Human Body Model 2000 V per JEDEC Standard JESD22, Method A114E.
   Machine Model (MM) 200 V per JEDEC Standard JESD22, Method A115A.
2. This device contains Latch−up protection and exceeds ±100 ma per JEDEC Standard JESD78

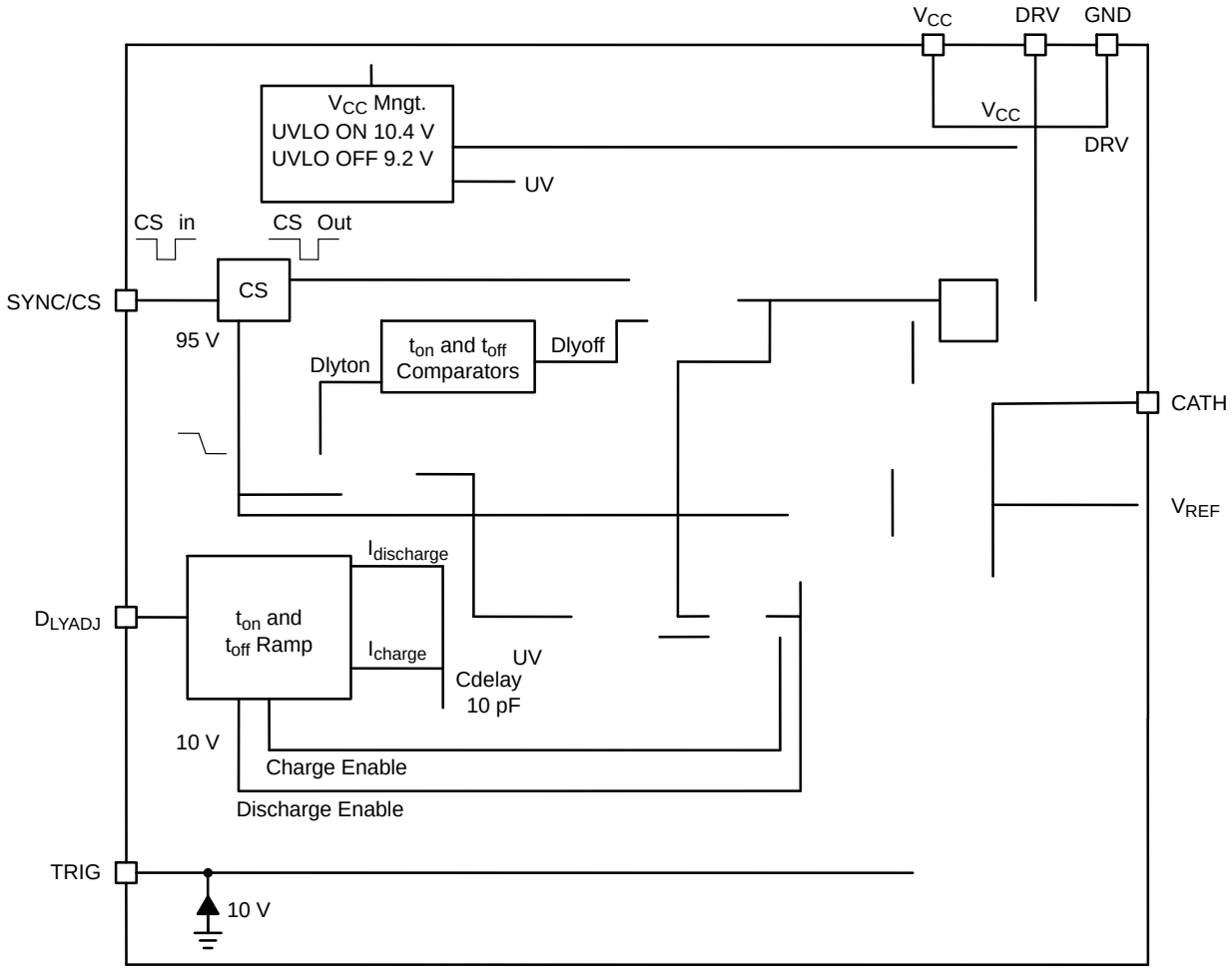


Figure 1. Block Diagram

ELECTRICAL CHARACTERISTICS

(V_{CC} = 19 V, Sync frequency = 100 kHz, V_{REF} = V_{KA} (I_{KA} = 1 mA), R_S = 75 ohms, V_{TRIG} = GND, C_{DRV} = 1 nF, R_{DLYADJ} = 30.1 k, V_{DLYADJ} = 2.0 V, for typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, unless otherwise noted)

Rating	Test Conditions	Symbol	Min	Typ	Max	Unit

TYPICAL CHARACTERISTICS

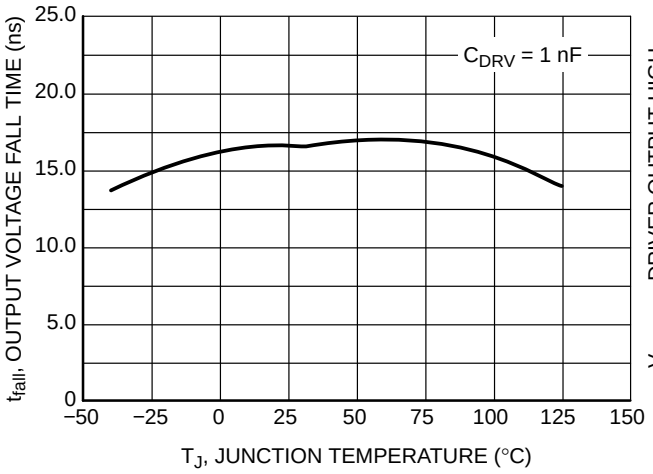


Figure 7. Drive Output Fall−time vs. Junction Temperature

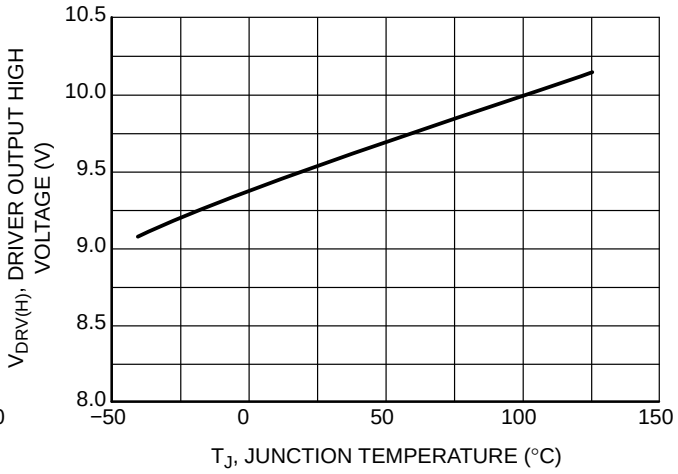


Figure 8. Driver V_{out} High vs. Junction Temperature

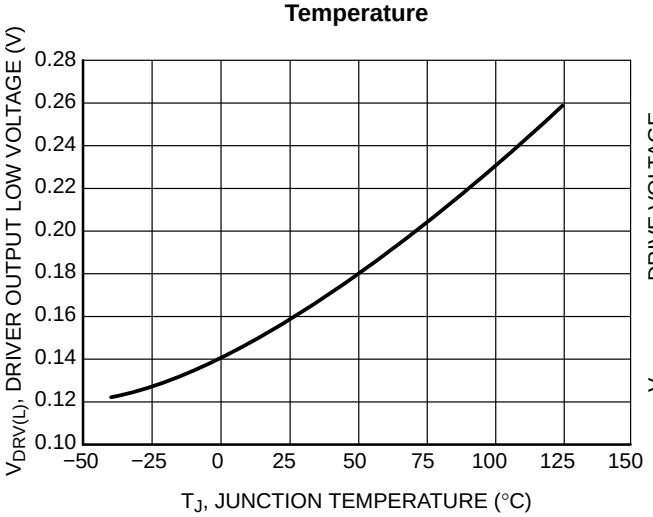


Figure 9. Driver V_{out} Low vs. Junction Temperature

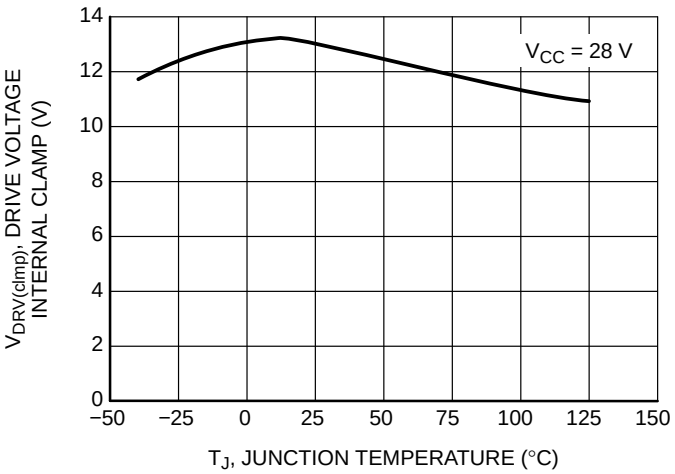


Figure 10. V_{gate} Clamp vs. Junction Temperature

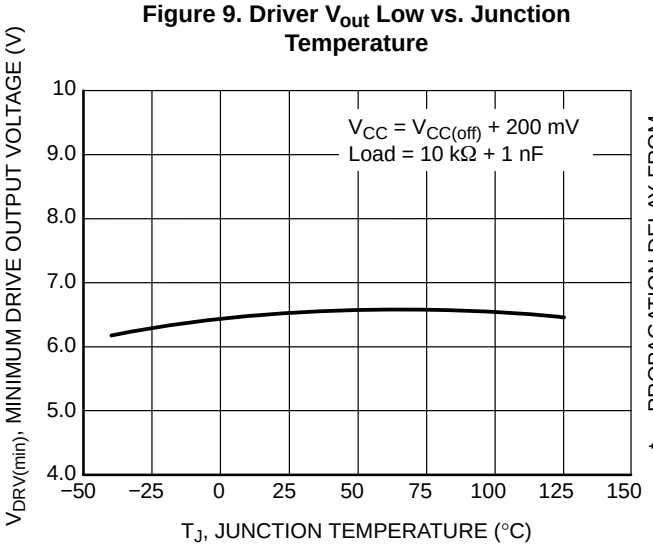


Figure 11. $V_{OUT(min)}$ vs. Junction Temperature

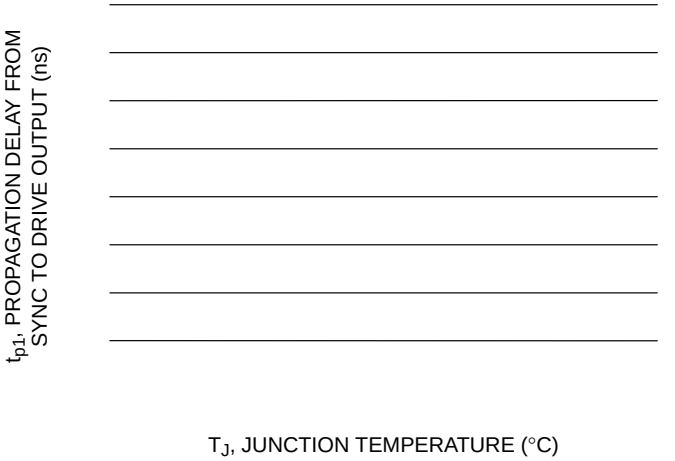


Figure 12. t_{p1} Propagation Delay, SYNC/CS to DRIVE vs. Junction Temperature

TYPICAL CHARACTERISTICS

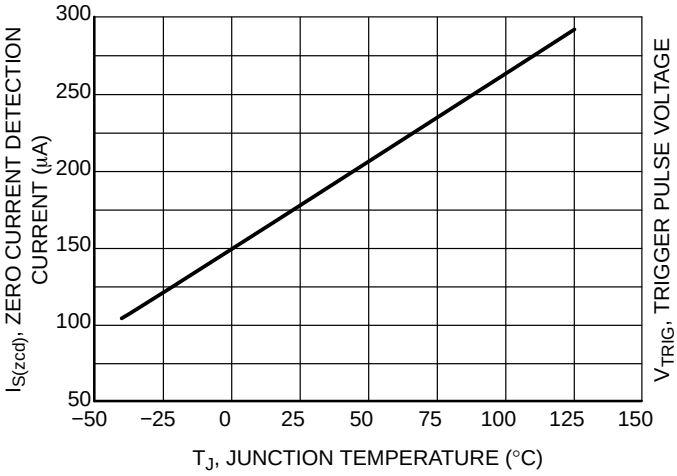


Figure 13. Zero Current Detect I_{source} vs. Junction Temperature

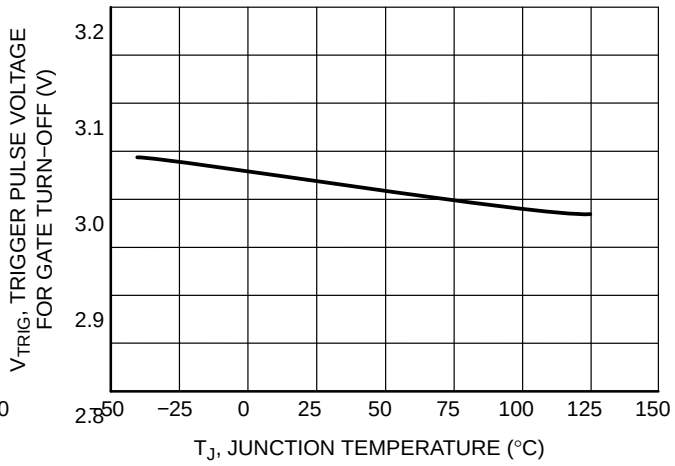


Figure 14. Trigger Pulse Voltage for Gate Turn−off vs. Junction Temperature

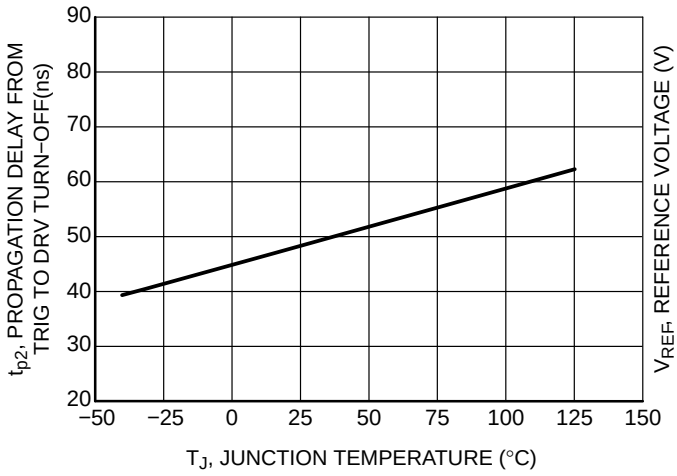


Figure 15. t_{p2} Propagation Delay TRIG in to DRIVE Off, NO Load vs. Junction Temperature

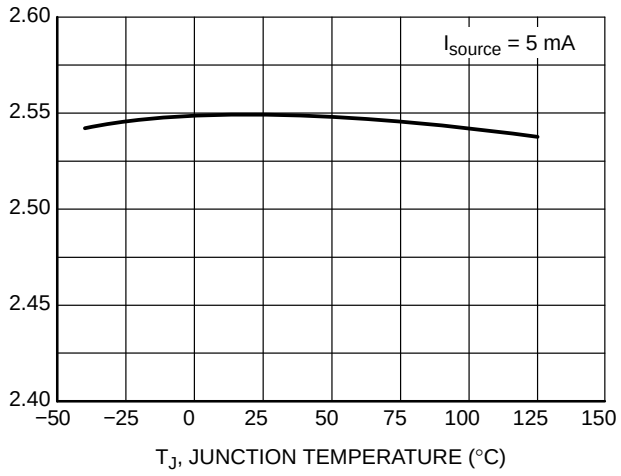


Figure 16. 2.55 V Reference (Option A) Voltage vs. Junction Temperature

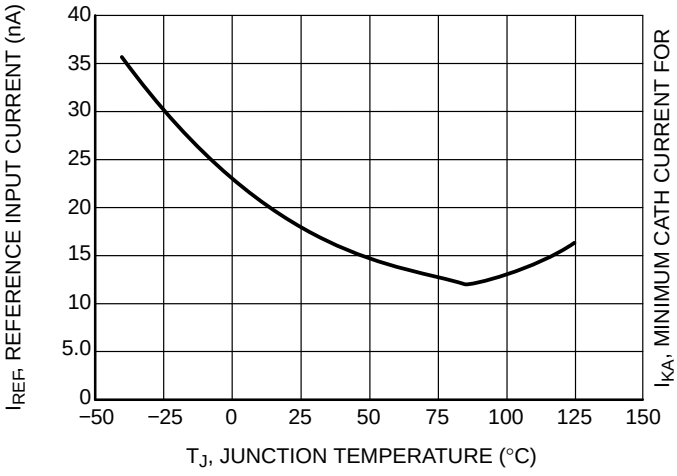


Figure 17. 2.55 V Reference Input Current vs. Junction Temperature

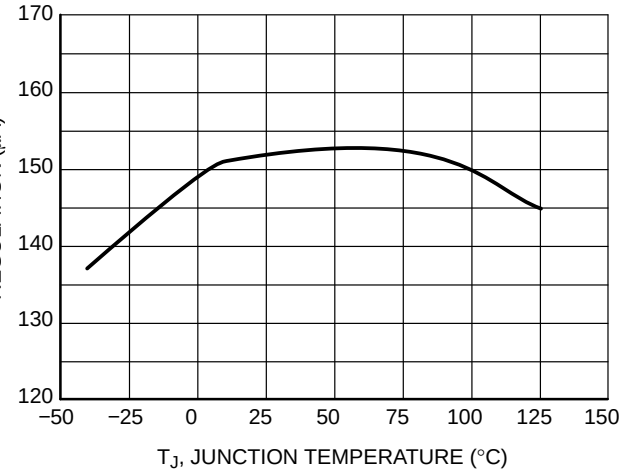


Figure 18. 2.55 V Reference Minimum Cathode Current for Regulation vs. Junction Temperature

TYPICAL CHARACTERISTICS

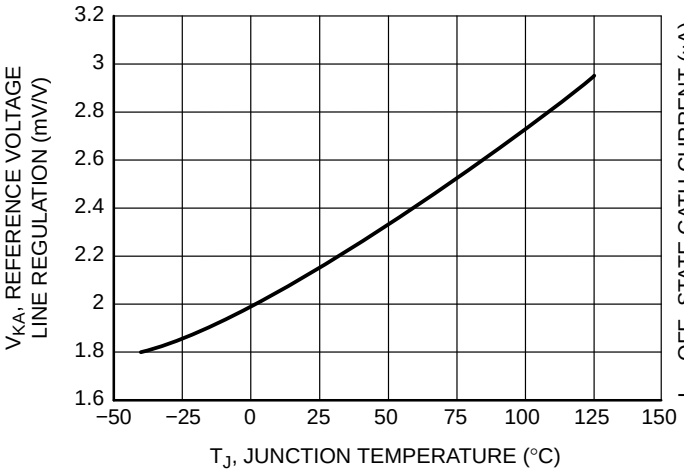


Figure 19. 2.55 V Reference Line Regulation vs. Junction Temperature

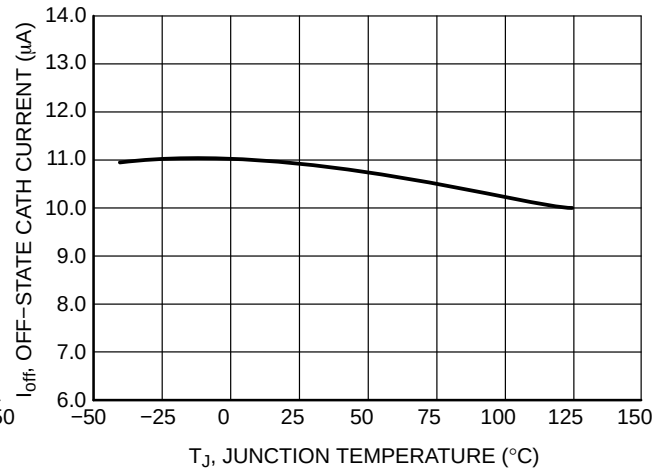


Figure 20. 2.55 V Reference Off−State Cathode Current vs. Junction Temperature

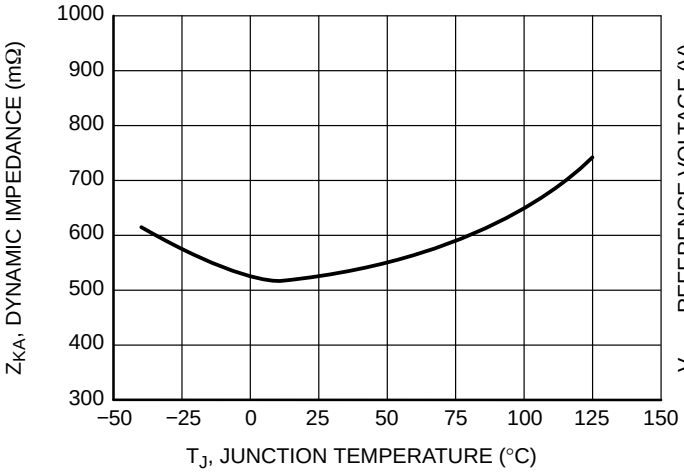


Figure 21. 2.55 V Reference Dynamic Impedance vs. Junction Temperature

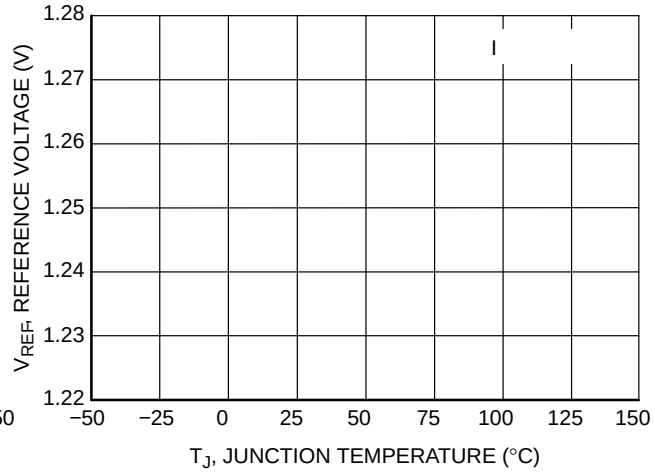


Figure 22. 1.275 V Reference Voltage (Option B) vs. Junction Temperature

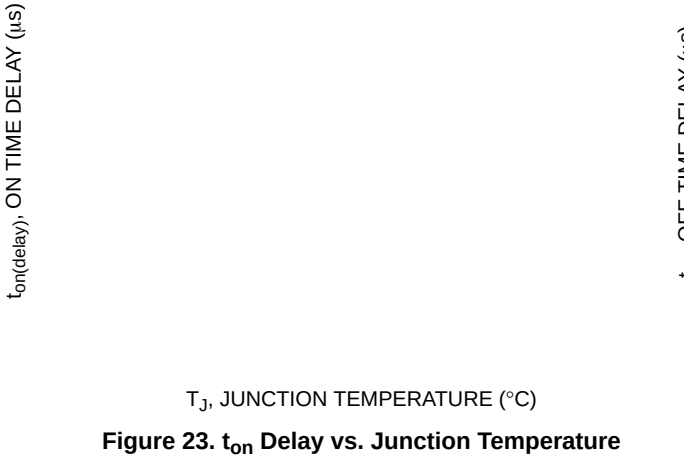


Figure 23. t_{on} Delay vs. Junction Temperature

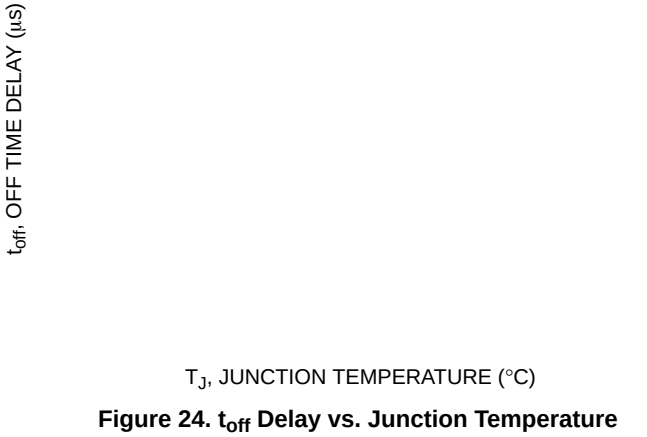


Figure 24. t_{off} Delay vs. Junction Temperature

Detailed Operating Description

The NCP4302 is designed to operate either as a standalone IC or as a companion IC to a primary side controller to help achieve efficient synchronous rectification for flyback converter systems. It has high current gate driver along with fast logic circuitry to provide appropriately timed drive signals to a synchronous MOSFET used for output rectification in a flyback converter. With its novel architecture, the NCP4302 has enough versatility to increase the synchronous rectification efficiency under any operating mode without requiring too much complexity.

Supply Section

The NCP4302 works from an available bias supply that can range from 10.4 V to 28 V (typical). This allows direct connection to the output voltage of many adapters such as notebook and LCD TV adapters. As a result, the NCP4302 simplifies circuit operation compared to other devices which require specific bias power supplies (e.g. 5 V). The high voltage capability of the V_{CC} is also a unique feature designed to allow operation across a broader range of applications. To prevent gate signal from operating under inadequate bias conditions, the NCP4302 features a UVLO circuit that turns on at 10.4 V (V_{CC} rising) typical and turns off at 9.2 V typical (V_{CC} falling).

Gate Drive Section

The NCP4302 features high current gate drivers delivering up to (>2.5 A peak) to achieve fast turn−on and turn−off requirements in a synchronous rectifier. Having a high gate drive current enables fast turn−on when SYNC/CS signal is

The minimum on time is set with a voltage divider with resistors R2 and R3 (refer to Figure 27).

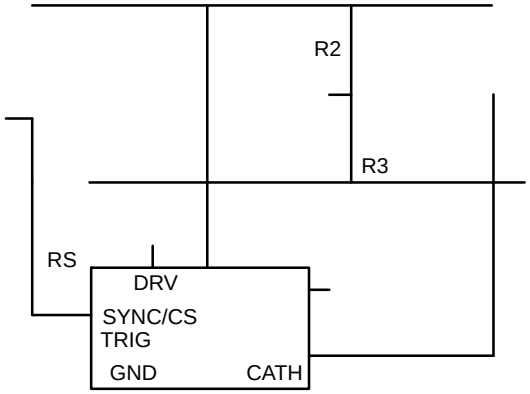
$$I_{in} = \left(\left(V_{out} \cdot \frac{R3}{R3 + R2}\right) - 0.7\right) \cdot \frac{1}{Rth}$$

Where Rth is the Thevenin equivalent resistance and is calculated by:

$$Rth = \frac{1}{\frac{1}{R3} + \frac{1}{R2}}$$

This input current is then used to charge an internal 10 pF capacitor setting the minimum t_{on} time.

$$t_{on(delay)} = 10\ pF \cdot \frac{4\ V}{I_{in}}$$



Discontinuous Condition Mode

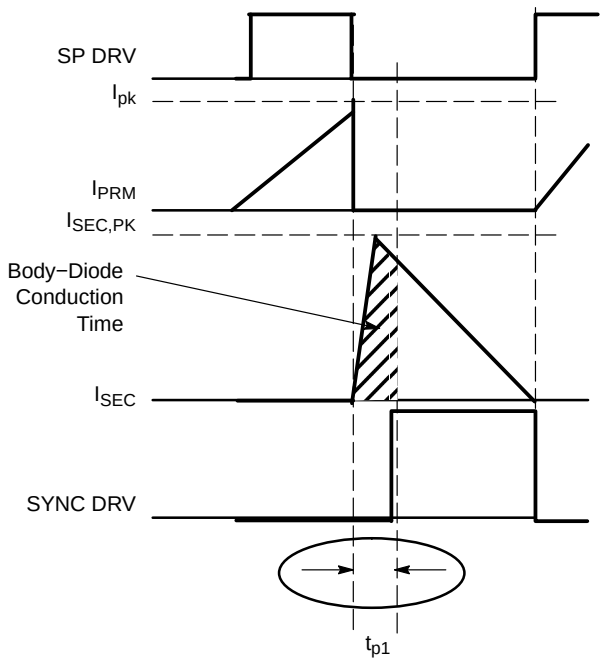


Figure 31. Discontinuous Conduction Mode Waveforms

t_{p1} is the propagation delay from the SYNC/CS input to the drive output.

Continuous Conduction Mode

When operating in continuous conduction mode (CCM) the current in the secondary doesn't fall to zero prior to turning on the primary side MOSFET. To eliminate cross conduction losses (have the primary side MOSFET and secondary side MOSFET on at the same time) the trigger input to the NCP4302 must be utilized. A signal which leads the Primary Side (SP) MOSFET turning on must be coupled to the TRIG input of the NCP4302 which will turn−off the SS MOSFET referring to Figure 32.

When the energy transfer begins in the transformer secondary, prior to the secondary side synchronous MOSFET turning−on, the secondary current flows through the synchronous rectifiers MOSFET's (SS) internal body diode (SSD). To minimize the power loss in the internal body the controller propagation delay has been minimized in the NCP4302.

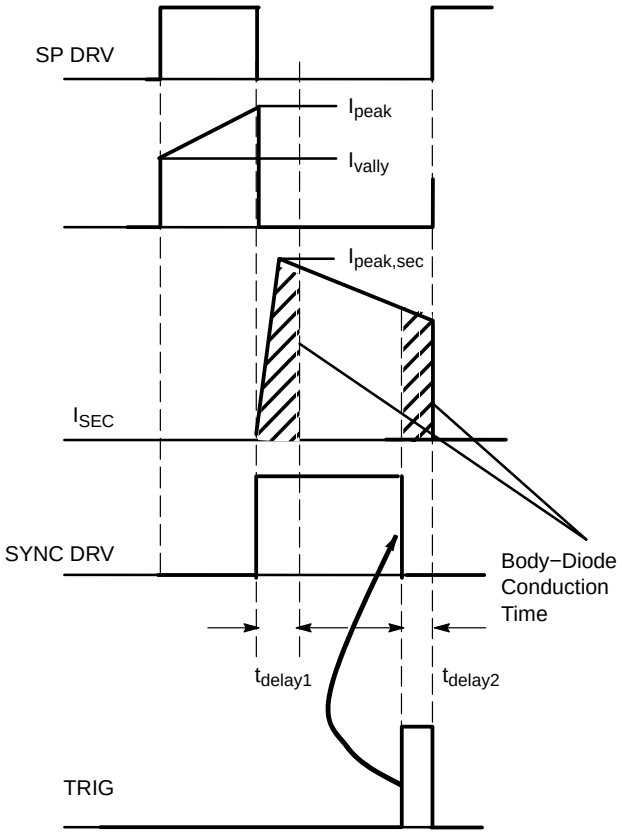


Figure 32. Continuous Conduction Mode Waveforms

$$P_{sync} = P_{ON} + P_{Qrr} + P_dP + PP_{OFF} \quad \text{(eq. 8)}$$

$$I_{sec,RMS} \approx \left(I_{sec,peak} - \frac{\Delta I_{L_{sec}}}{2}\right)\sqrt{1 - D} \quad \text{(eq. 9)}$$

$$I_{sec,RMS}{}^2 \approx \left(I_{sec,peak} - \frac{\Delta I_{L_{sec}}}{2}\right)^2 1 - D \quad \text{(eq. 10)}$$

Combining equations 9 and 10,

$$\Delta IL_{sec} = \frac{V_{OUT} + V_f}{\frac{LM}{n^2}}(1 - D)T \quad \text{(eq. 11)}$$

$$P_{on} = I_{sec,RMS}{}^2 \cdot R_{DS(on)} \quad \text{(eq. 12)}$$

$$P_{QRR} = Q_{RR}\left(V_{OUT} + \frac{V_{IN}}{n}\right)f \quad \text{(eq. 13)}$$

$$P_{BODY\_DIODE} = V_f \cdot I_{OUT} \cdot f(t_{delay1} + td_{delay2}) \quad \text{(eq. 14)}$$

$$P_{off} = \frac{1}{2}$$

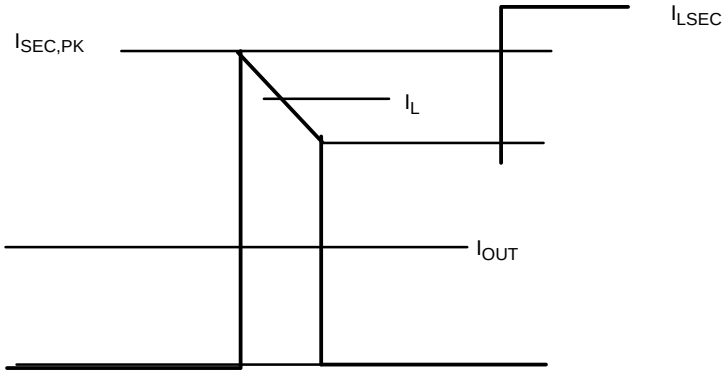


Figure 33.

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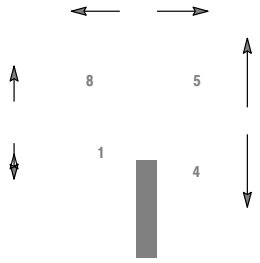

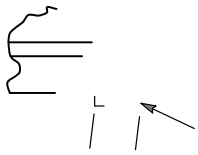

SEATING
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