





NCP4304A, NCP4304B

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{CC}	IC Supply Voltage		

NCP4304A, NCP4304B

TYPICAL CHARACTERISTICS

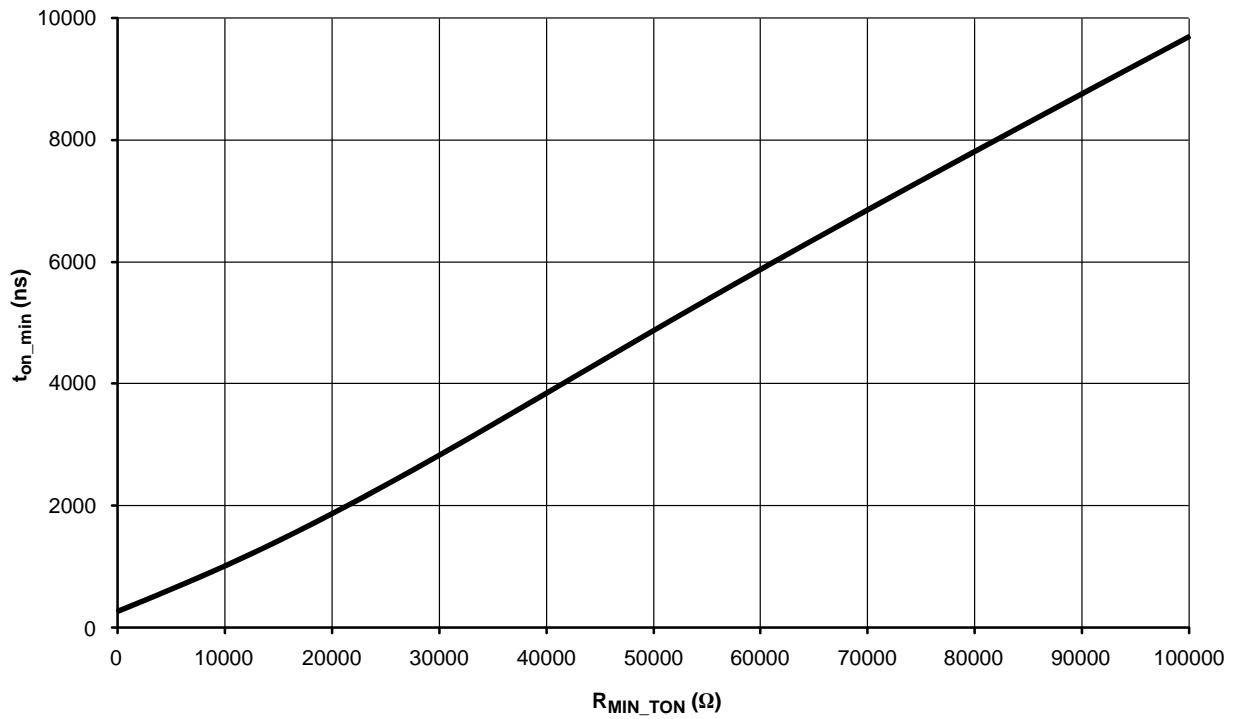


Figure 4. t_{on_min} on R_{MIN_TON} Dependency

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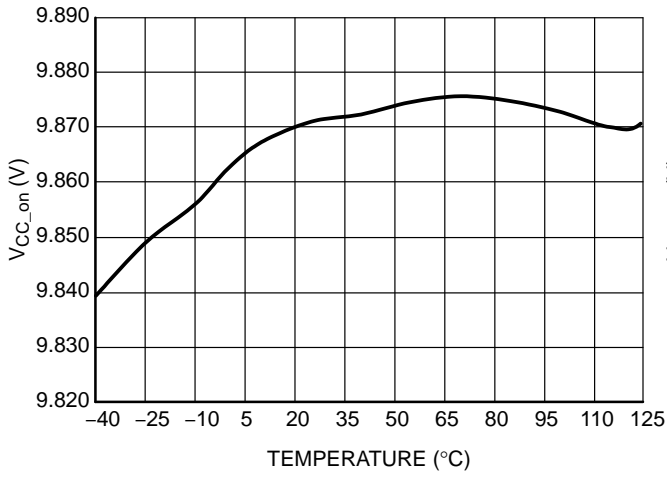


Figure 5. VCC Startup Voltage

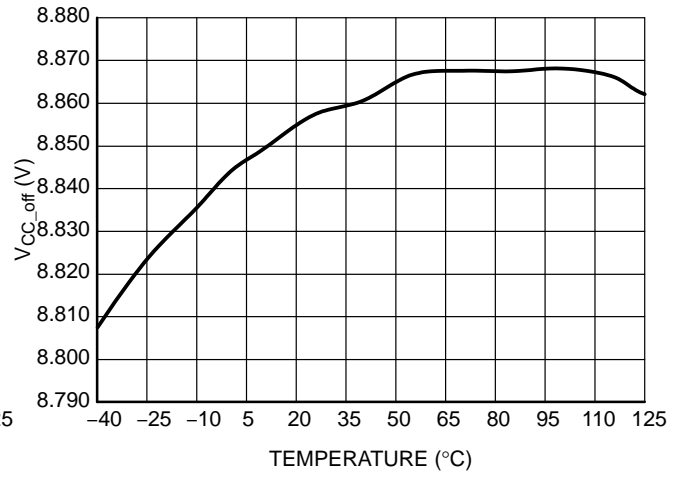


Figure 6. VCC Turn-off Voltage

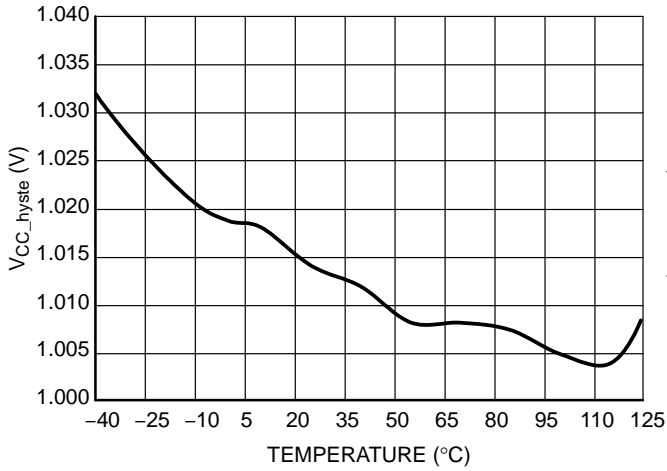


Figure 7. VCC Hysteresis

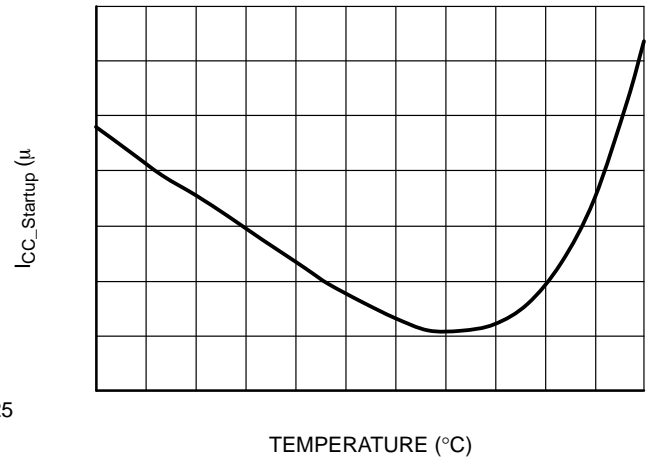
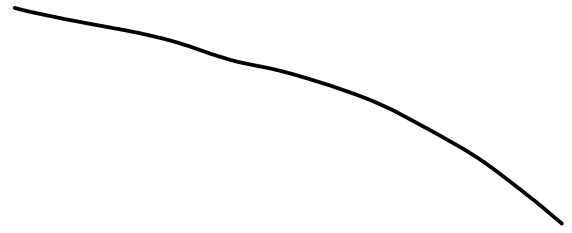
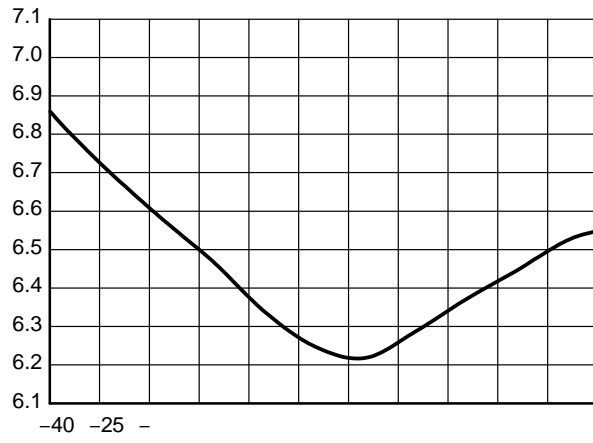


Figure 8. Startup Current

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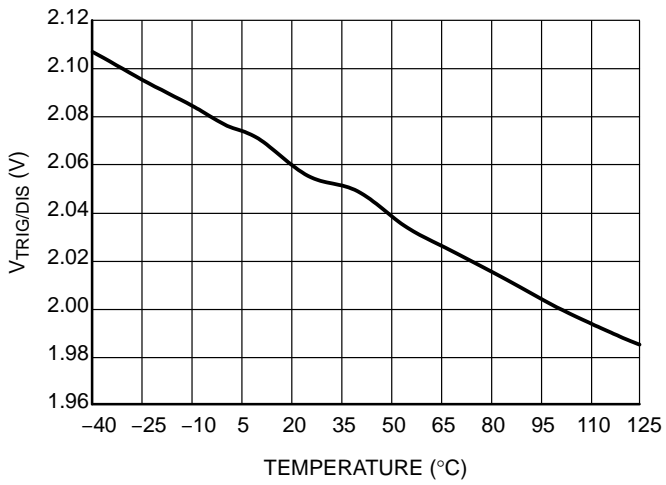


Figure 23. Trigger Input Threshold Voltage

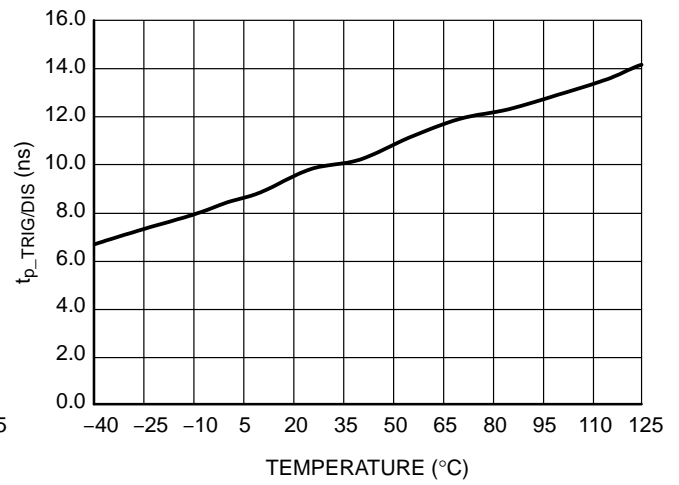


Figure 24. Propagation Delay from Trigger Input to DRV Turn-off

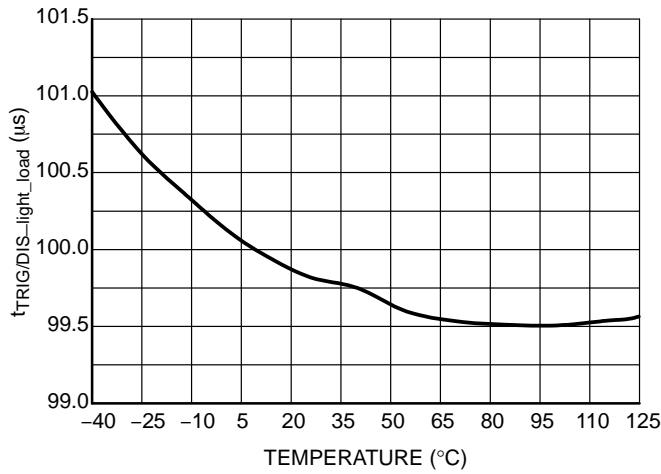
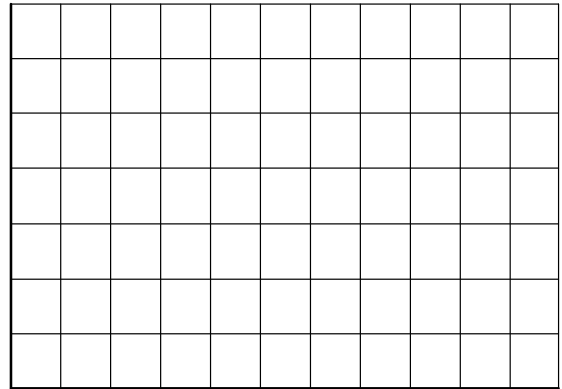


Figure 25. Light Load Transition Timer Duration



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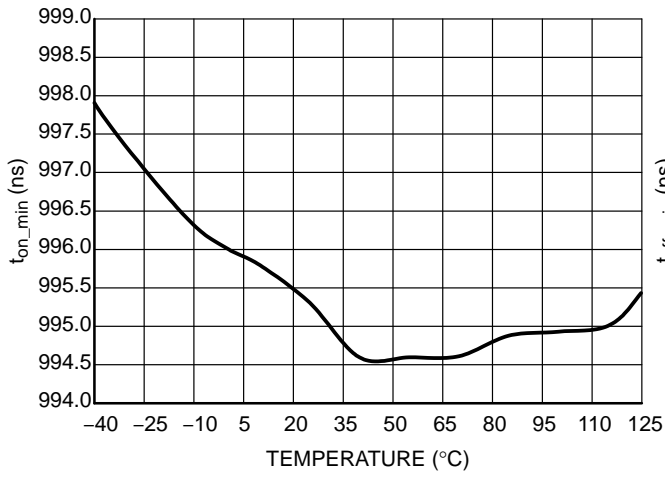


Figure 29. Minimum On Time @ R_{MIN_TON} = 10 kΩ

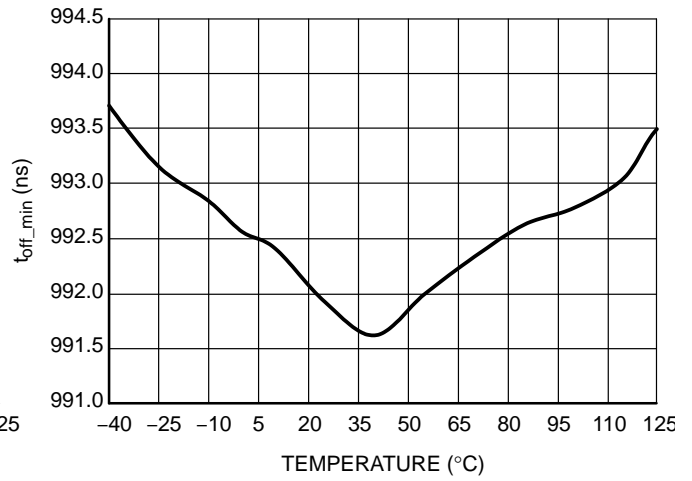


Figure 30. Minimum Off Time @ R_{MIN_TOFF} = 10 kΩ

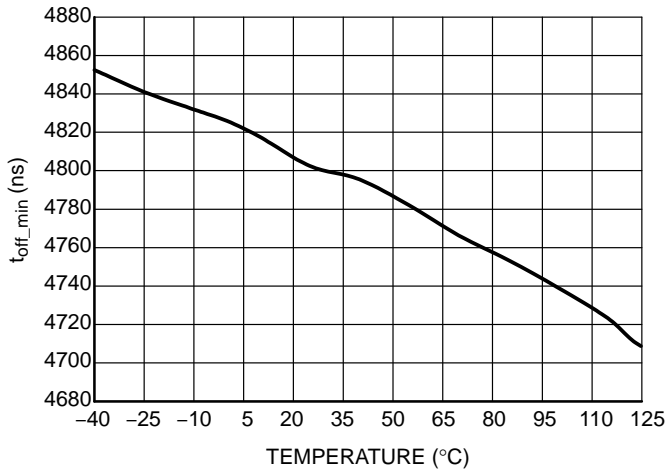


Figure 31. Minimum Off Time @ R_{MIN_TOFF} = 50 kΩ

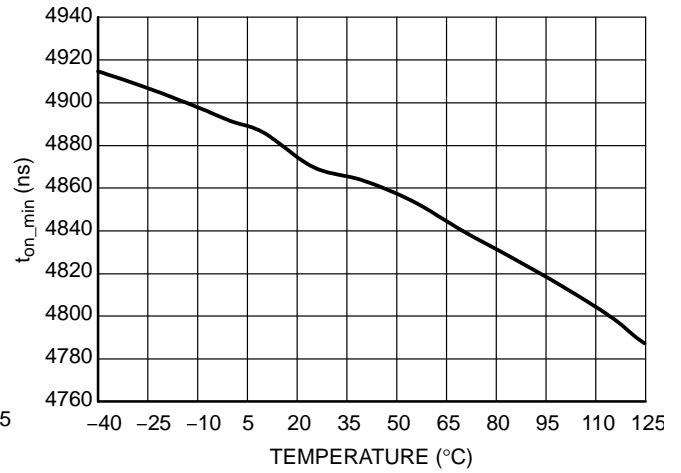
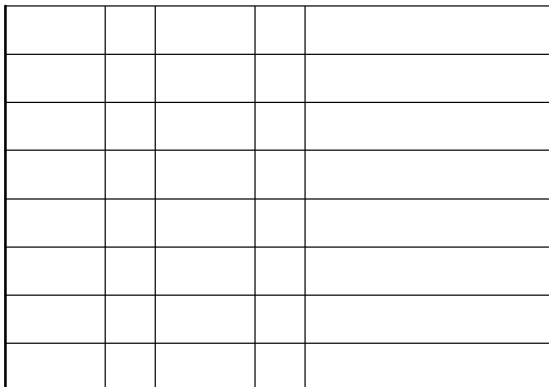
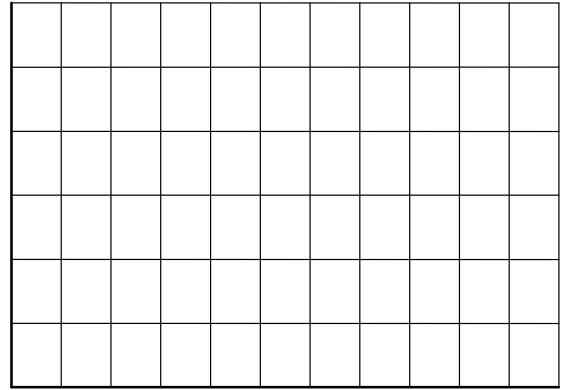
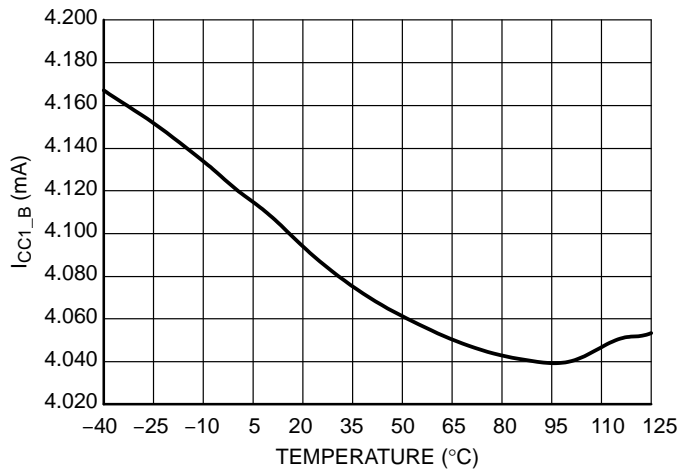


Figure 32. Minimum On Time @ R_{MIN_TON} = 50 kΩ



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**Figure 35. Internal IC Consumption (B version,
C_{DRV} = 0 nF, f_{SW} = 500 kHz,
t_{on_min} = 500 ns, t_{off_min} = 620 ns)**

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APPLICATION INFORMATION

General Description

μ

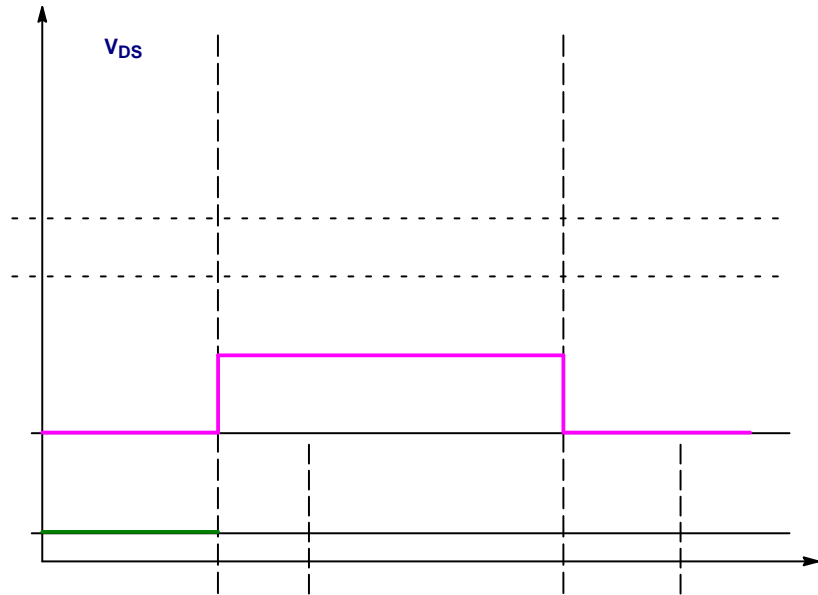


Figure 41. ZCD Comparators Thresholds and Blanking Periods Timing

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Figure 42. Waveforms from SR System Using MOSFET in TO-220 Package Without Parasitic Inductance

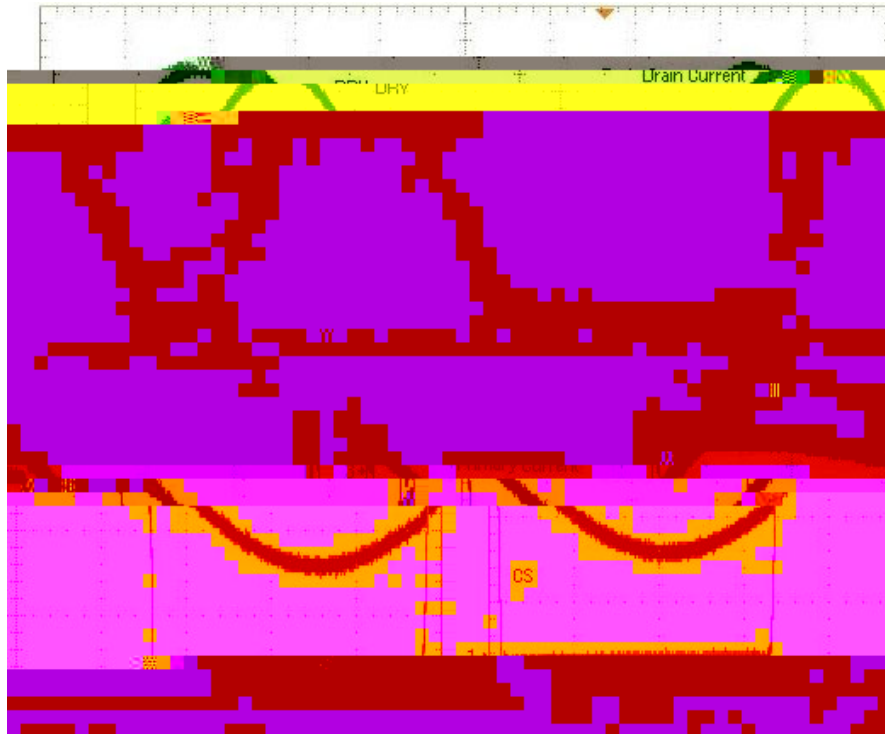
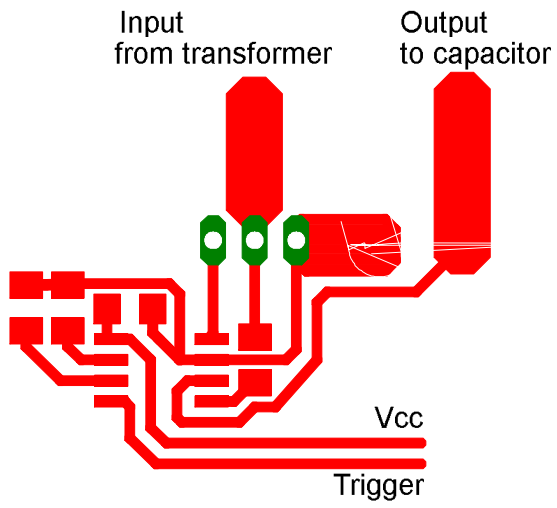


Figure 44. Waveforms SR System Using MOSFET in TO-220 Package with Parasitic Inductance Compensation – SR MOSFET Channel Conduction Time is Optimized

Ω

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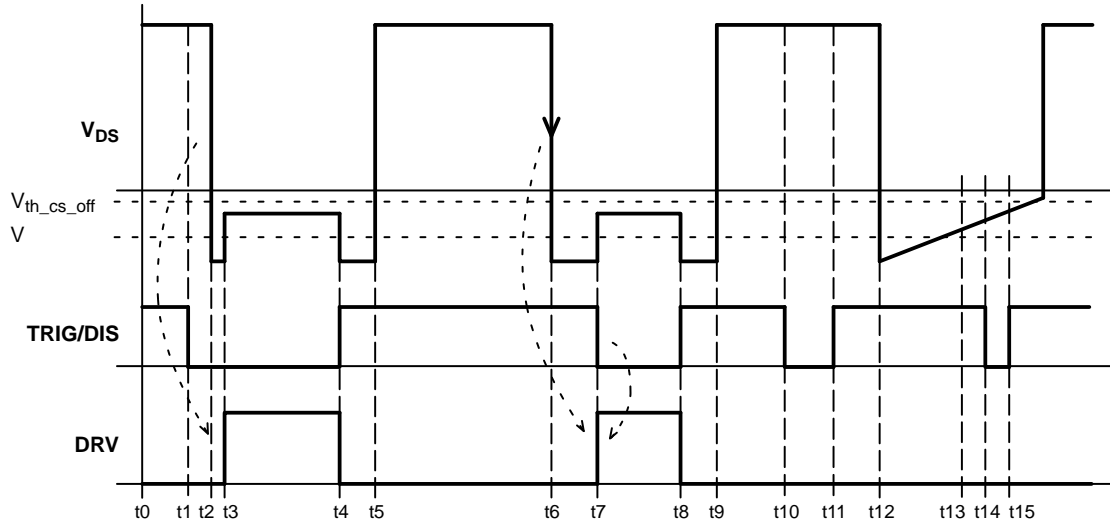


Figure 48. DRV Turn ON Events

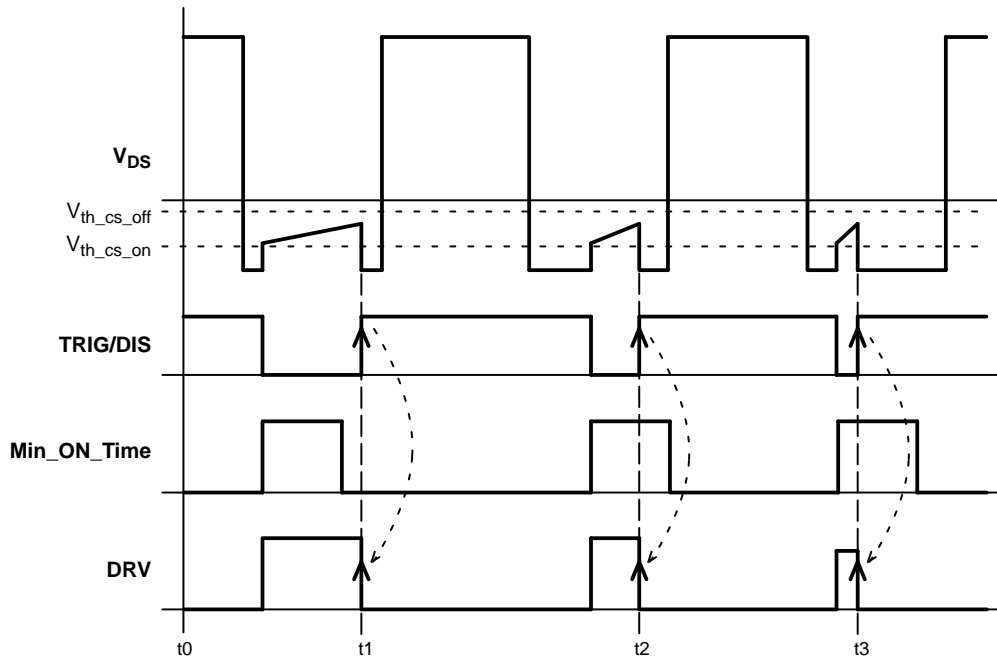


Figure 51. Driver Turn-OFF Events Based on the TRIG/DIS Input

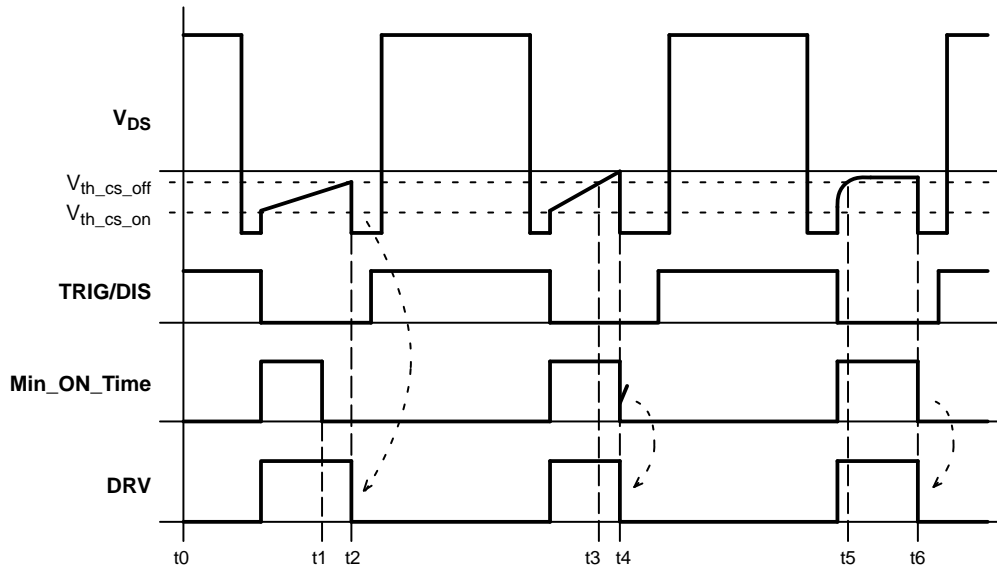


Figure 52. Driver OFF Sequence Chart 2

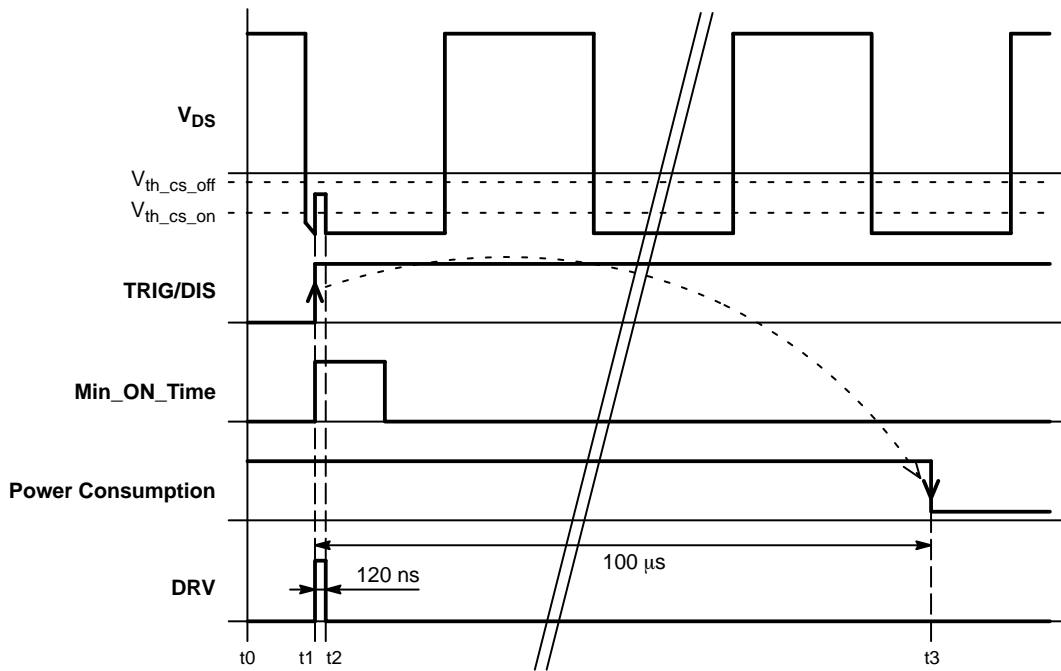


Figure 55. TRIG/DIS from LOW to HIGH Sequence 2

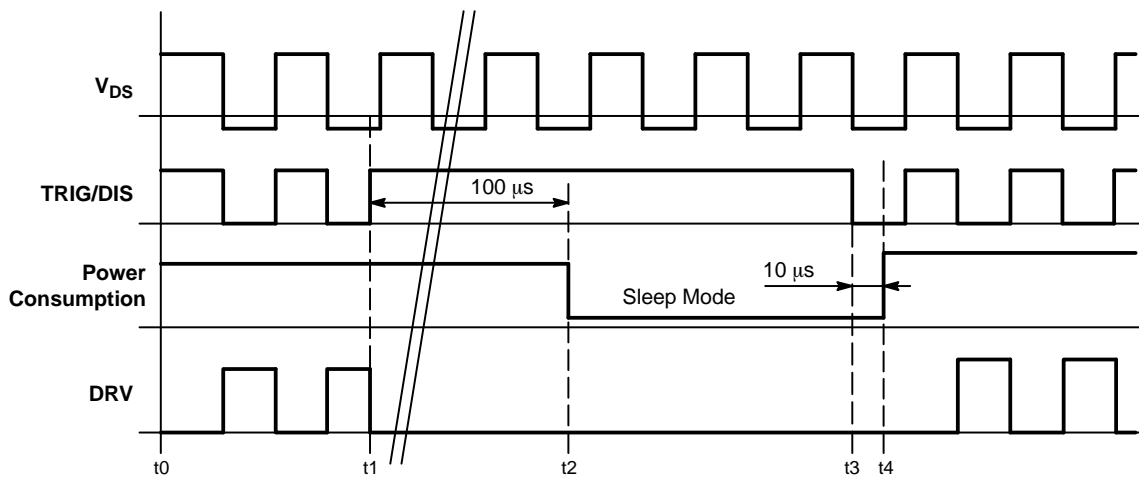


Figure 56. Sleep Mode Sequence

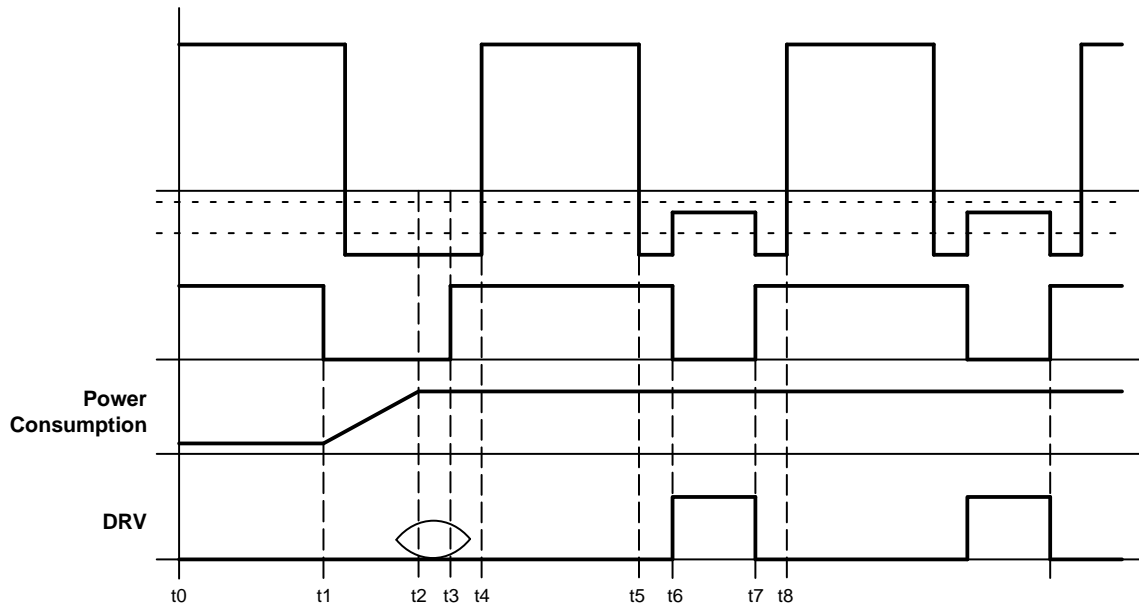


Figure 57. Waking-up Sequence

Figure 58. Wake-up Time Sequence

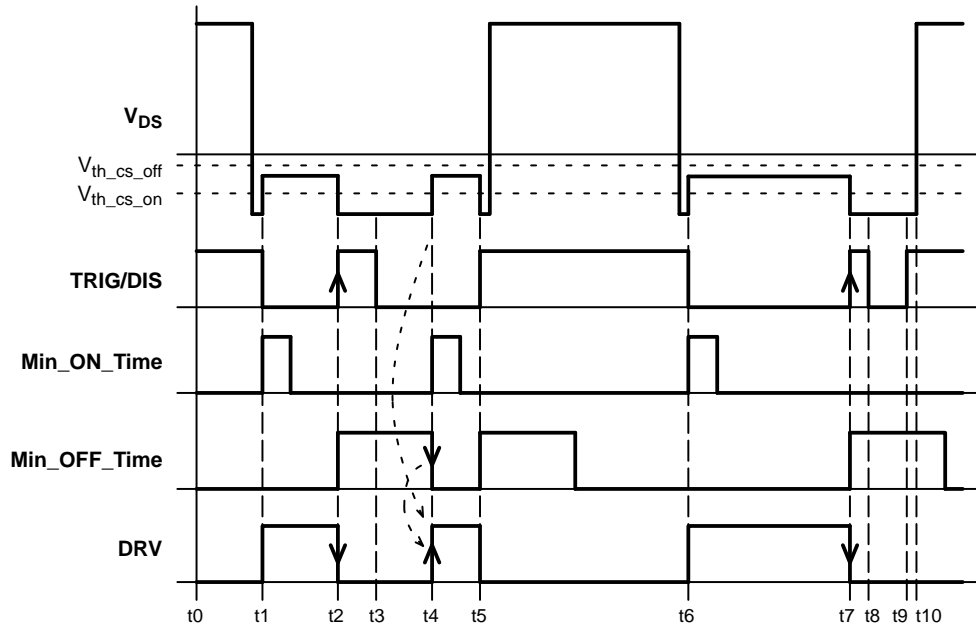


Figure 59. IC Behavior when Multiple Trigger Pulses Appear on TRIG/DIS Input

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NCP4304A, NCP4304B

Figure 66. Typical MOSFET Capacitance Dependency on V_{DS} and V_{GS} Voltage

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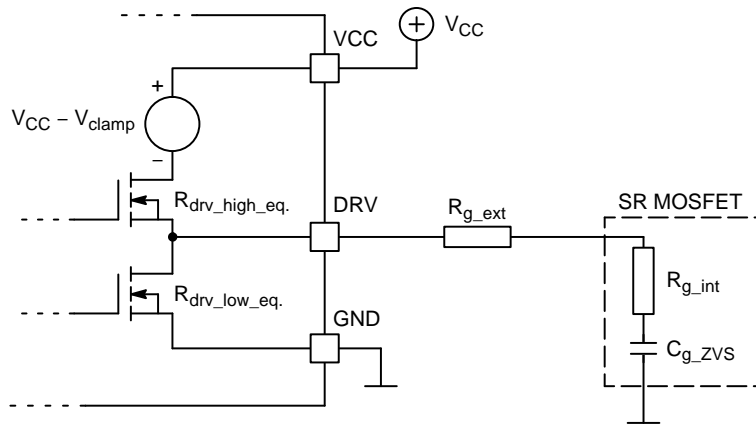
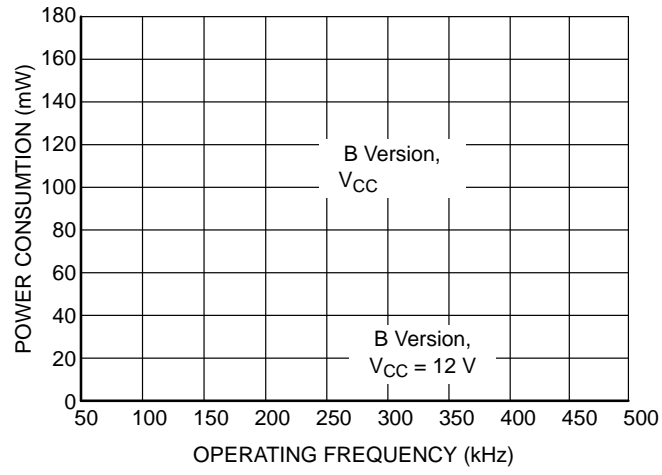


Figure 67. Equivalent Schematic of Gate Drive Circuitry

$$P_{\text{DRV_IC}} = \frac{1}{2} \cdot C_{\text{g_ZVS}} \cdot V_{\text{clamp}}^2 \cdot f_{\text{SW}} \cdot \left(\frac{R_{\text{drv_low_eq}}}{R_{\text{drv_low_eq}} + R_{\text{g_ext}} + R_{\text{g_int}}} \right) + C_{\text{g_ZVS}} \cdot V_{\text{clamp}} \cdot f_{\text{SW}} \cdot (V_{\text{CC}} - V_{\text{clamp}}) \quad (\text{eq. 7})$$

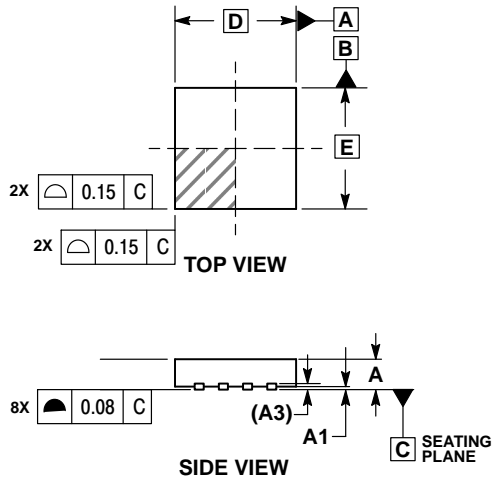
$$+ \frac{1}{2} \cdot C_{\text{g_ZVS}} \cdot V_{\text{clamp}}^2 \cdot$$

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DFN8, 4x4
CASE 488AF
ISSUE C

DATE 15 JAN 2009

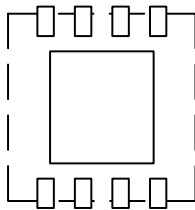


NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION *b* APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS.

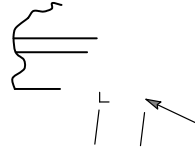
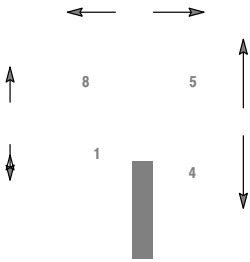
MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
<i>b</i>	0.25	0.35
D	4.00	BSC
D2	1.91	2.21
E	4.00	BSC
E2	2.09	2.39
<i>e</i>	0.80	BSC
K	0.20	---
L	0.30	0.50

BOTTOM VIEW



SOIC 8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



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PLANE



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