**MAXIMUM RATINGS**

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | IC Supply Voltage | | |

## TYPICAL CHARACTERISTICS

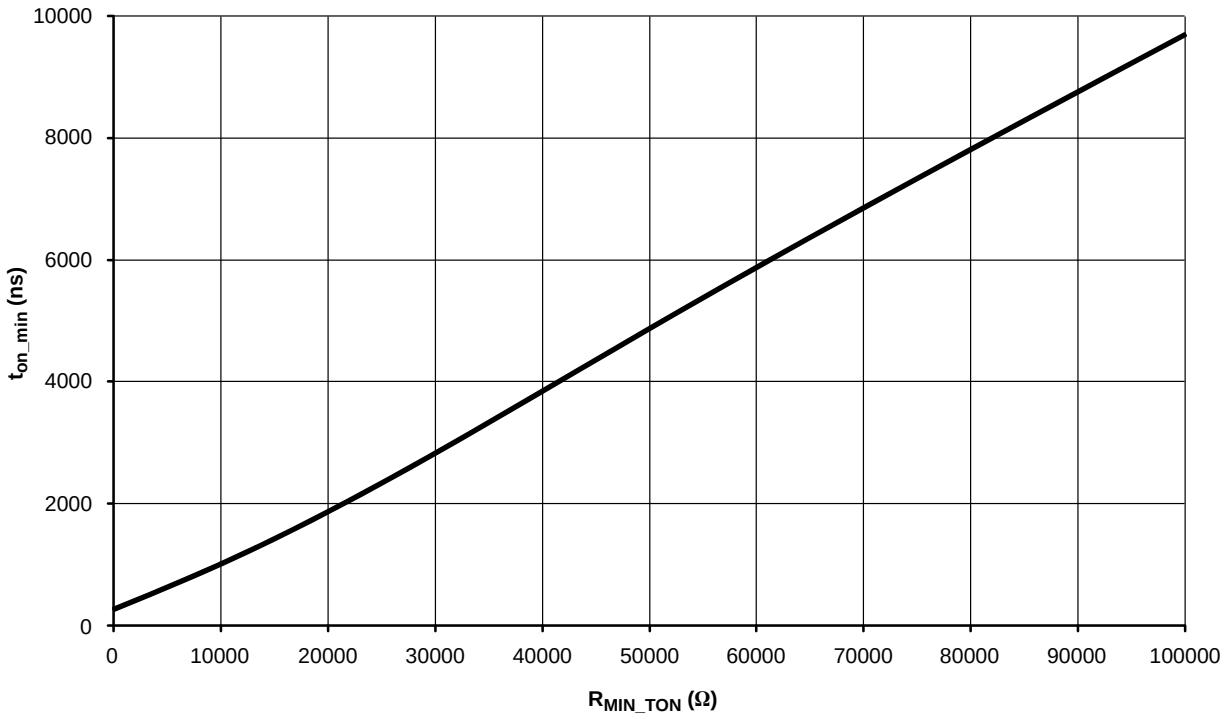



**Figure 4. $t_{on\ min}$ on $R_{MIN\ TON}$ Dependency**

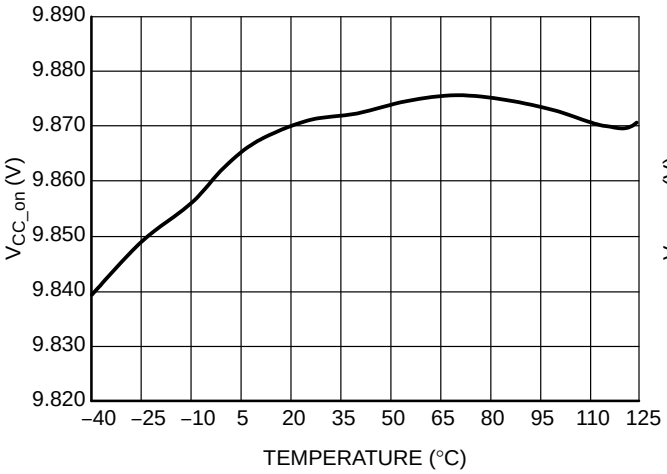



**Figure 5. VCC Startup Voltage**

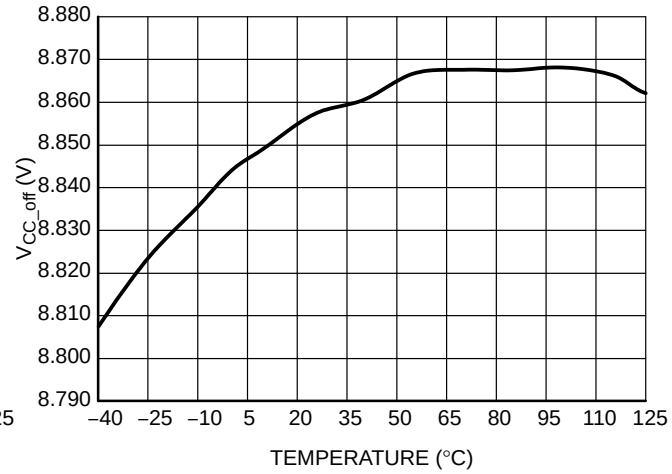



**Figure 6. VCC Turn-off Voltage**

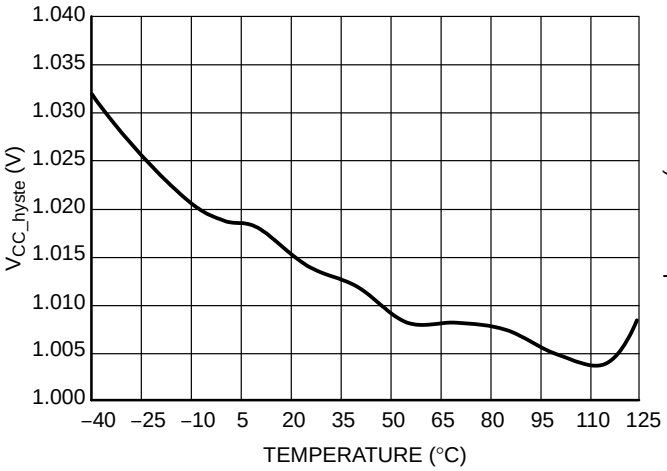



**Figure 7. VCC Hysteresis**

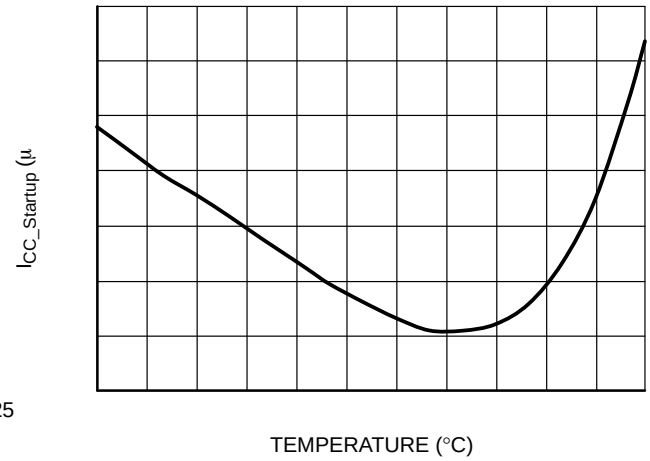
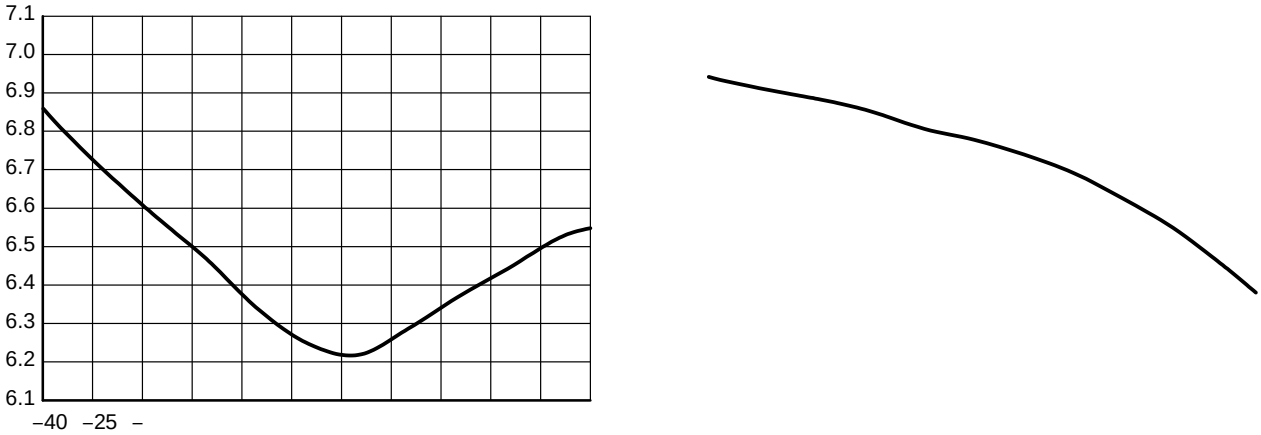



**Figure 8. Startup Current**


7.1
7.0
6.9
6.8
6.7
6.6
6.5
6.4
6.3
6.2
6.1
−40
−25
–

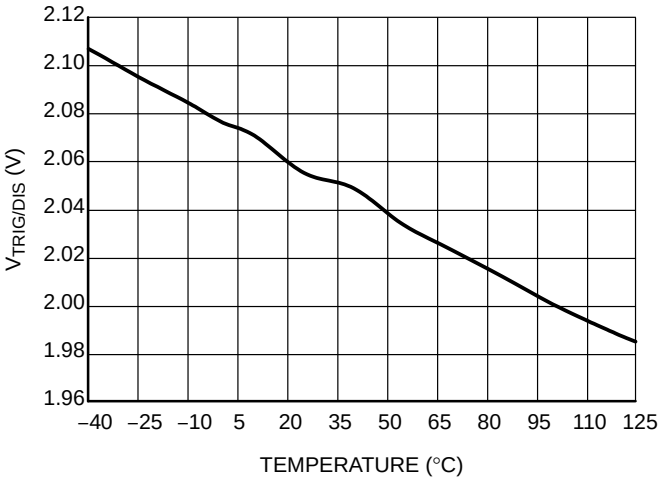



**Figure 23. Trigger Input Threshold Voltage**

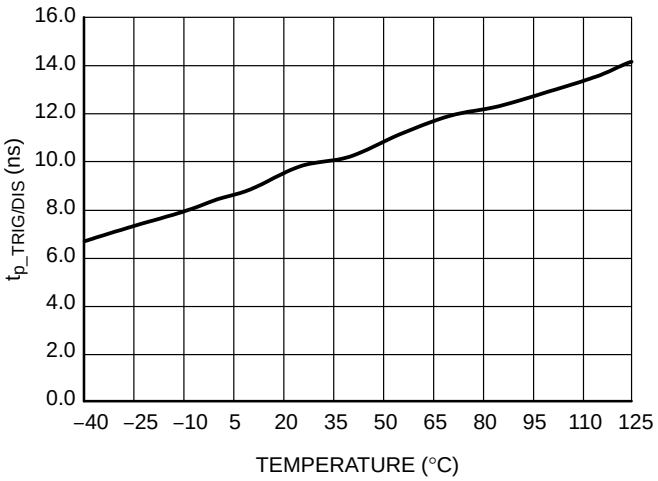



**Figure 24. Propagation Delay from Trigger Input to DRV Turn-off**

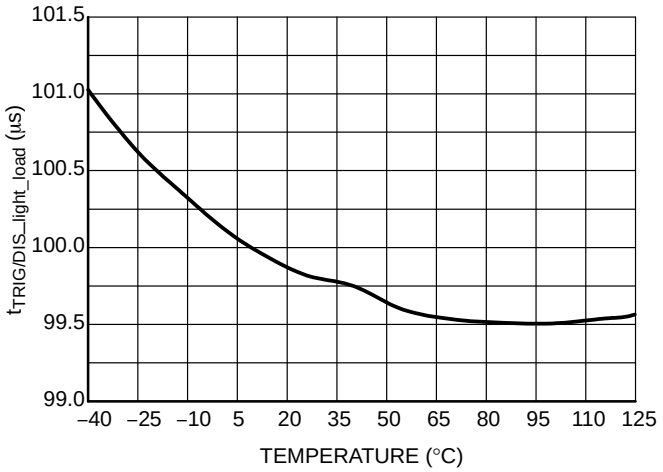
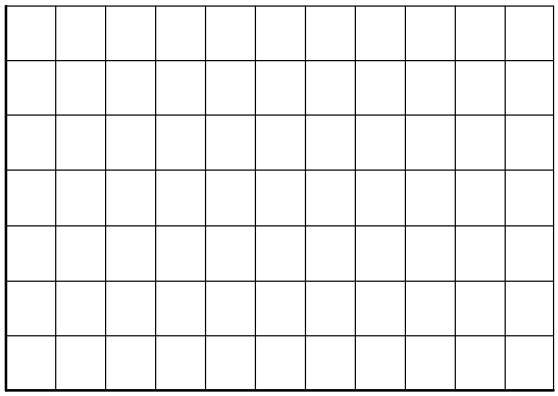



**Figure 25. Light Load Transition Timer Duration**



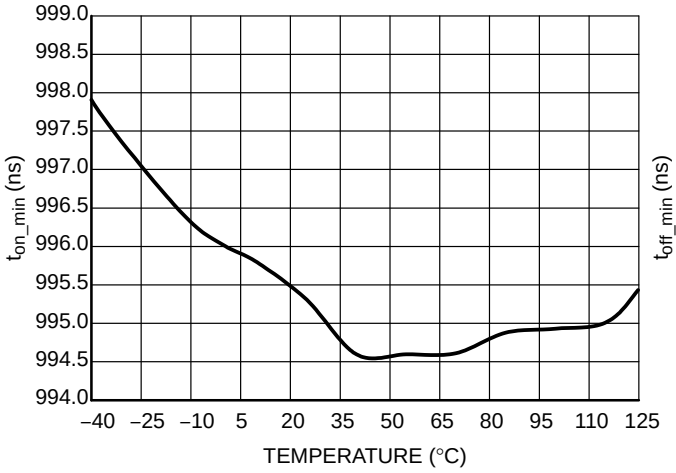



**Figure 29. Minimum On Time @ $R_{MIN\_TON}$ = 10 kΩ**

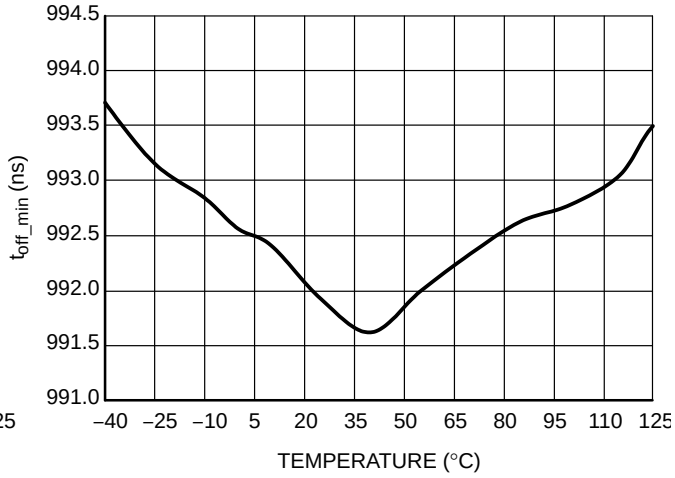



**Figure 30. Minimum Off Time @ $R_{MIN\_TOFF}$ = 10 kΩ**

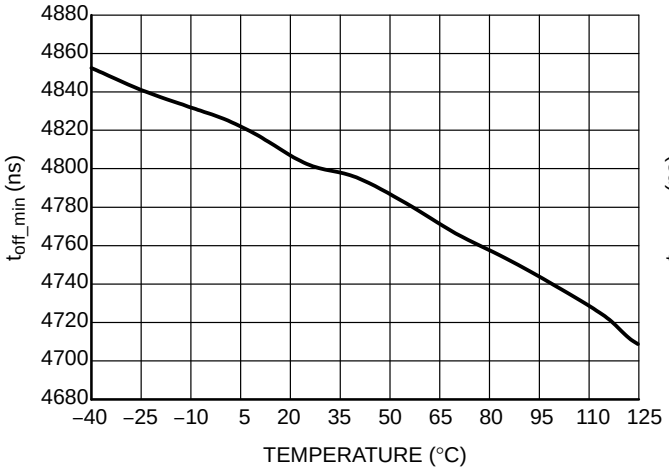



**Figure 31. Minimum Off Time @ $R_{MIN\_TOFF}$ = 50 kΩ**

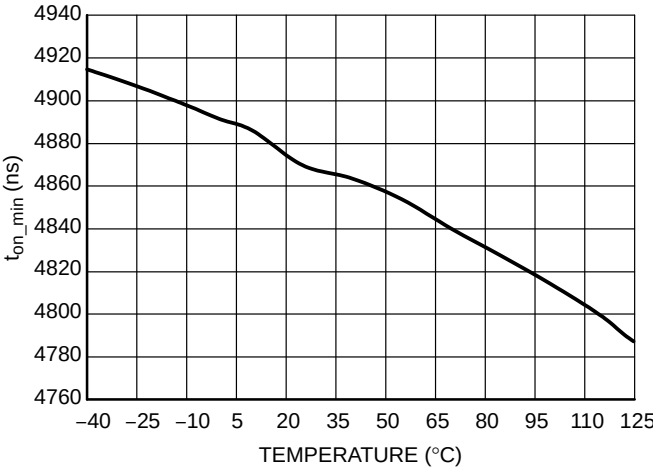
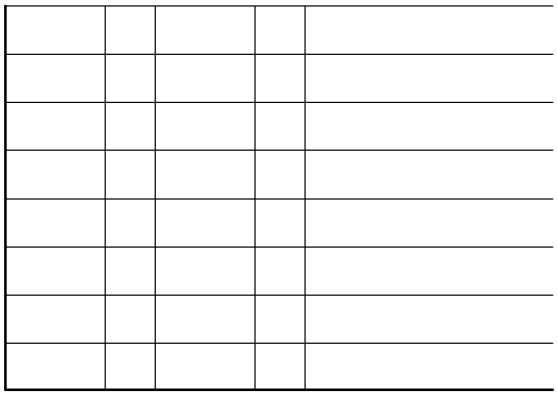
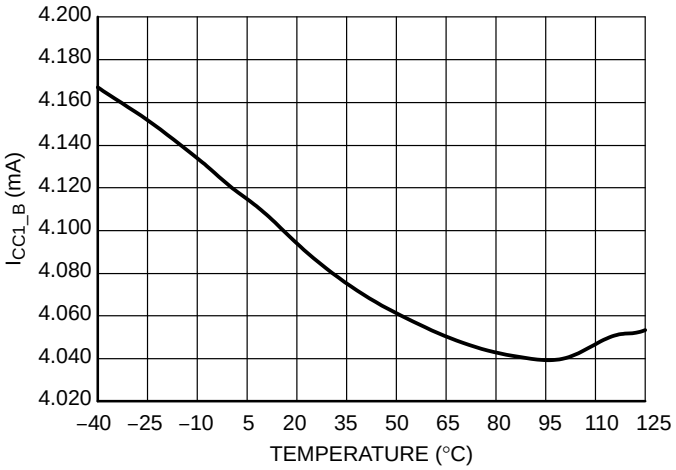



**Figure 32. Minimum On Time @ $R_{MIN\_TON}$ = 50 kΩ**





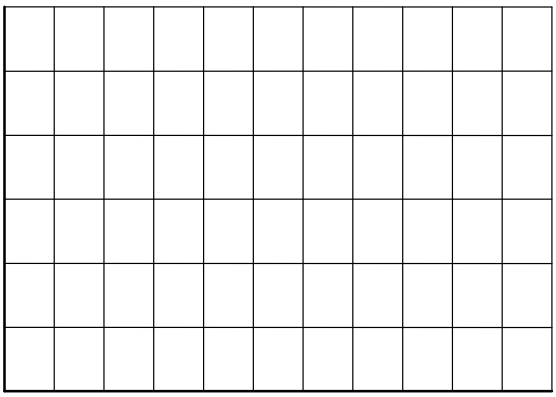



**Figure 35. Internal IC Consumption (B version, $C_{DRV}$ = 0 nF, $f_{SW}$ = 500 kHz, $t_{on\_min}$ = 500 ns, $t_{off\_min}$ = 620 ns)**

## APPLICATION INFORMATION

### General Description

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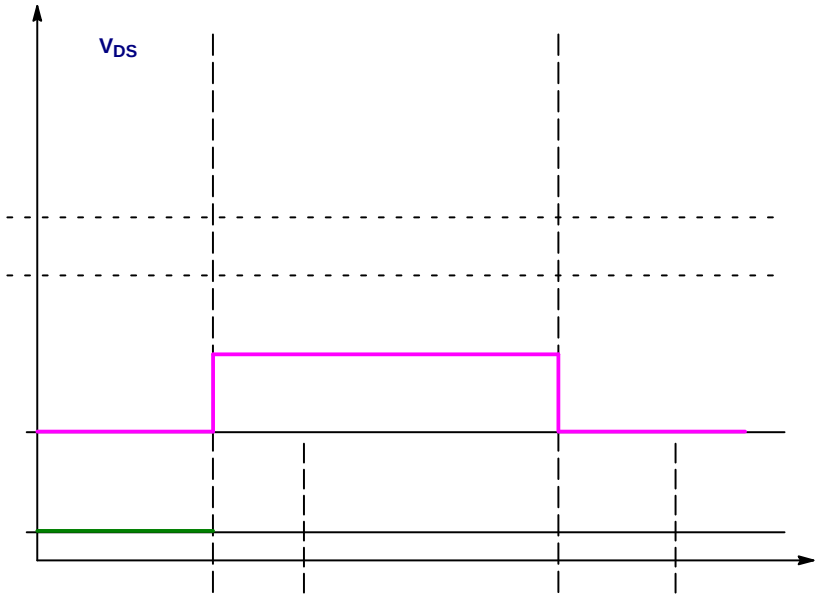


**Figure 41. ZCD Comparators Thresholds and Blanking Periods Timing**

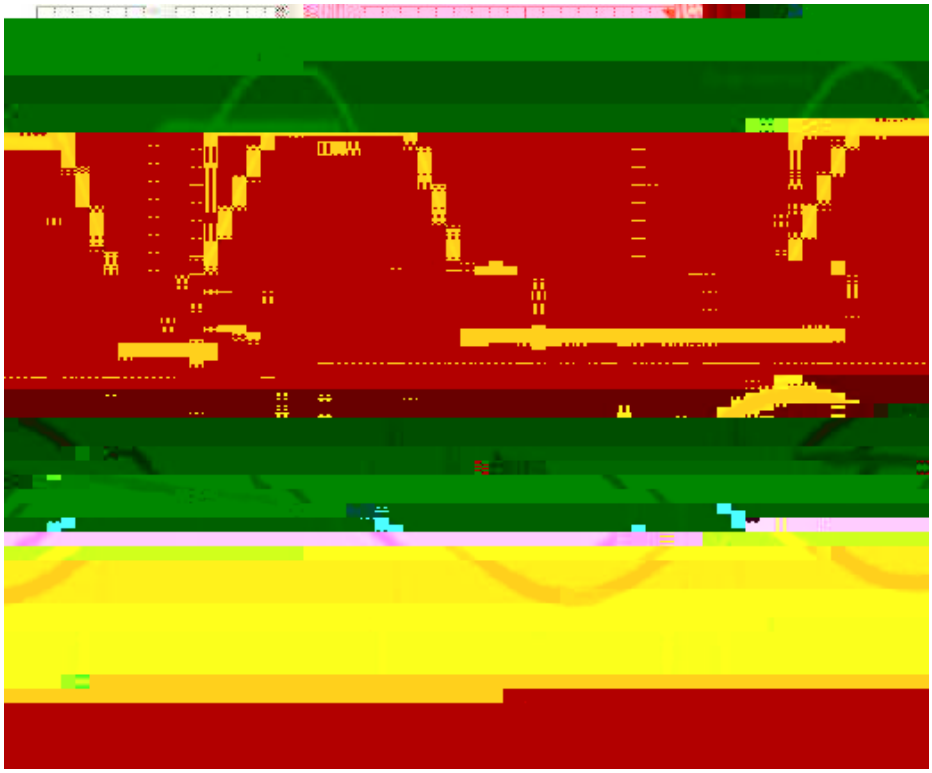

**Figure 42. Waveforms from SR System Using MOSFET in TO−220 Package Without Parasitic Inductance**

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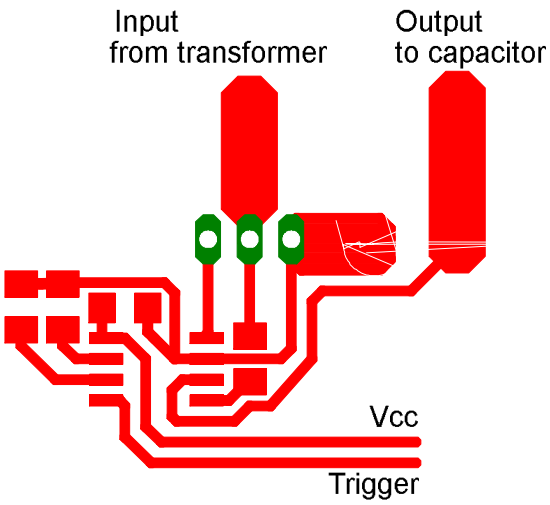
**Figure 44. Waveforms SR System Using MOSFET in TO−220 Package with Parasitic Inductance Compensation – SR MOSFET Channel Conduction Time is Optimized**

–

Ω


Input
from transformer
Output
to capacitor
Vcc
Trigger

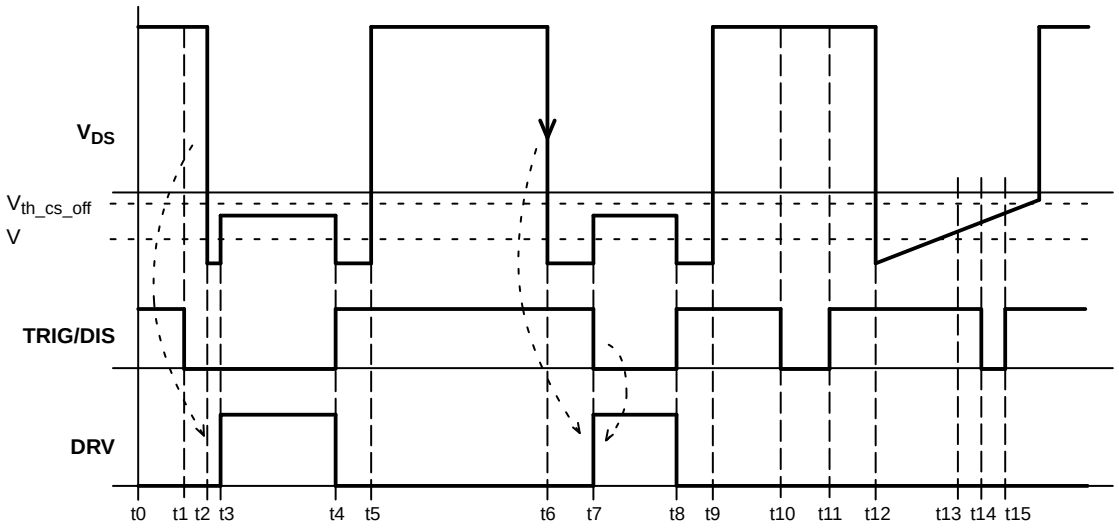



**Figure 48. DRV Turn ON Events**

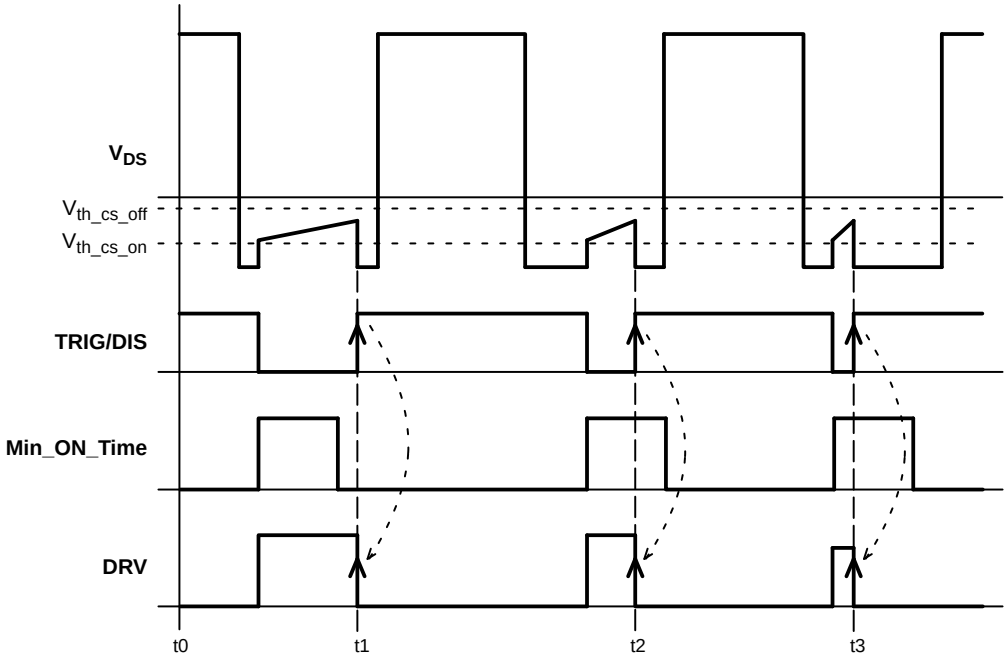



**Figure 51. Driver Turn-OFF Events Based on the TRIG/DIS Input**

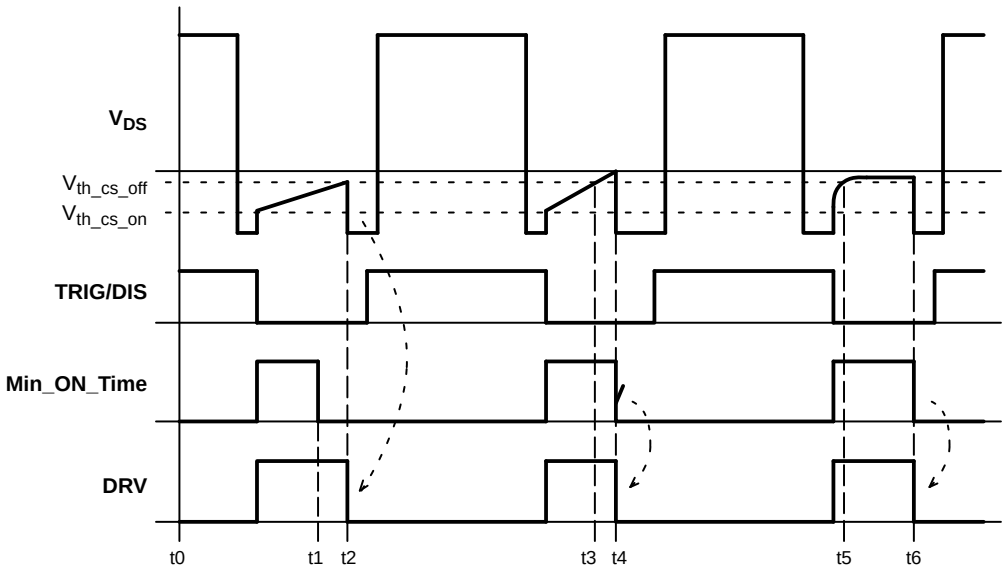



**Figure 52. Driver OFF Sequence Chart 2**

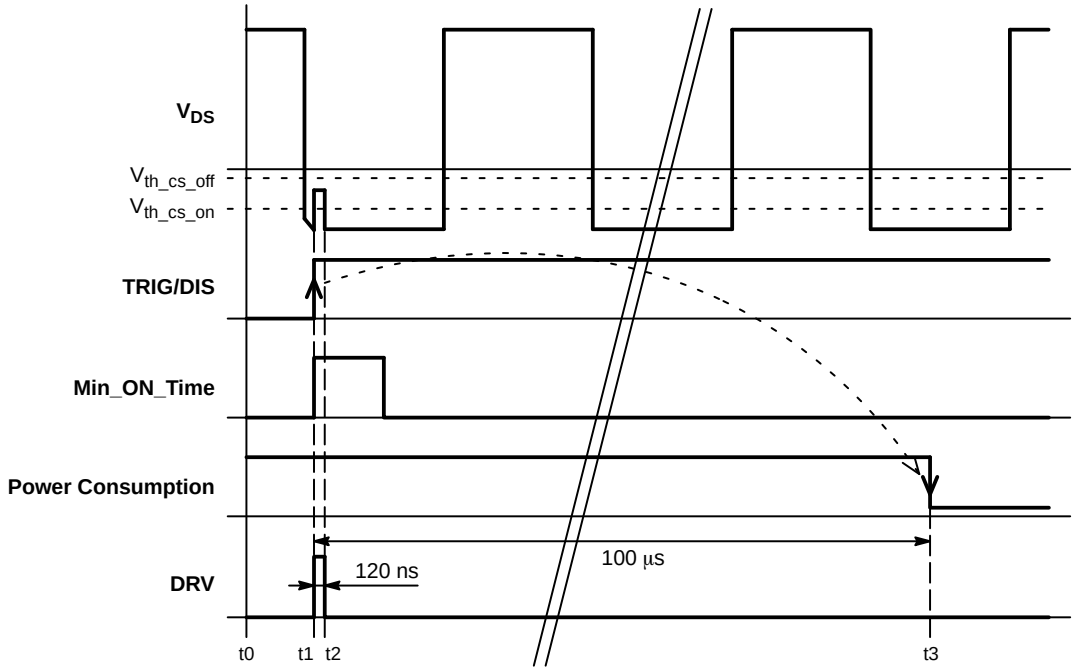



**Figure 55. TRIG/DIS from LOW to HIGH Sequence 2**

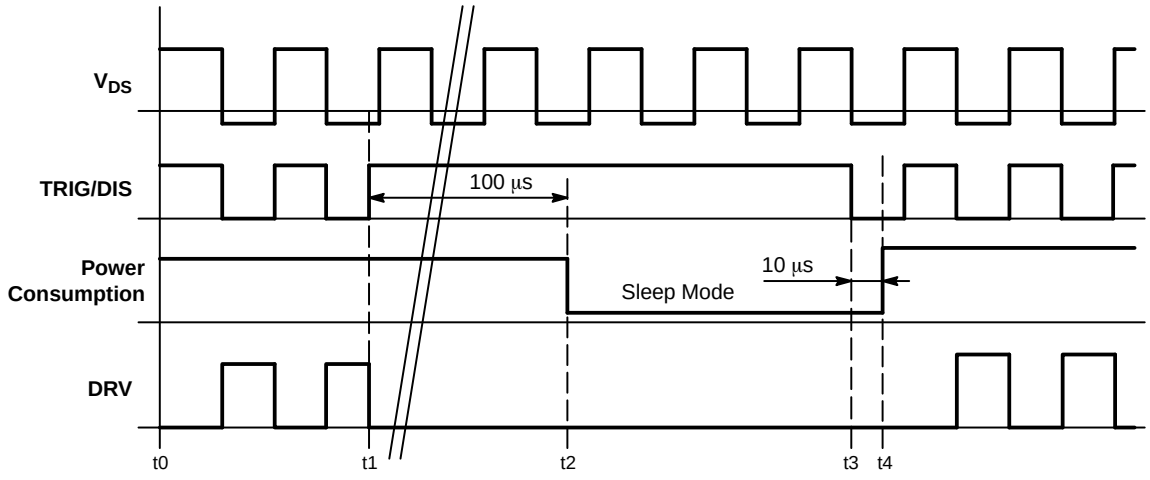



**Figure 56. Sleep Mode Sequence**

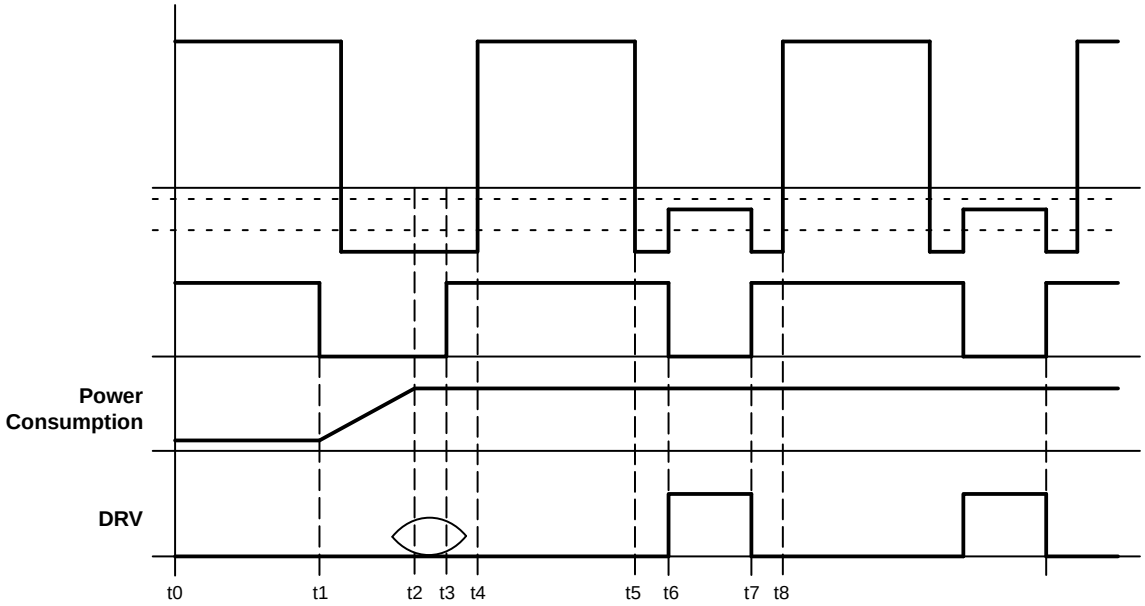



**Figure 57. Waking-up Sequence**

**Figure 58. Wake-up Time Sequence**

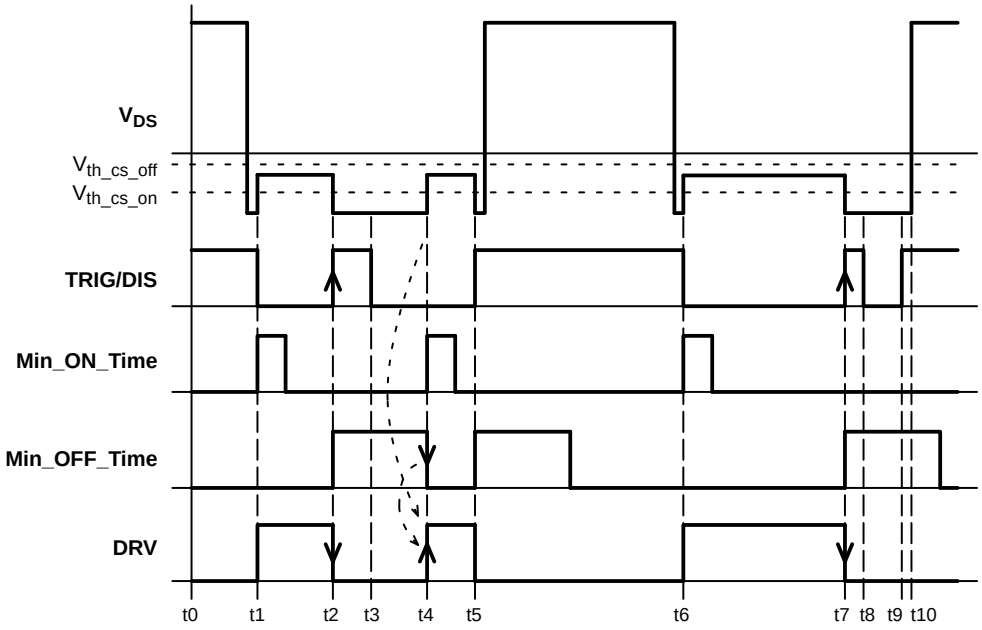



**Figure 59. IC Behavior when Multiple Trigger Pulses Appear on TRIG/DIS Input**

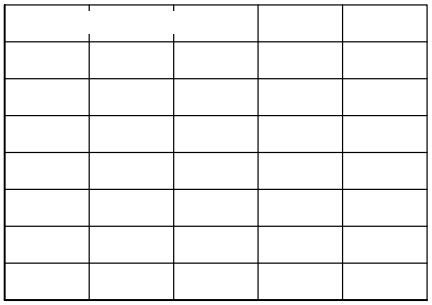


**Figure 66. Typical MOSFET Capacitance Dependency on $V_{DS}$ and $V_{GS}$ Voltage**

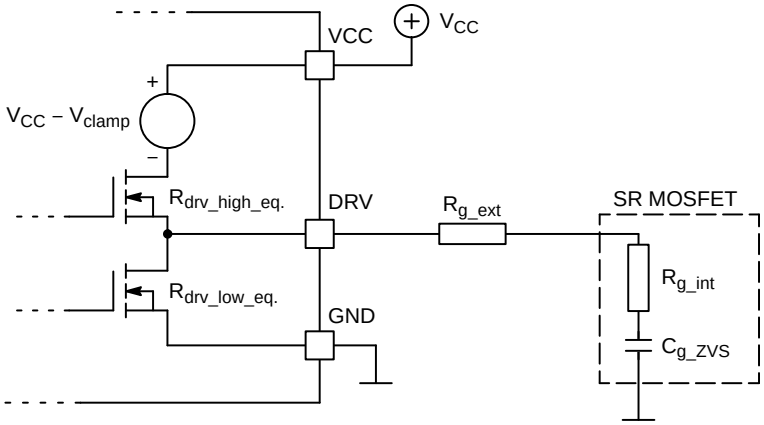
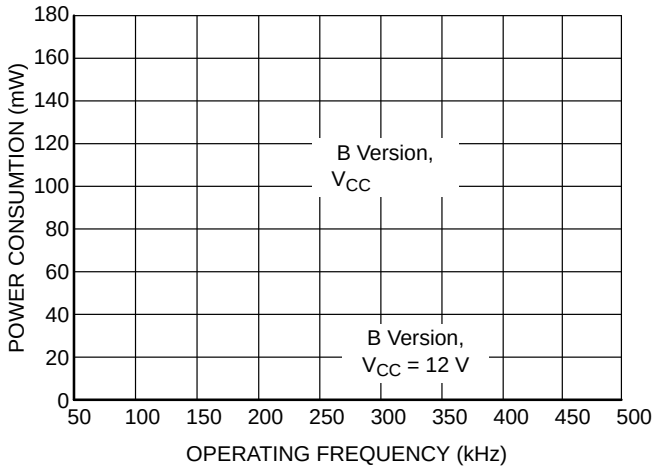



**Figure 67. Equivalent Schematic of Gate Drive Circuitry**

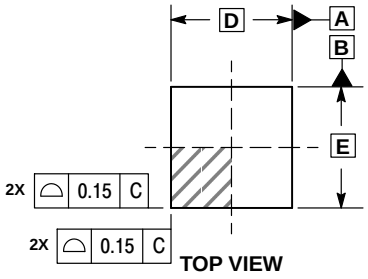
$$P_{DRV\_IC} = \frac{1}{2} \cdot C_{g\_ZVS} \cdot V_{clamp}{}^{2} \cdot f_{SW} \cdot \left( \frac{R_{drv\_low\_eq}}{R_{drv\_low\_eq} + R_{g\_ext} + R_{g\_int}} \right) + C_{g\_ZVS} \cdot V_{clamp} \cdot f_{SW} \cdot \left( V_{CC} - V_{clamp} \right) \quad \text{(eq. 7)}$$

$$+ \frac{1}{2} \cdot C_{g\_ZVS} \cdot V_{clamp}{}^{2} \cdot$$

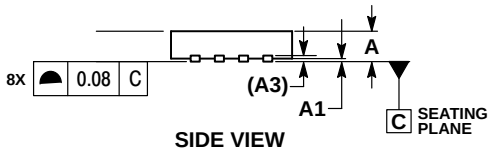

180
160
140
120
100
80
60
40
20
0
POWER CONSUMTION (mW)
B Version,
VCC
B Version,
VCC = 12 V
50
100
150
200
250
300
350
400
450
500
OPERATING FREQUENCY (kHz)

**DFN8, 4x4**
CASE 488AF
ISSUE C

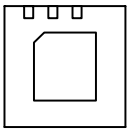
DATE 15 JAN 2009



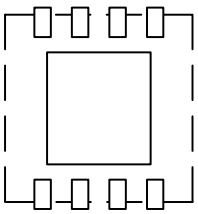

**TOP VIEW**




**SIDE VIEW**



**BOTTOM VIEW**

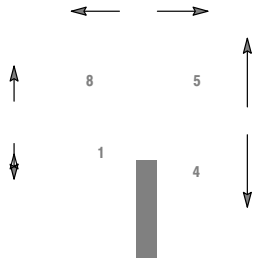


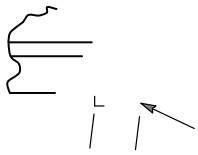
NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| **DIM** | **MIN** | **MAX** |
| **A** | 0.80 | 1.00 |
| **A1** | 0.00 | 0.05 |
| **A3** | 0.20 REF | |
| **b** | 0.25 | 0.35 |
| **D** | 4.00 BSC | |
| **D2** | 1.91 | 2.21 |
| **E** | 4.00 BSC | |
| **E2** | 2.09 | 2.39 |
| **e** | 0.80 BSC | |
| **K** | 0.20 | --- |
| **L** | 0.30 | 0.50 |

**SOIC 8 NB**
CASE 751−07
ISSUE AK

DATE 16 FEB 2011



SEATING
PLANE