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#### MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V <sub>CC</sub>	IC Supply Voltage		

#### **TYPICAL CHARACTERISTICS**

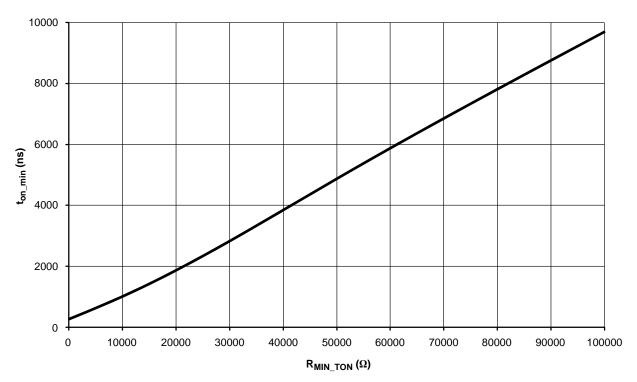
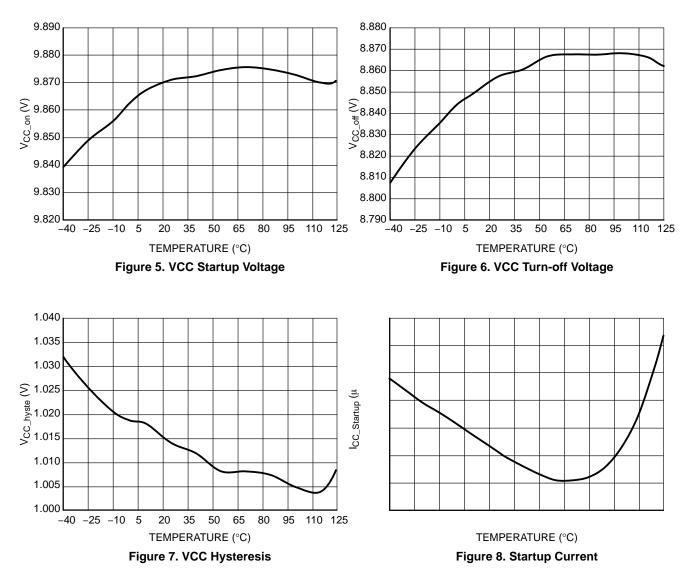


Figure 4.  $t_{\text{on}\ \text{min}}$  on  $R_{\text{MIN}\ \text{TON}}$  Dependency





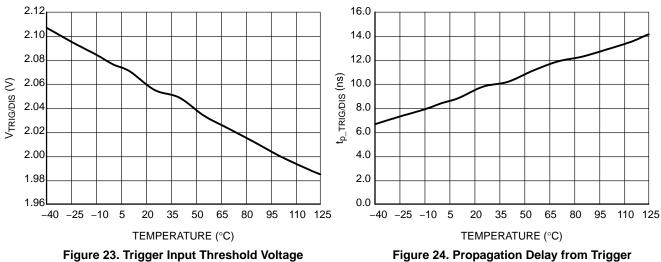
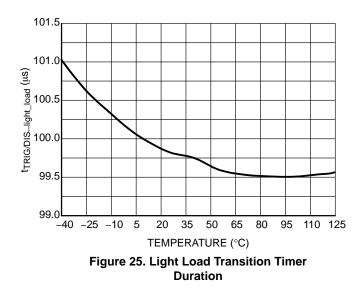


Figure 24. Propagation Delay from Trigger Input to DRV Turn-off



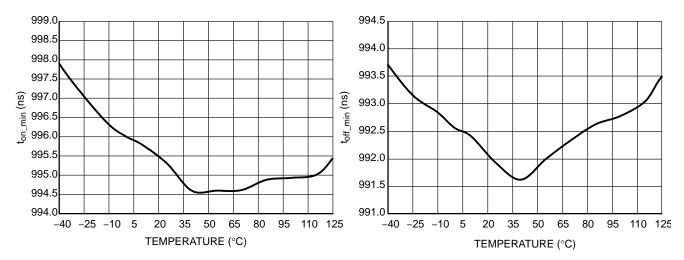


Figure 29. Minimum On Time @  ${\sf R}_{\rm MIN\_TON}$  = 10  $k\Omega$ 



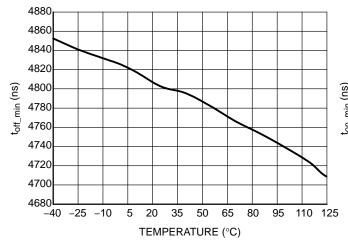
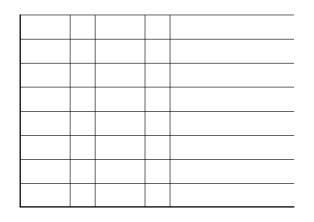


Figure 31. Minimum Off Time @  $R_{MIN_{TOFF}} = 50 \text{ k}\Omega$ 



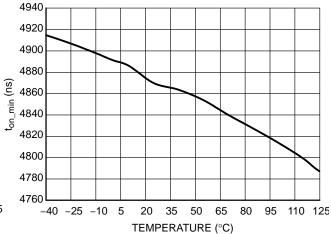


Figure 32. Minimum On Time @  $R_{MIN_{TON}} = 50 \text{ k}\Omega$ 

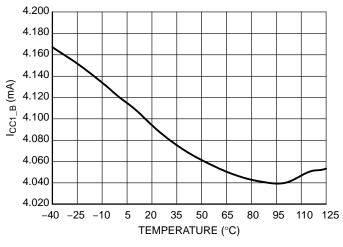


Figure 35. Internal IC Consumption (B version,  $C_{DRV} = 0 \text{ nF}, f_{SW} = 500 \text{ kHz},$  $t_{on\_min} = 500 \text{ ns}, t_{off\_min} = 620 \text{ ns})$ 

#### **APPLICATION INFORMATION**

#### **General Description**

The NCP4304A/B is designed to operate either as a standalone IC or as a companion IC to a primary side controller to help achieve efficient synchronous rectification in switch mode power supplies. This controller features a high current gate driver along with high-speed logic circuitry to provide appropriately timed drive signals to a synchronous rectification MOSFET. With its novel architecture, the NCP4304A/B has enough versatility to keep the synchronous rectification efficient under any operating mode.

The NCP4304A/B works from an available bias supply with voltage range from 10.4 V to 28 V (typical). The wide  $V_{CC}$ 

When the voltage on the secondary winding of the SMPS reverses, the body diode of M1 starts to conduct current and the voltage of M1's drain drops approximately to -1 V. The CS pin sources current of 100  $\mu$ A that creates a voltage drop on the RSHIFT\_CS resistor. Once the voltage on the CS pin is lower than V<sub>th\_CS\_on</sub> threshold, M1 is turned on. Because of parasitic impedances, significant ringing can occur in the application. To overcome sudden turn-off due to mentioned ringing, the minimum conduction time of the SR MOSFET is activated. Minimum conduction time can be adjusted using R<sub>MIN\_TON</sub> resistor.

The SR MOSFET is turned-off as soon as the voltage on the CS pin is higher than  $V_{th_{CS}off}$ . For the same ringing reason, a minimum off time timer is asserted once the turn-off is detected. The minimum off time can be externally adjusted using  $R_{MIN_{TOFF}}$  resistor. MOSFET M1 conducts when the secondary current decreases, therefore the turn-off time depends on its  $R_{DS(on)}$ . The 0 mV threshold provides an optimum switching period usage while keeping enough time margin for the gate turn off. The RSHIFT\_CS resistor provides the designer with the possibility to modify (increase) the actual turn-off current threshold.

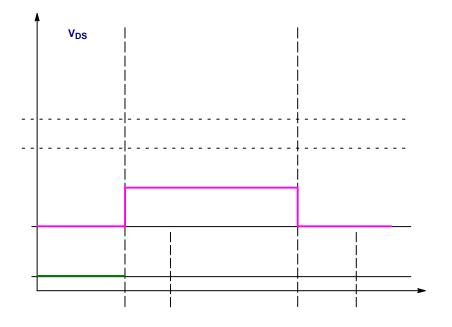


Figure 41. ZCD Comparators Thresholds and Blanking Periods Timing

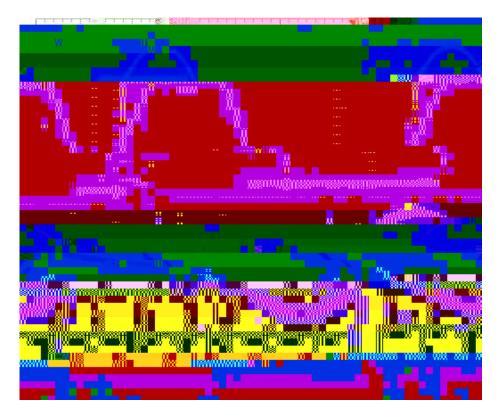


Figure 42. Waveforms from SR System Using MOSFET in TO-220 Package Without Parasitic Inductance

be as low as possible compared to the SR MOSFET channel and leads resistance otherwise compensation is not efficient. Typical value of compensation inductance for a TO-220 package is 7 nH. Waveforms from the application with compensated SR system can be seen in Figure 44. One can see the conduction time has been significantly increased and turn-off current reduced.

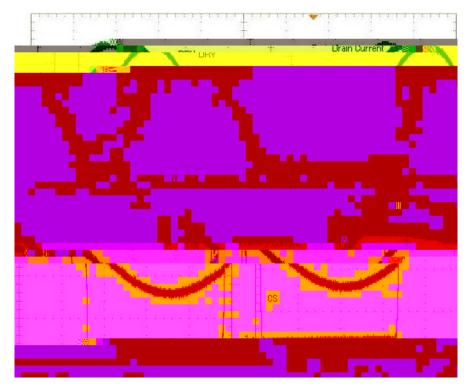


Figure 44. Waveforms SR System Using MOSFET in TO-220 Package with Parasitic Inductance Compensation – SR MOSFET Channel Conduction Time is Optimized

Note that using the compensation system is only beneficial in applications that are using a low  $R_{DS(on)}$  MOSFET in non-SMT package. Using the compensation method allows for optimized efficiency with a standard TO–220 package that in turn results in reduced costs, as the SMT MOSFETs usually require reflow soldering process and more expensive PCB.

From the above paragraphs and parameter tables it is evident that turn-off threshold precision is quite critical. If we consider a SR MOSFET with  $R_{DS(on)}$  of 1 m $\Omega$ , the 1 mV error voltage on the CS pin results in a 1 A turn-off current threshold difference. Thus the PCB layout is very critical when

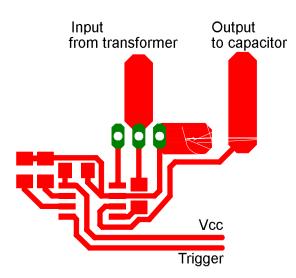
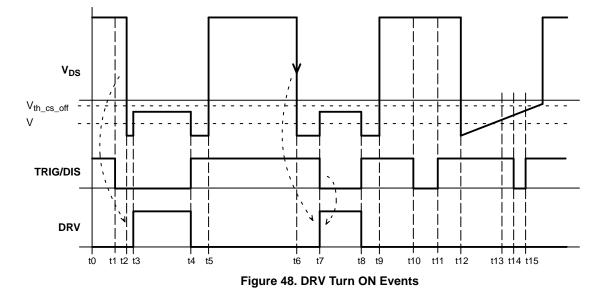


Figure 48 depicts driver turn-ON events. Turn-ON of the SR MOSFET is possible if CS ( $V_{DS}$ ) signal falls under  $V_{th\_cs\_on}$  threshold and TRIG/DIS is pulled LOW (t1 to t3 time interval).

When the CS ( $V_{DS}$ ) reached the  $V_{th\_cs\_on}$  threshold and TRIG/DIS is pulled HIGH the driver stays LOW (t6, t7 time markers) if the TRIG/DIS is HIGH. If the TRIG/DIS is

pulled LOW and CS (V<sub>DS</sub>) is still under V<sub>th\_cs\_on</sub> threshold then the DRV is turned-ON (t7 marker).

Time markers t14 and t15 in Figure 48 demonstrate situation when CS (V<sub>DS</sub>) is above V<sub>th\_cs\_on</sub> threshold and TRIG/DIS is pulled down. In this case the driver stays LOW (t12 to t15 marker).



Advantage of the trigger blanking time during DRV turn-ON event is evident from Figure 50. Rising edge of the

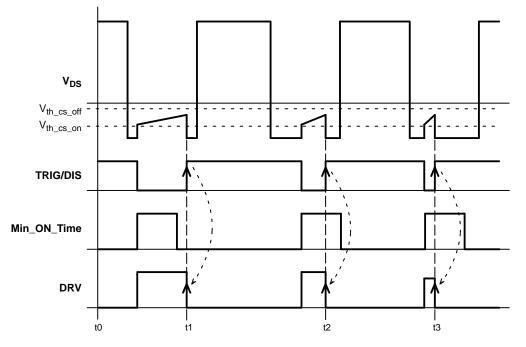


Figure 51. Driver Turn-OFF Events Based on the TRIG/DIS Input

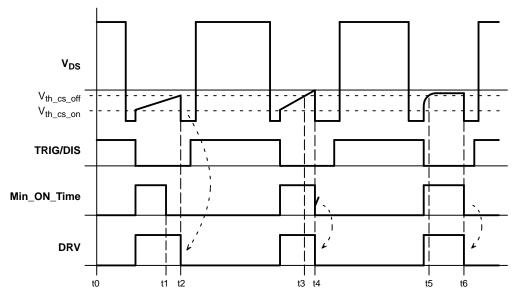


Figure 52. Driver OFF Sequence Chart 2

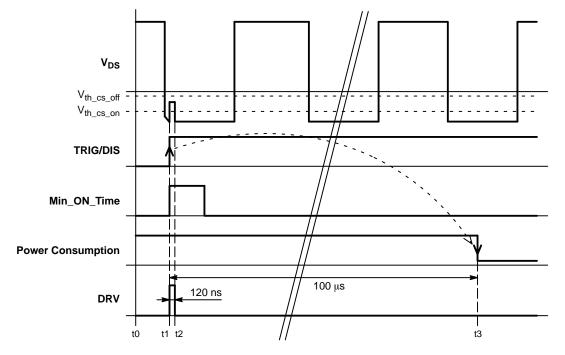
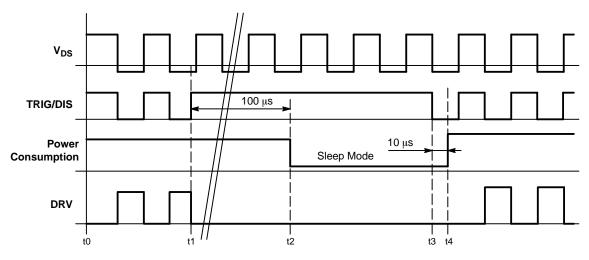


Figure 55. TRIG/DIS from LOW to HIGH Sequence 2





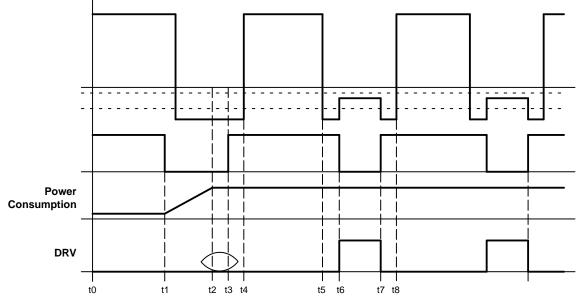




Figure 58. Wake-up Time Sequence

Figure 59 shows IC behavior in case the trigger signal features two pulses during one cycle of the  $V_{DS}$  (CS) signal. TRIG/DIS enables driver at time t1 and DRV turns ON because the  $V_{DS}$  voltage is under  $V_{th\_CS\_on}$  threshold voltage. The trigger signal and consequently DRV output fall down in time t2. The minimum OFF time generator is triggered in time t2. TRIG/DIS drops down to LOW level in time t3 but there is still minimum OFF time sequence present so the DRV output stays low. When the minimum OFF time

sequence elapses in time t4 the DRV is turned ON. In time t5 Trigger signal rises up and terminates this cycle of the CS signal in time t5. Next cycle starts in time t6. Trigger enables DRV and V<sub>DS</sub> is under V<sub>th\_cs\_on</sub> threshold voltage so DRV turns ON in time t6. TRIG/DIS signal rises up to HIGH level in time t7, consequently DRV turns OFF and this starts minimum OFF time generator. Because minimum OFF time period is longer then the rest of time to the end of cycle of V<sub>DS</sub> – DRV is disabled.

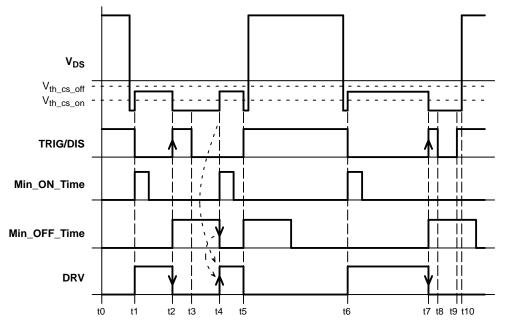


Figure 59. IC Behavior when Multiple Trigger Pulses Appear on TRIG/DIS Input

Note that the TRIG/DIS input is an ultrafast input that is sensitive even to very narrow voltage pulses. Thus it is wise to keep this input on a low impedance path and provide it with a clean triggering signal in the time this input is enabled by internal logic.

A typical application schematic of a CCM flyback converter with the NCP4304A/B driver can be seen in Figure 60. In this application the trigger signal is taken directly from the flyback controller driver output and transmitted to the secondary side by pulse transformer TR2. Because the TRIG/DIS input is edge sensitive, it is not necessary to transmit the entire primary driver pulse to the secondary. The coupling capacitor C5 is used to allow pulse transformer core reset and also to prepare a needle pulse (a pulse with width lower than 100 ns) to be transmitted to the NCP4304A/B TRIG/DIS input. The advantage of needle trigger pulse usage is that the required volt-second product of the pulse transformer is very low and that allows the designer to use very small and cheap magnetics. The trigger transformer can be for instance prepared on a small toroidal ferrite core with diameter of 8 mm. Proper safety insulation between primary and secondary sides can be easily assured by using triple insulated wire for one or even both windings.

The primary MOSFET gate voltage rising edge is delayed by external circuitry consisting of transistors Q1, Q2 and surrounding components. The primary MOSFET is thus turned-on with a slight delay so that the secondary controller turns-off the SR MOSFET by trigger signal prior to the primary switching. This method reduces the commutation losses and the SR MOSFET drain voltage spike, which results in improved efficiency.

It is also possible to use capacitive coupling (use additional capacitor with safety insulation) between the primary and secondary to transmit the trigger signal. We do not recommend this technique as the parasitic capacitive currents between primary and secondary may affect the trigger signal and thus overall system functionality.


Figure 66. Typical MOSFET Capacitance Dependency on  $V_{\text{DS}}$  and  $V_{\text{GS}}$  Voltage

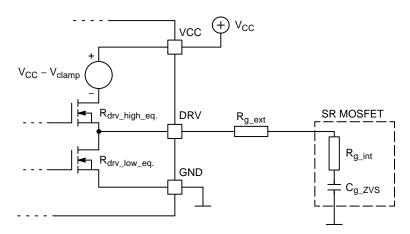
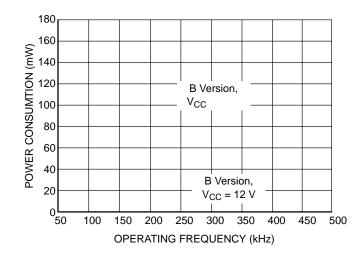


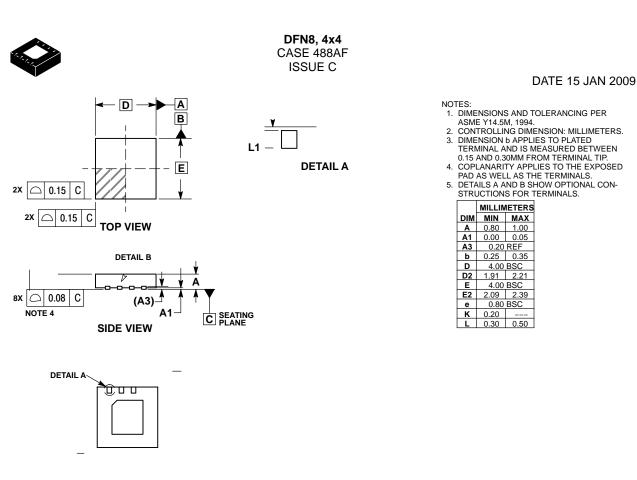
Figure 67. Equivalent Schematic of Gate Drive Circuitry

$$\begin{split} \mathsf{P}_{\mathsf{DRV\_IC}} &= \frac{1}{2} \cdot \mathsf{C}_{\mathsf{g\_ZVS}} \cdot \mathsf{V}_{\mathsf{clamp}} \, {}^{2} \cdot f_{\mathsf{SW}} \cdot \left( \frac{\mathsf{R}_{\mathsf{drv\_low\_eq}}}{\mathsf{R}_{\mathsf{drv\_low\_eq}} + \mathsf{R}_{\mathsf{g\_ext}} + \mathsf{R}_{\mathsf{g\_int}}} \right) + \mathsf{C}_{\mathsf{g\_ZVS}} \cdot \mathsf{V}_{\mathsf{clamp}} \cdot f_{\mathsf{SW}} \cdot \left( \mathsf{V}_{\mathsf{CC}} - \mathsf{V}_{\mathsf{clamp}} \right) \\ &+ \frac{1}{2} \cdot \mathsf{C}_{\mathsf{g\_ZVS}} \cdot \mathsf{V}_{\mathsf{clamp}} \, {}^{2} \cdot \end{split}$$

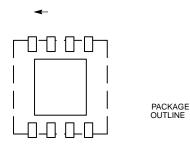
$$(eq. 7)$$



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#### BOTTOM VIEW



DIMENSIONS: MILLIMETERS

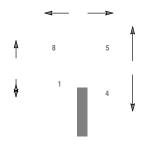
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SEATING PLANE



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