NCP4305

Secondar Side S nchrono s Rectification Dri er for High Efficienc SMPS Topologies

The NCP4305 is high performance driver tailored to control a synchronous rectification MOSFET in switch mode power supplies. Thanks to its high performance drivers and versatility, it can be used in various topologies such as DCM or CCM flyback, quasi resonant flyback, forward and half bridge resonant LLC.

The combination of externally adjustable minimum off-time and on-time blanking periods helps to fight the ringing induced by the PCB layout and other parasitic elements. A reliable and noise less operation of the SR system is insurt Efd lTD-. c-.0iwit2.318128 0 TD-.015 Tc-.2074 TwthrRh-2.6(e S4 lTe)14.hale S-3((synchrizinatiof S-5(eature(f)]TJ/

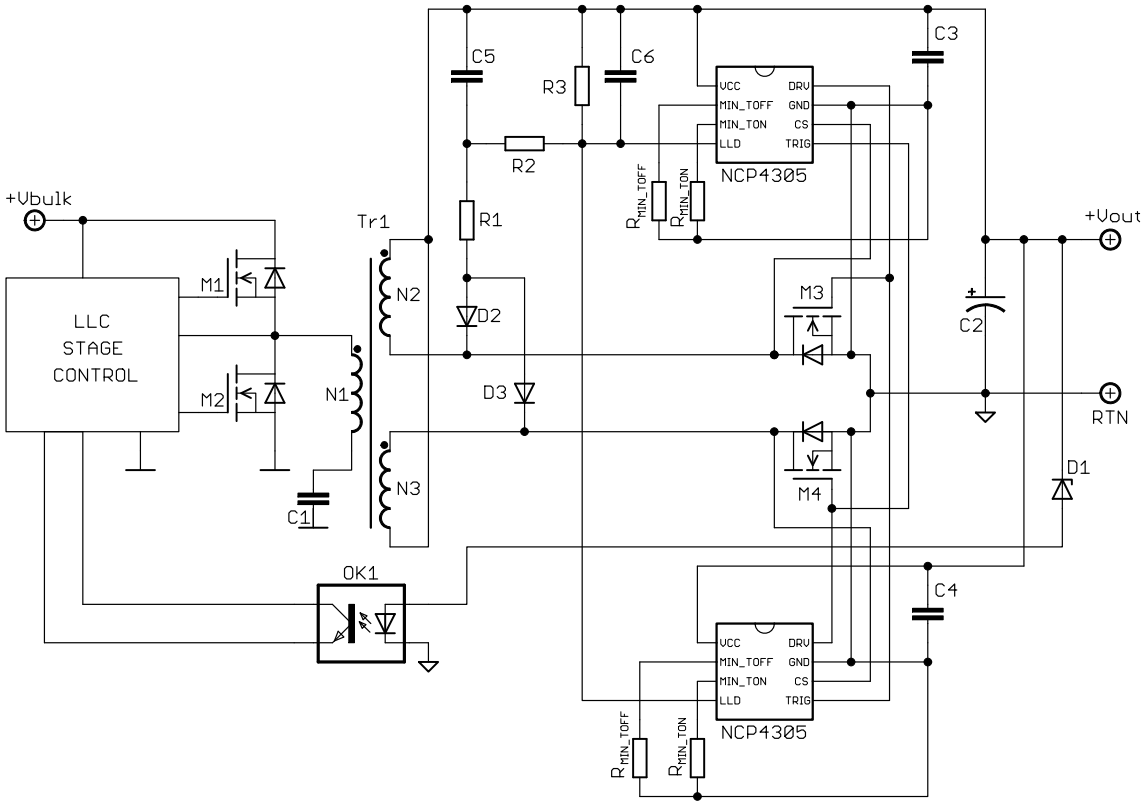


Figure 1. Typical Application Example − LLC Converter with Optional LLD and Trigger Utilization

TRIG

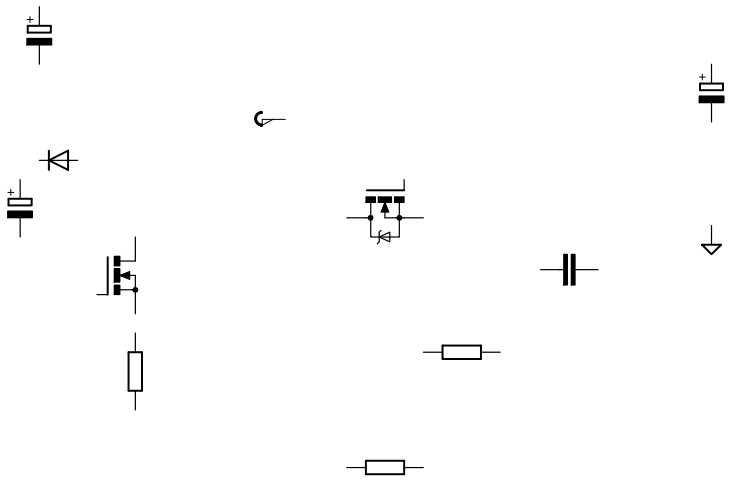


Figure 3. Typical Application Example − Primary Side Flyback Converter with optional LLD and Disabled TRIG

PIN FUNCTION DESCRIPTION

ver. A, B, C, D	ver. Q	Pin Name	Description
1	1	VCC	Supply voltage pin
2	2	MIN_TOFF	Adjust the minimum off time period by connecting resistor to ground.
3	3	MIN_TON	Adjust the minimum on time period by connecting resistor to ground.
4	4	LLD	This input modulates the driver clamp level and/or turns the driver off during light load conditions.
5	−	TRIG/DIS	Ultrafast turn−off input that can be used to turn off the SR MOSFET in CCM applications in order to improve efficiency. Activates disable mode if pulled−up for more than 100 μs.
6	6	CS	Current sense pin detects if the current flows through the SR MOSFET and/or its body

ELECTRICAL CHARACTERISTICS
$-40°C \le T_J \le 125°C$; V_{CC} = 12 V; C_{DRV} = 0 nF; R

TYPICAL CHARACTERISTICS

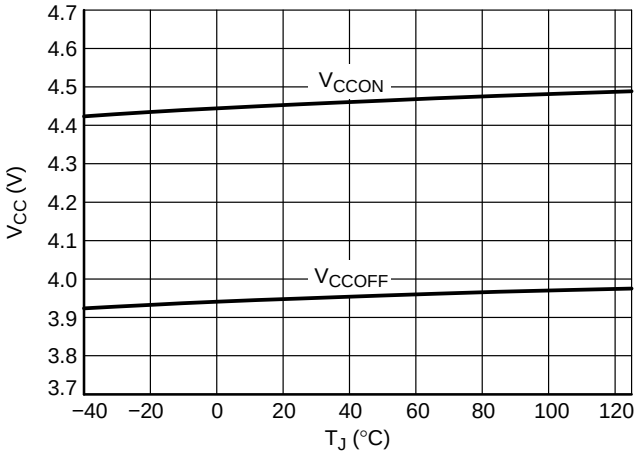


Figure 7. V_{CCON} and V_{CCOFF} Levels, ver. A, D, Q

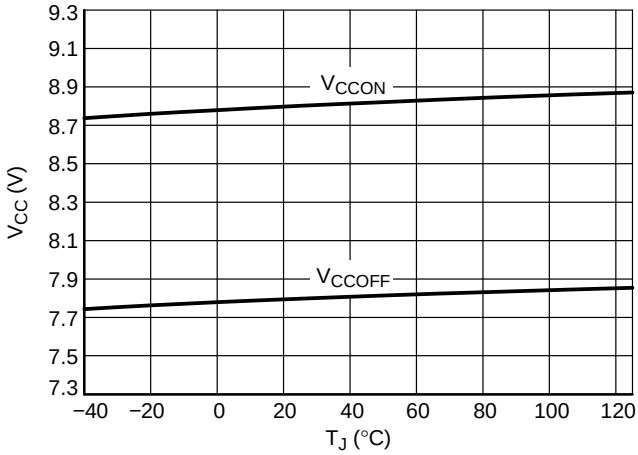


Figure 8. V_{CCON} and V_{CCOFF} Levels, ver. B, C

TYPICAL CHARACTERISTICS

Figure 9. Current Consumption, C_{DRV} = 0 nF, f_{CS} = 500 kHz, ver. D

Figure 10. Current Consumption, V_{CC} = V_{CCOFF}

TYPICAL CHARACTERISTICS

T_J

Figure 15. CS Current, V_{CS} = −20 mV

Figure 16. CS Current, V_{CC} = 12 V

TYPICAL CHARACTERISTICS

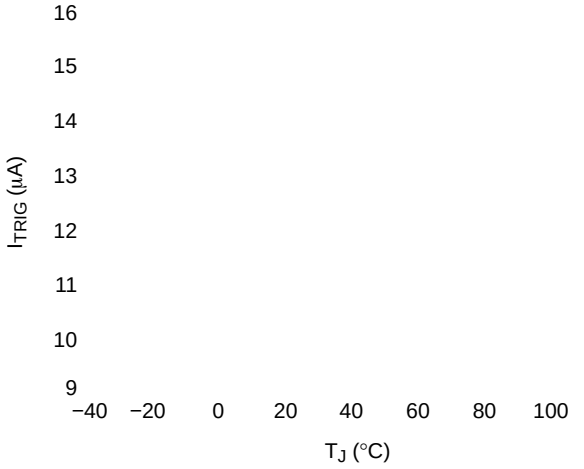


Figure 27. Trigger Pull Down Current

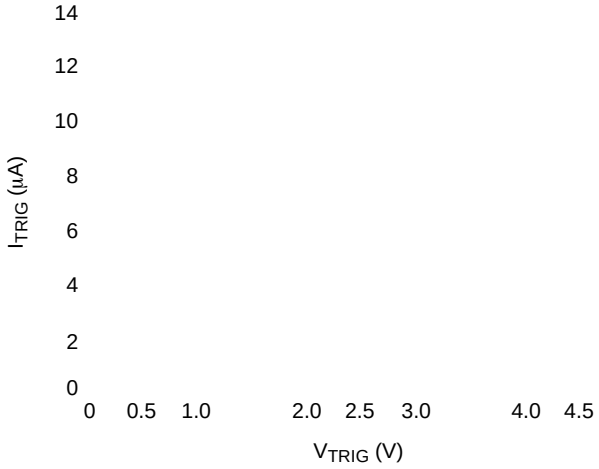


Figure 28. Trigger Pull Down Current, V_{CC} = 12 V

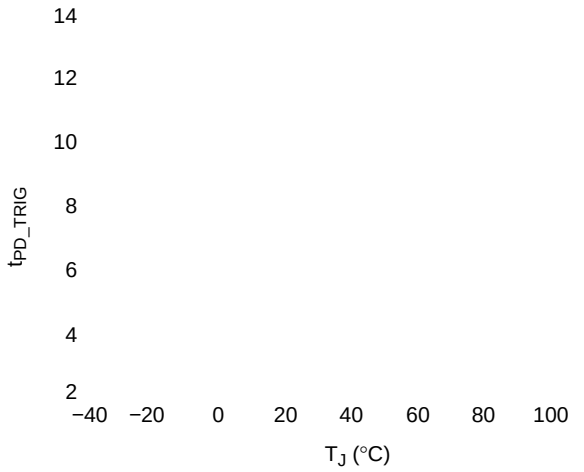


Figure 29. Propagation Delay from Trigger to Driver Output Off

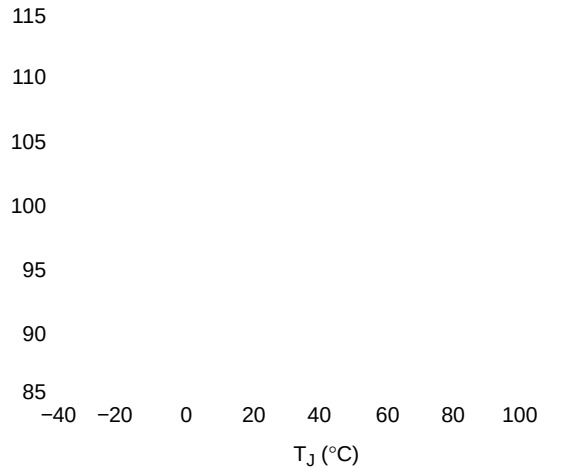


Figure 30. Delay to Disable Mode, V_{TRIG} = 5 V

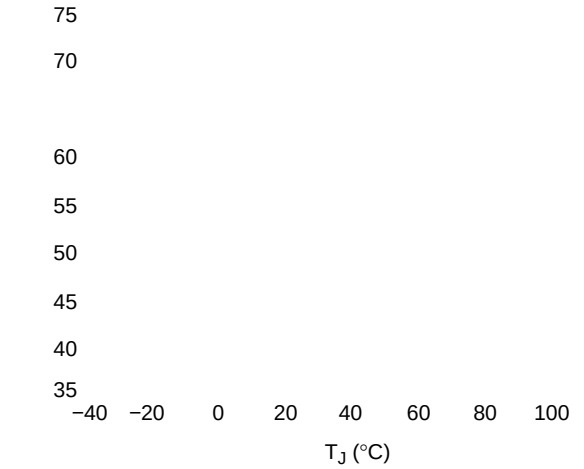


Figure 31. Minimum On−time R_{MIN_TON} = 0 Ω

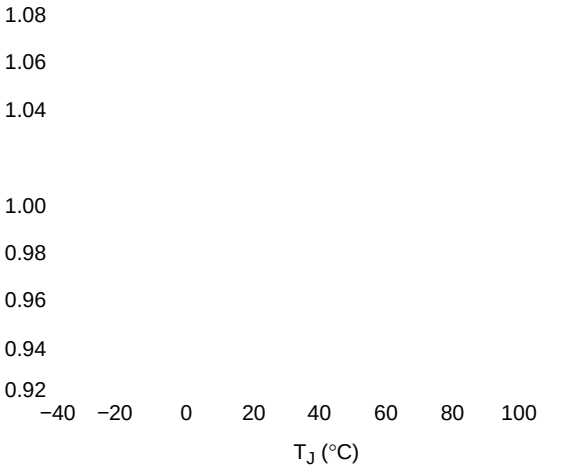


Figure 32. Minimum On−time R_{MIN_TON} = 10 kΩ

TYPICAL CHARACTERISTICS

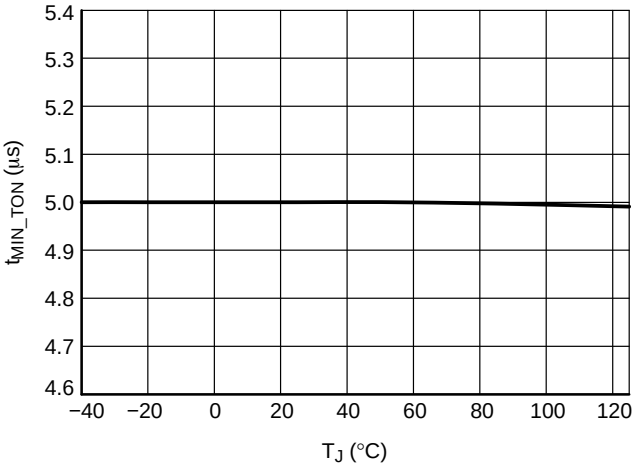


Figure 33. Minimum On−time R_{MIN_TON} = 50 kΩ

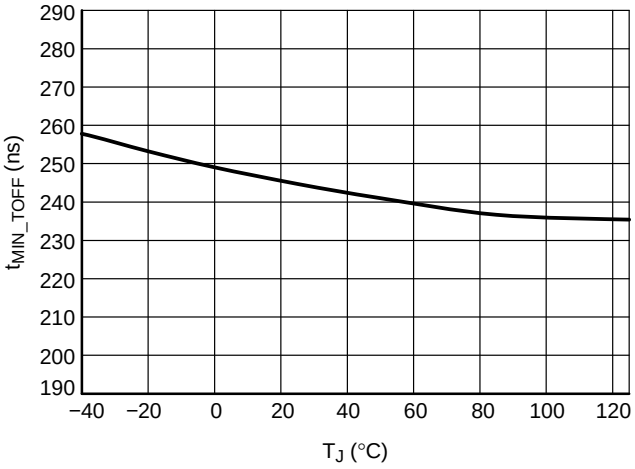


Figure 34. Minimum Off−time R_{MIN_TOFF} = 0 Ω

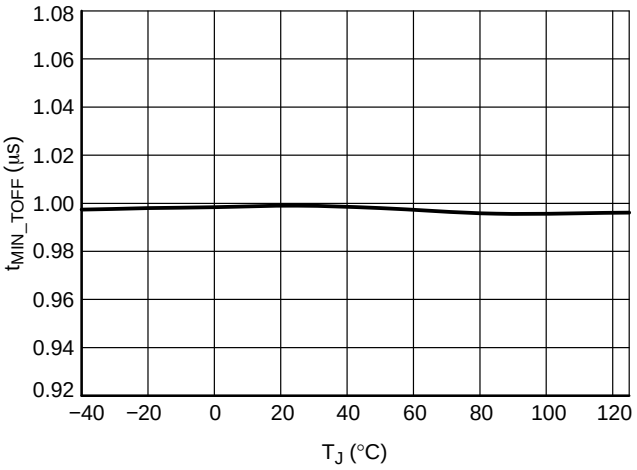


Figure 35. Minimum Off−time R_{MIN_TOFF} = 10 kΩ

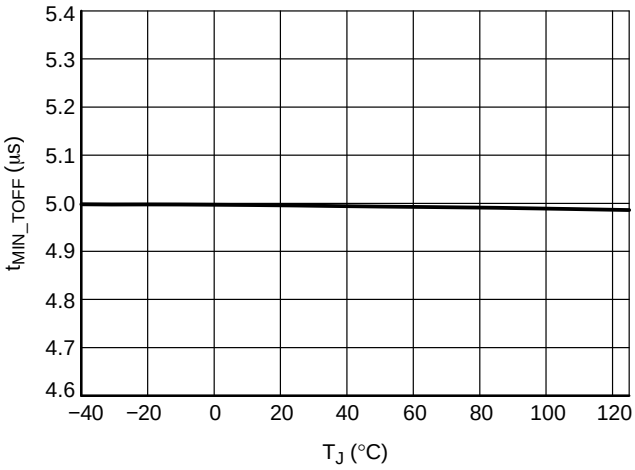


Figure 36. Minimum Off−time R_{MIN_TOFF} = 50 kΩ

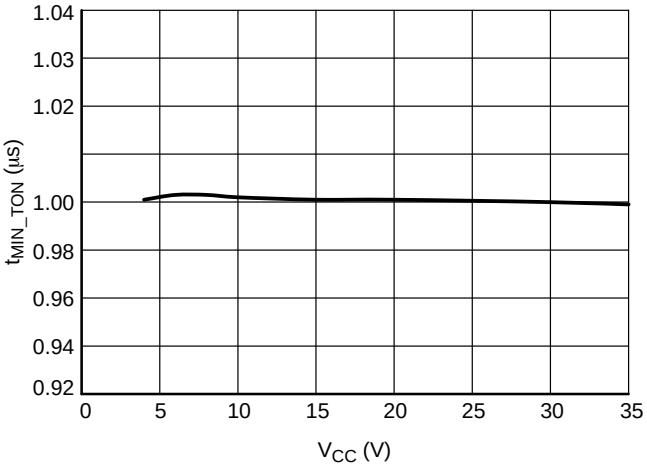


Figure 37. Minimum On−time R_{MIN_TON} = 10 kΩ

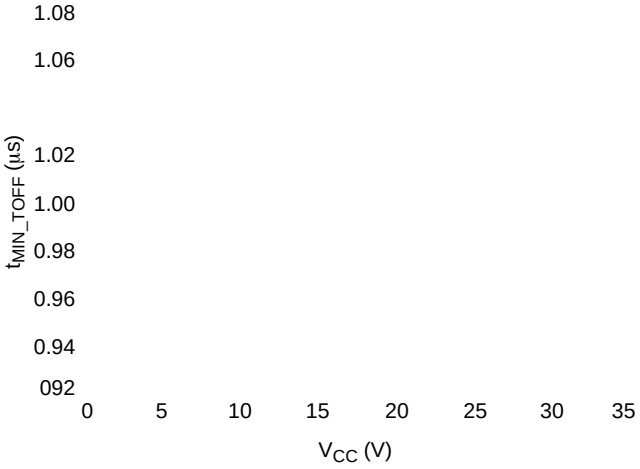


Figure 38. Minimum Off−time R_{MIN_TOFF} = 10 kΩ

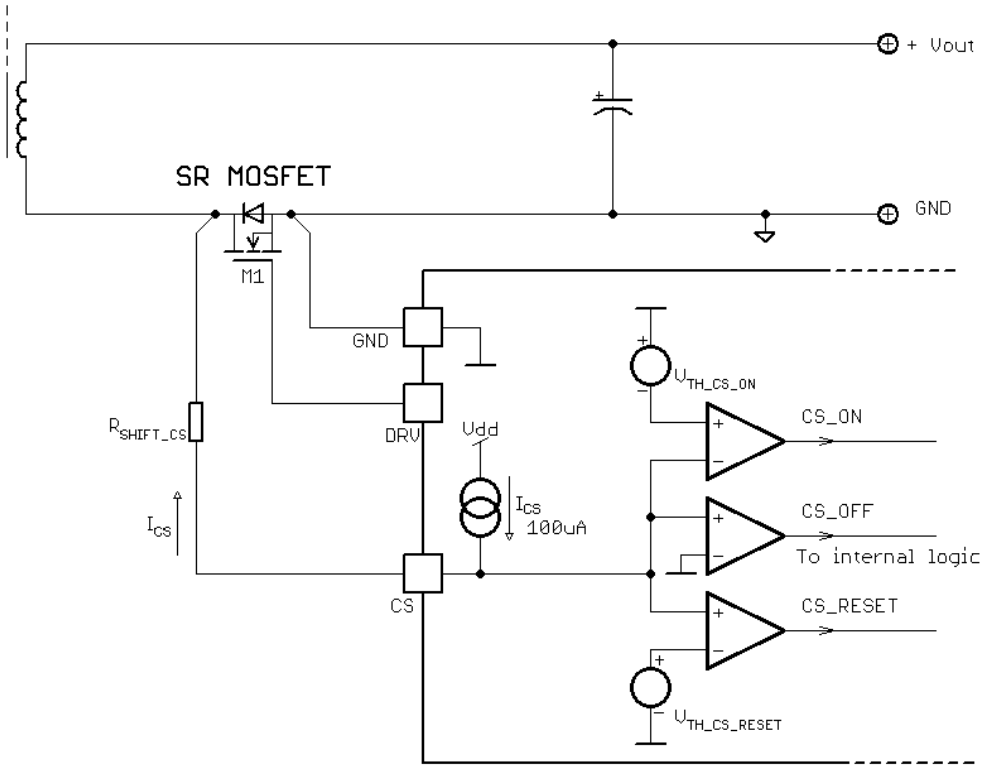
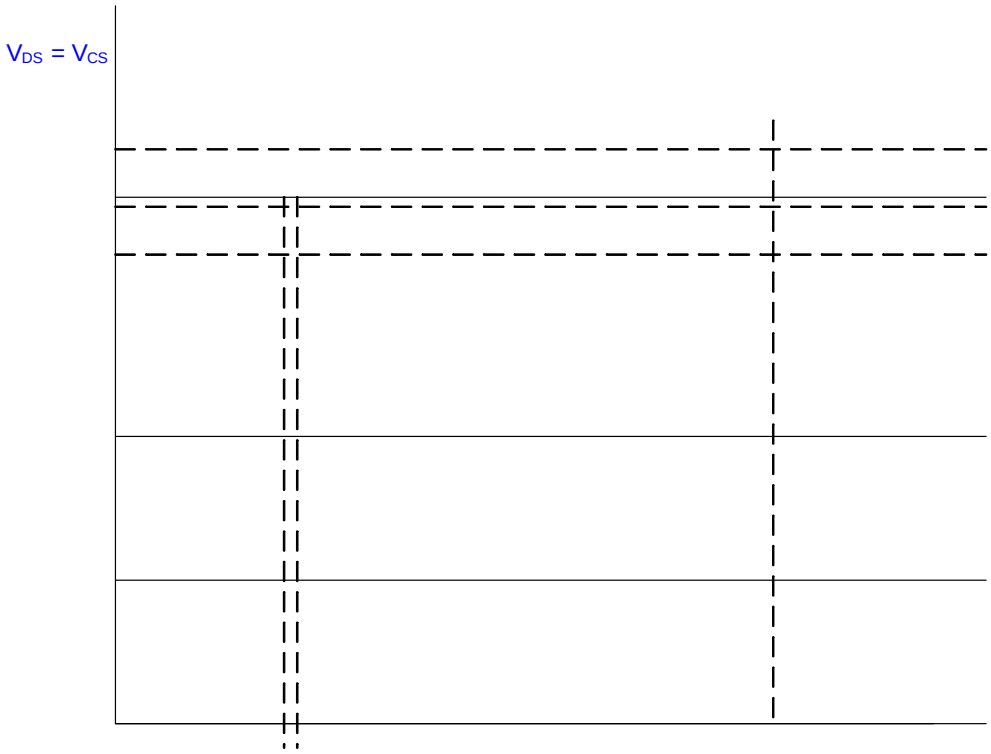


Figure 44. Current Sensing Circuitry Functionality

The SR MOSFET is turned-off as soon as the voltage on the CS pin is higher than $V_{TH\_CS\_OFF}$ (typically −0.5 mV minus any voltage dropped on the optional R_{SHIFT_CS}). For the same ringing reason, a minimum off-time timer is asserted once the V_{CS} goes above $V_{TH\_CS\_RESET}$. The minimum off-time can be externally adjusted using R_{MIN_TOFF} resistor. The minimum off−time generator can be re−triggered by MIN_TOFF reset compa6(gene12145 r)4NTt comp05 Tc.0257 Twmuscurs.3528 38 8 input af-6.10.902 0 T[(mi


V_{DS} = V_{CS}

If no R_{SHIFT_CS} resistor is used, the turn-on, turn-off and $V_{TH\_CS\_RESET}$ thresholds are fully given by the CS input specification (please refer to electrical characteristics table). The CS pin offset current causes a voltage drop that is equal to:

$$V_{RSHIFT\_CS} = R_{SHIFT\_CS} * I_{CS} \quad \text{(eq. 1)}$$

Final turn−on and turn off thresholds can be then calculated as:

$V_{CS\_TURN\_ON}$

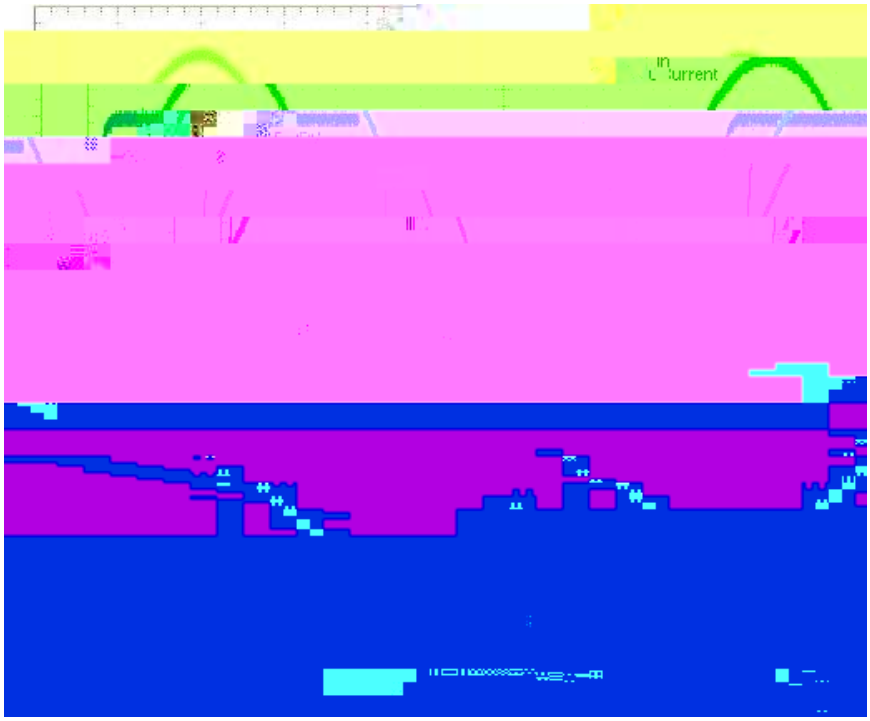


Figure 48. Waveforms From SR System Implemented in LLC Application and Using MOSFET in TO220 Package With Long Leads − SR MOSFET channel Conduction Time is Reduced

Note that the efficiency impact caused by the error voltage due to the parasitic inductance increases with lower MOSFETs $R_{DS(on)}$ and/or higher operating frequency.

It is thus beneficial to minimize SR MOSFET package leads length in order to maximize application efficiency. The optimum solution for applications with high secondary current $\Delta i/\Delta t$ and high operating frequency is to use lead−less SR MOSFET i.e. SR MOSFET in SMT package. The parasitic inductance of a SMT package is negligible causing insignificant CS turn−off threshold shift and thus minimum impact to efficiency (refer to Figure 49).


Drain Current
CS

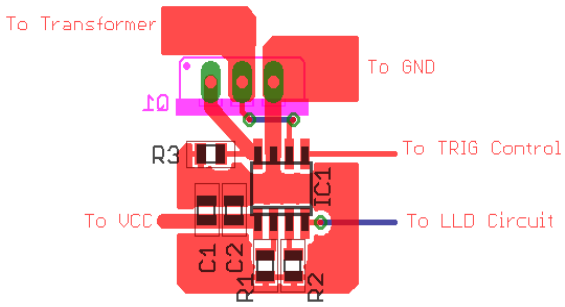
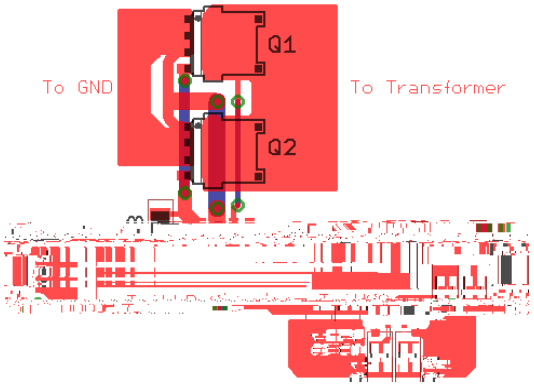
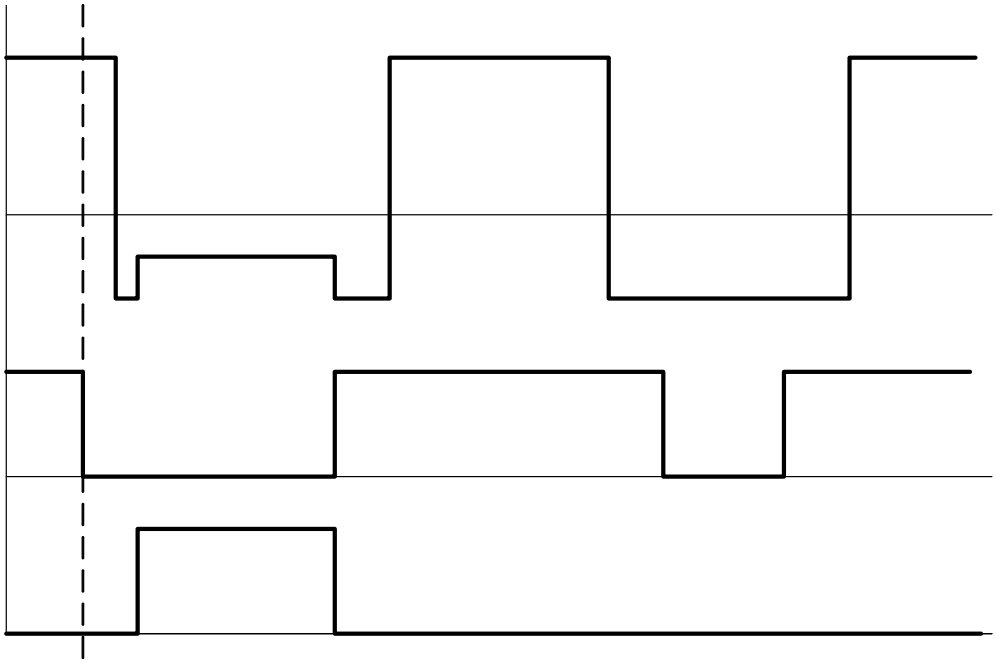
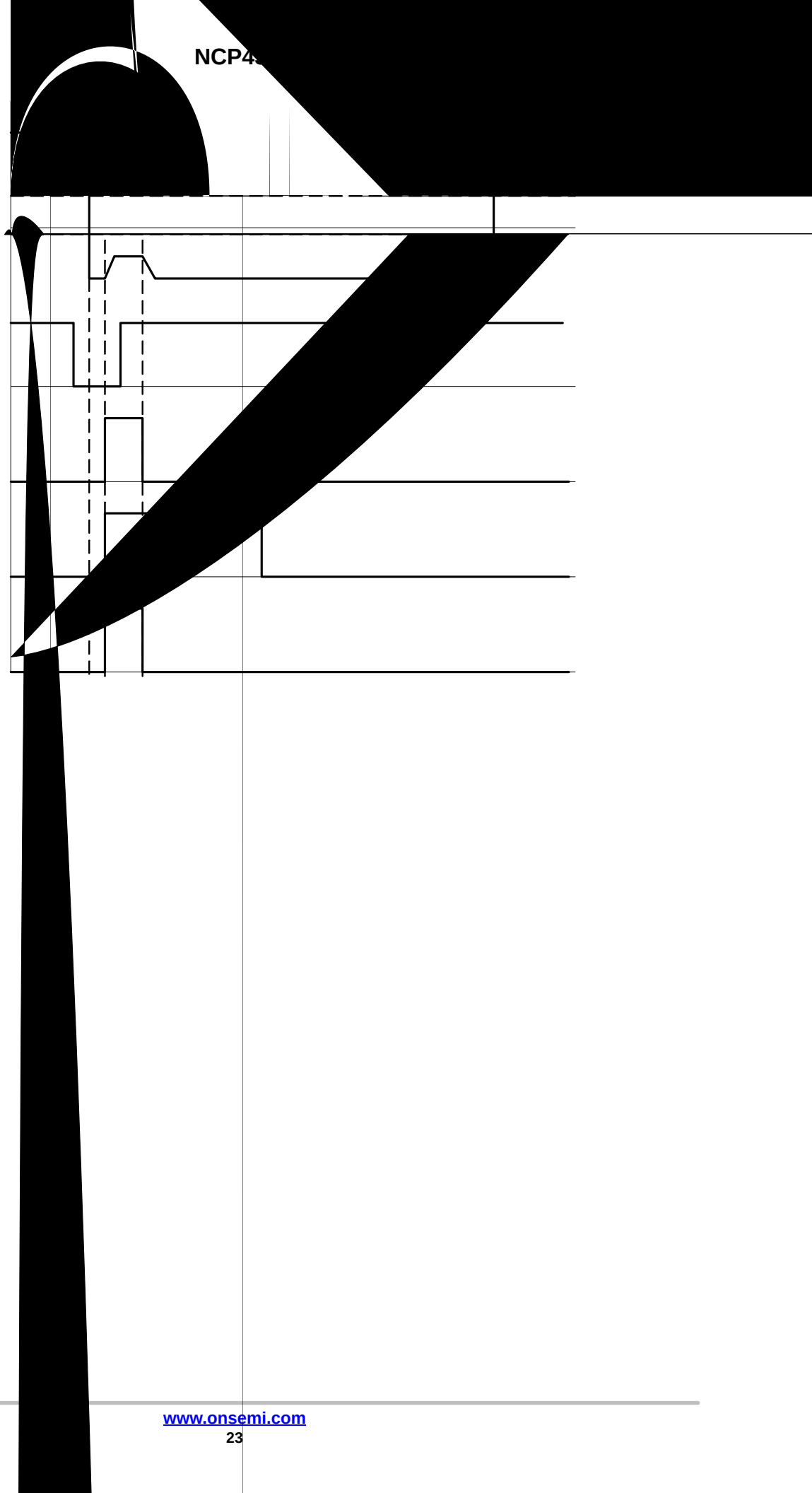
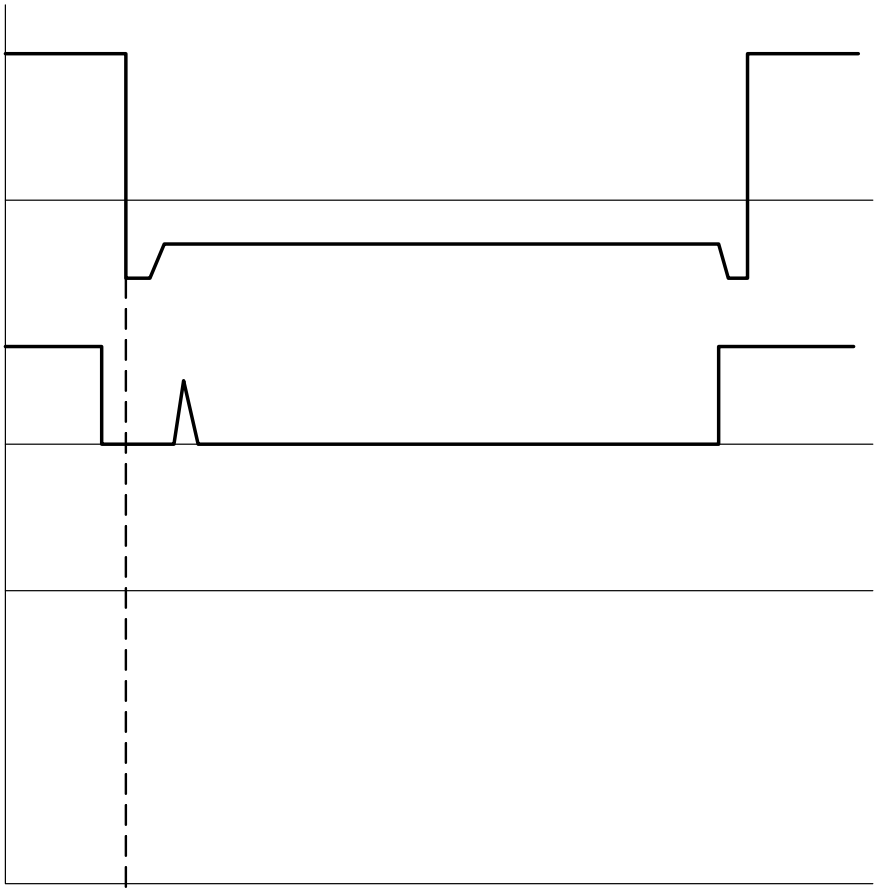


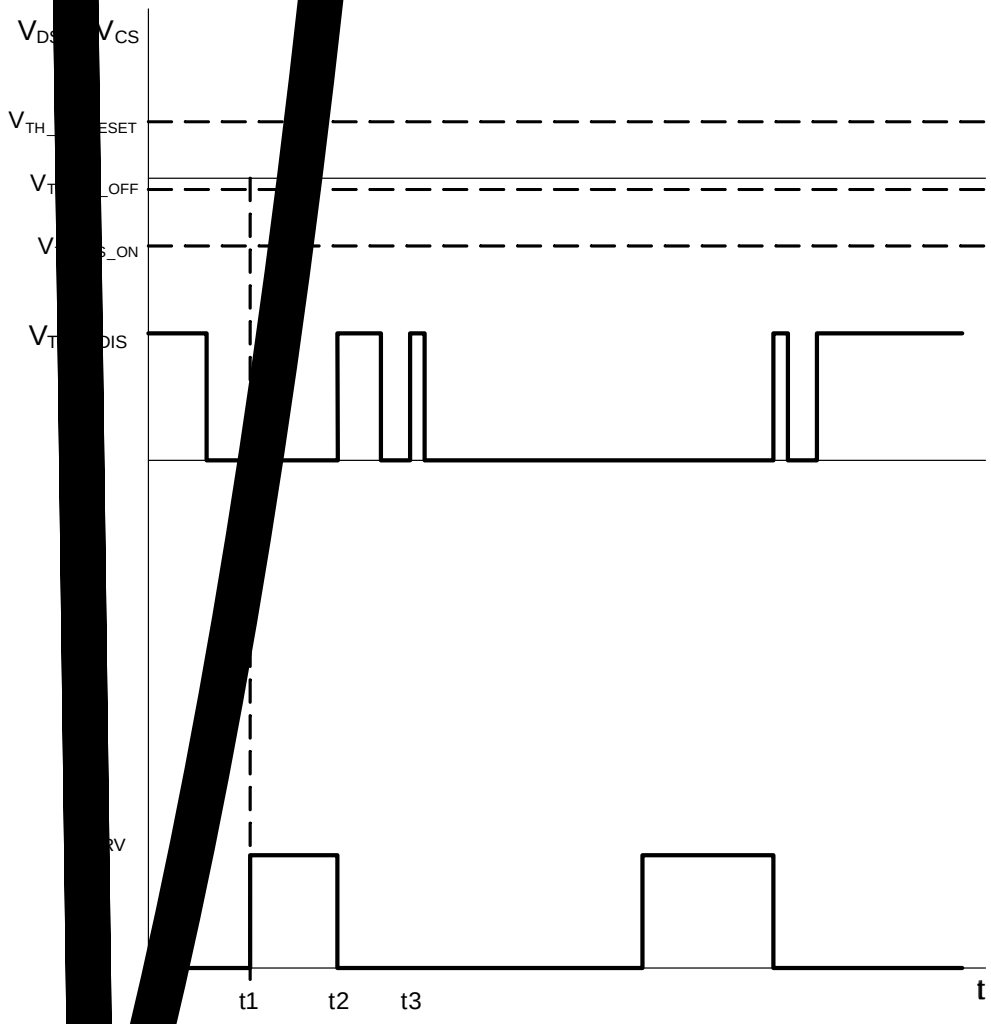
Figure 50. Recommended Layout When Using SR

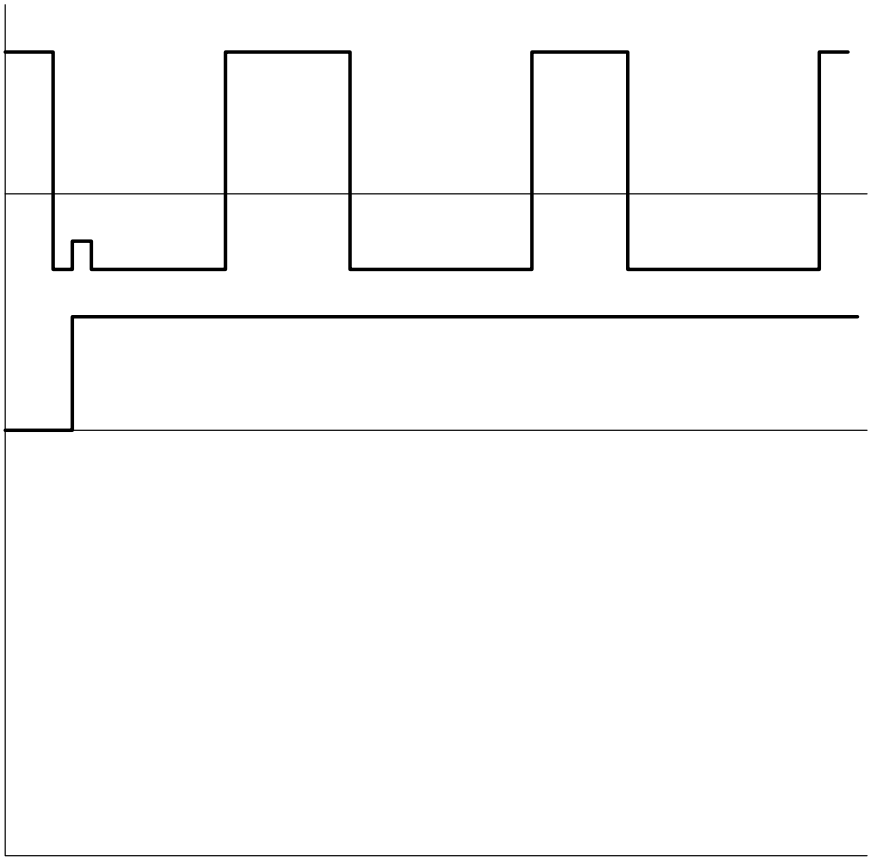


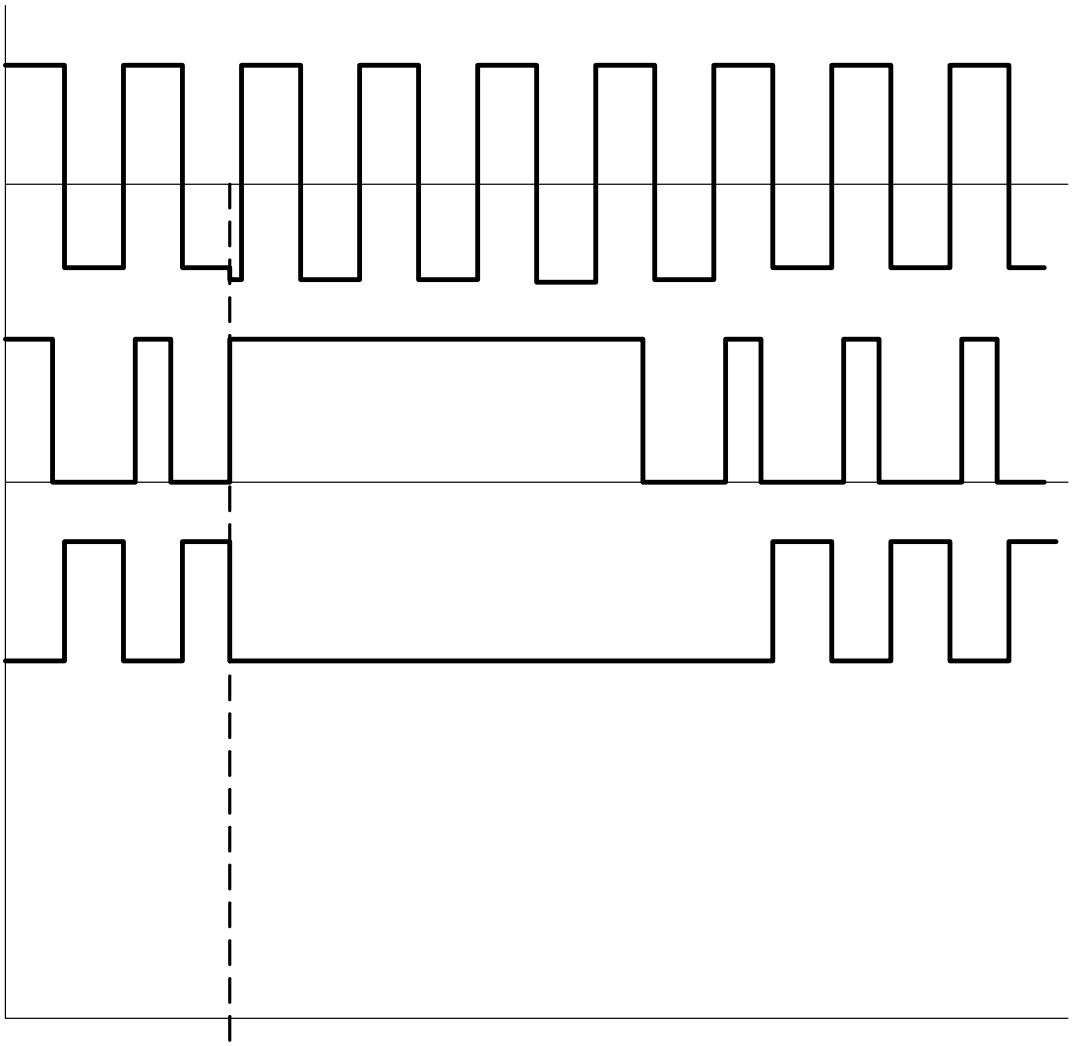







V_{CS}
V_{TH_RESET}
V_{TH_OFF}
V_{TH_ON}
V_{TH_DIS}
t1
t2
t3
t





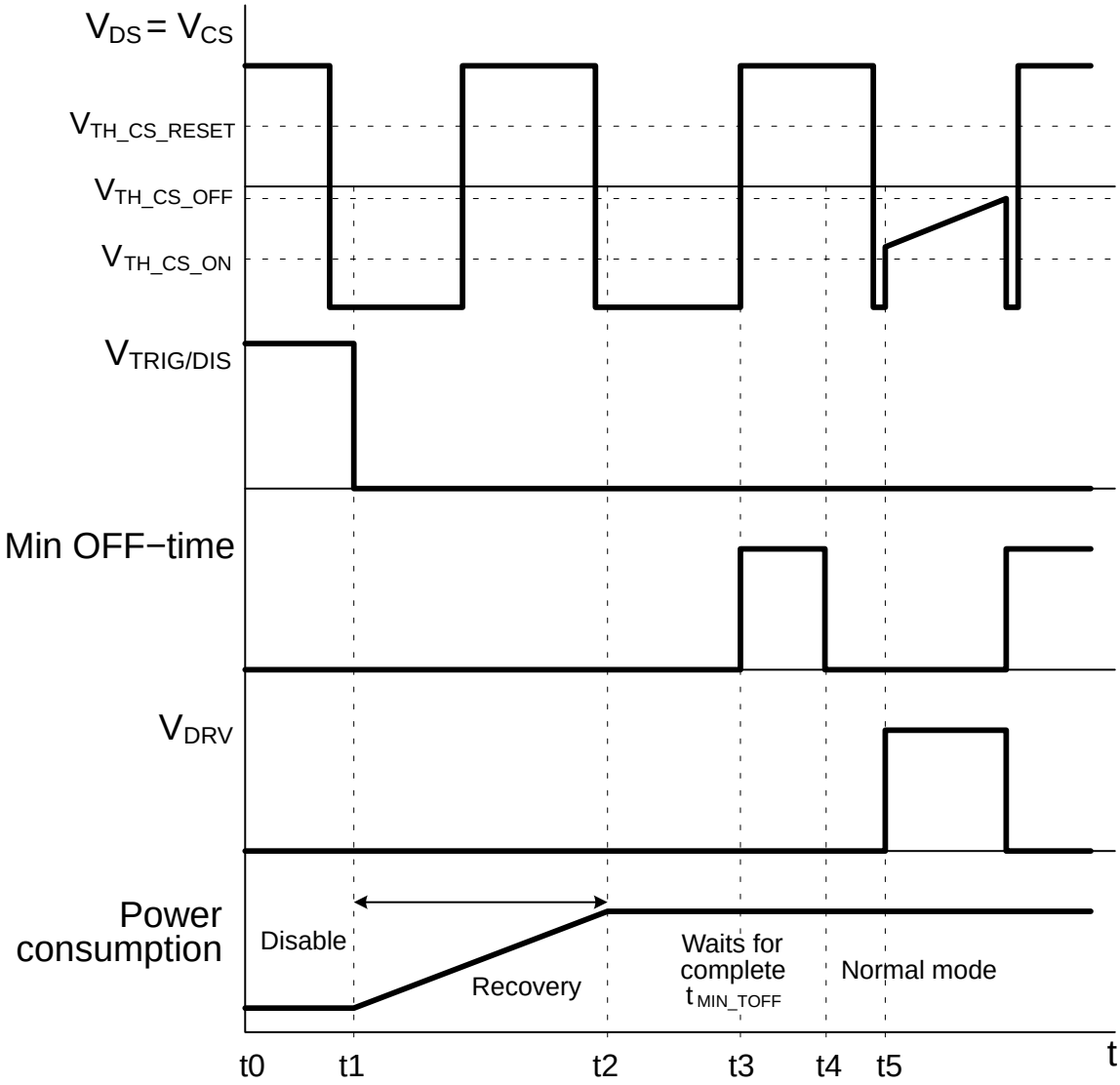


Figure 63. Trigger Input Functionality Waveforms

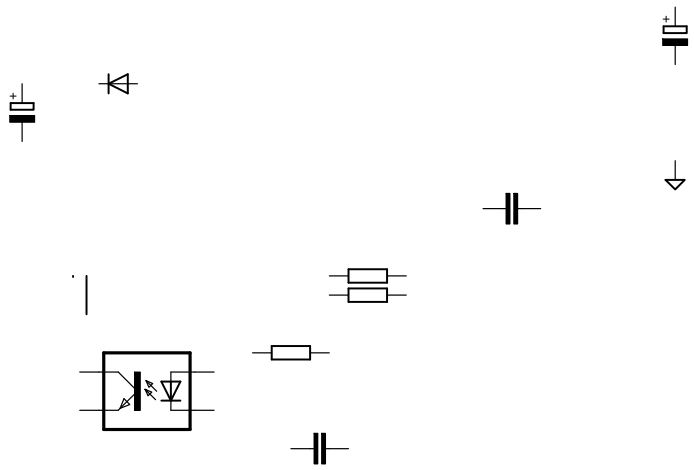


Figure 66. Primary Triggering in Deep CCM Application Using Auxiliary Winding − NCP4305A, B, C or D

100 ns) to be transmitted to the NCP4305 trigger input. The advantage of needle trigger pulse usage is that the required volt−second product of the pulse transformer is very low and that allows the designer to use very small and cheap

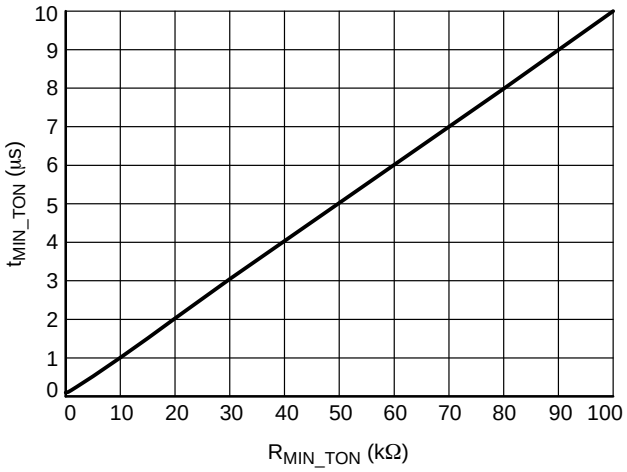


Figure 69. MIN_TON Adjust Characteristics

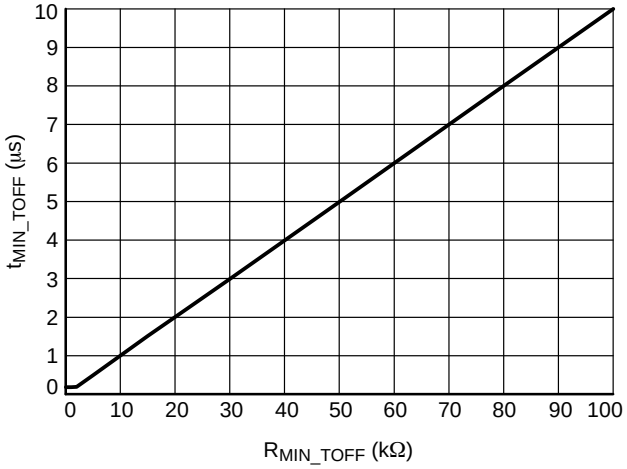


Figure 70. MIN_TOFF Adjust Characteristics

The absolute minimum t_{ON} duration is internally clamped to 55 ns and minimum t_{OFF} duration to 245 ns in order to prevent any potential issues with the MIN_TON and/or MIN_TOFF pins being shorted to GND.

The NCP4305 features dedicated anti−ringing protection system that is implemented with a MIN_TOFF blank generator. The minimum off−time one−shot generator is restarted in the case when the CS pin voltage crosses $V_{TH\_CS\_RESET}$ threshold and MIN_TOFF period is active. The total off-time blanking period is prolonged due to the ringing in the application (refer to Figure 45).

Some applications may require adaptive minimum on and off time blanking periods. With NCP4305 it is possible to modulate blanking periods by using an external NPN transistor − refer to Figure 71. The modulation signal can be derived based on the load current, feedback regulator voltage or other application parameter.

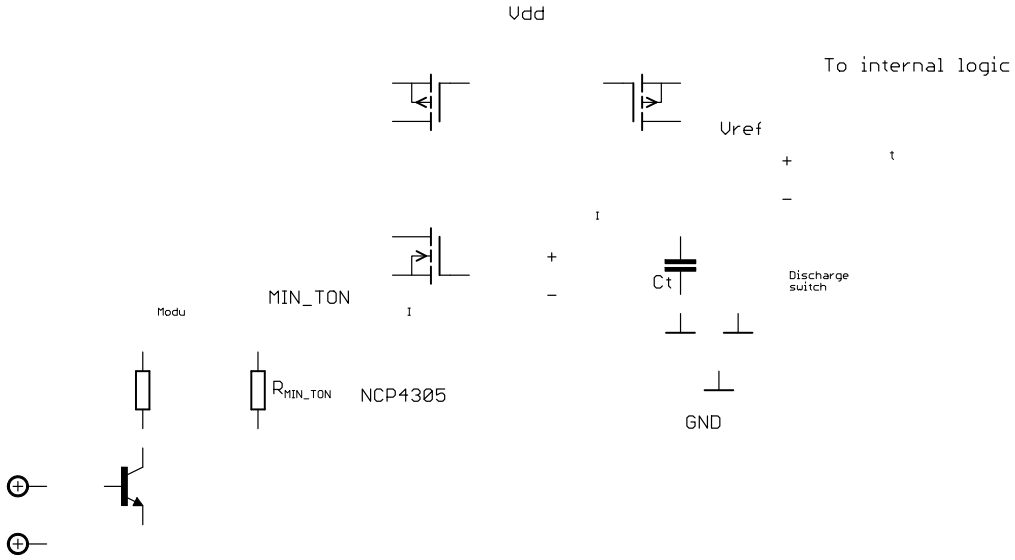


Figure 71. Possible Connection for MIN_T_{ON} and MIN_T_{OFF} Modulation

Maximum t_{ON} adjustment

The NCP4305Q offers an adjustable maximum on−time (like the min_t_{ON} and min_t_{OFF} settings shown above) that can be very useful for QR controllers at high loads. Under high load conditions the QR controller can operate in CCM thanks to this feature. The NCP4305Q version has the ability to turn−off the DRV signal to the SR MOSFET before the secondary side current reaches zero. The DRV signal from the NCP4305Q can be fed to the primary side through a pulse transformer (see Figure 4 for detail) to a transistor on the primary side to emulate a ZCD event before an actual ZCD event occurs. This feature helps to keep the minimum switching frequency up so that there is better energy transfer through the transformer (a smaller transformer core can be used). Also another advantage is that the IC controls the SR MOSFET and turns off from secondary side before the primary side is turned on in CCM to ensure no cross conduction. By controlling the SR MOSFET's turn off before the primary side turn off, producing a zero cross conduction operation, this will improve efficiency.

The Internal connection of the MAX_TON feature is shown in Figure 72. Figure 72 shows a method that allows for a modification of the maximum on−time according to output voltage. At a lower V_{OUT}, caused by hard overload or at startup, the maximum on−time should be longer than at nominal voltage. Resistor R_A can be used to modulate maximum on−time according to V_{OUT} or any other parameter.

The operational waveforms at heavy load in QR type SMPS are shown in Figure 73. After t_{MAX_TON} time is exceeded, the synchronous switch is turned off and the secondary current is conducted by the diode. Information about turned off SR MOSFET is transferred by the DRV pin through a small pulse transformer to the primary side where it acts on the ZCD detection circuit to allow the primary switch to be turned on. Secondary side current disappears before the primary switch is turned on without a possibility of cross current condition.

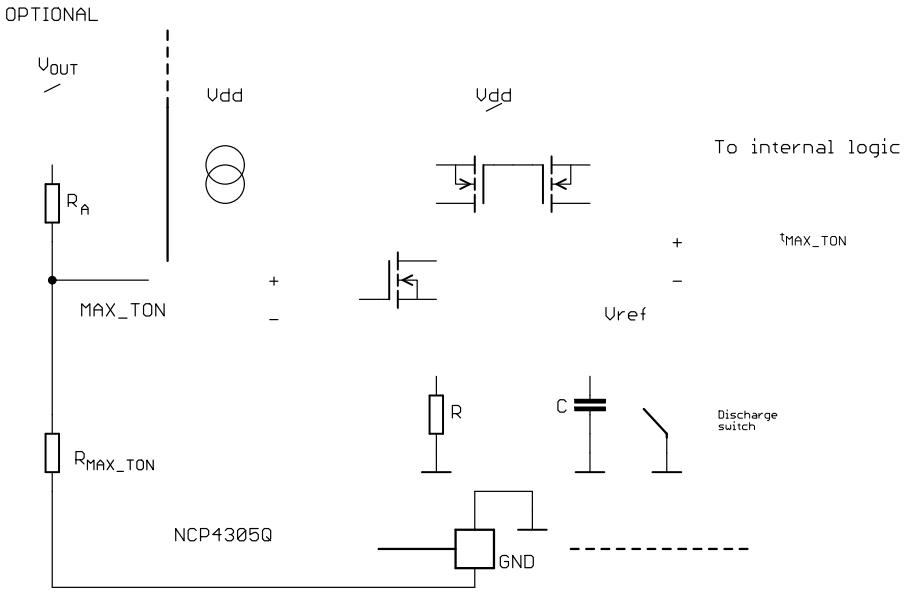
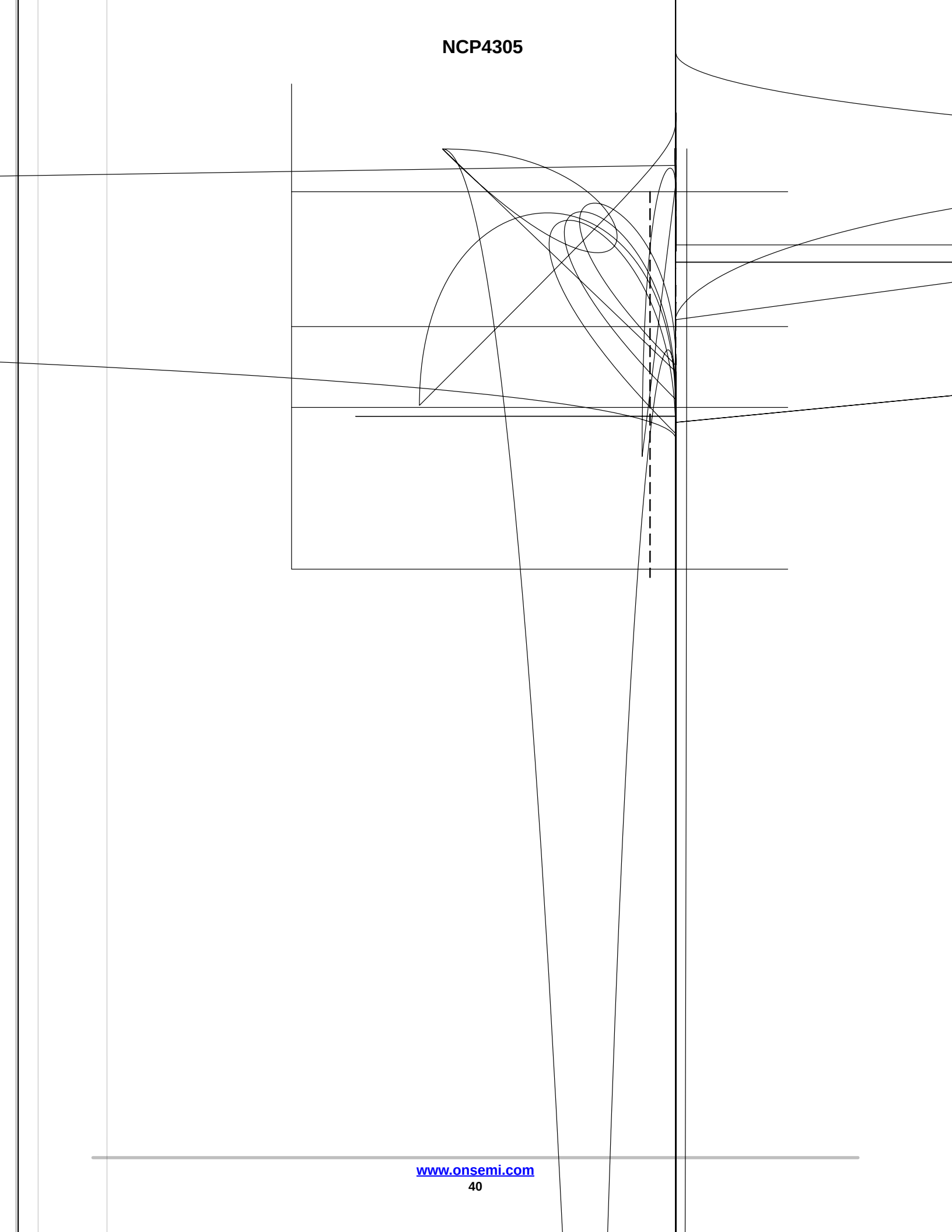
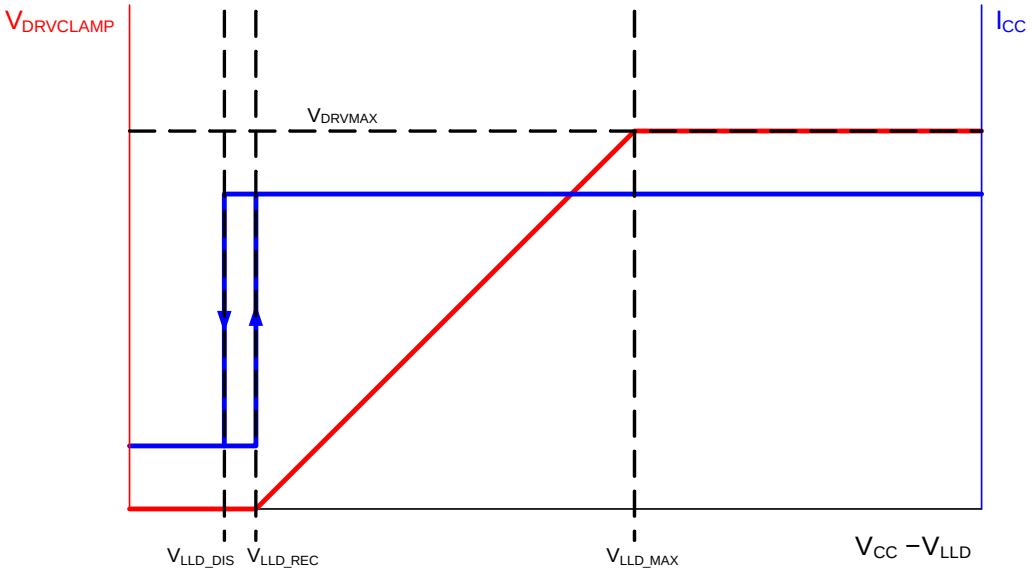


Figure 72. Internal Connection of the MAX_TON Generator, NCP4305Q




VDRVCLAMP
ICC
VDRVMAX
VLLD_DIS
VLLD_REC
VLLD_MAX
VCC −VLLD

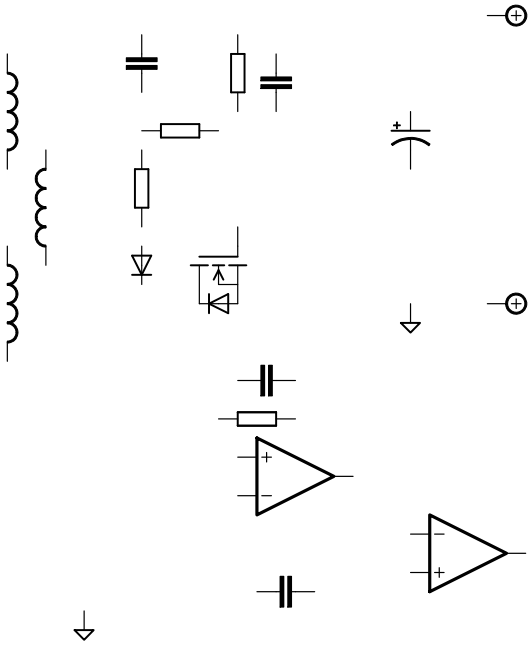


Figure 76. NCP4305 Light Load and No Load Detection Principle in Flyback Topologies

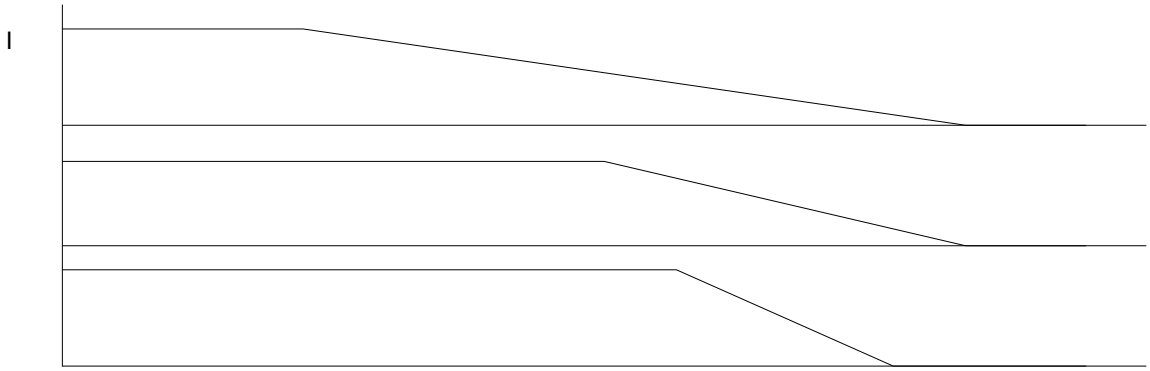
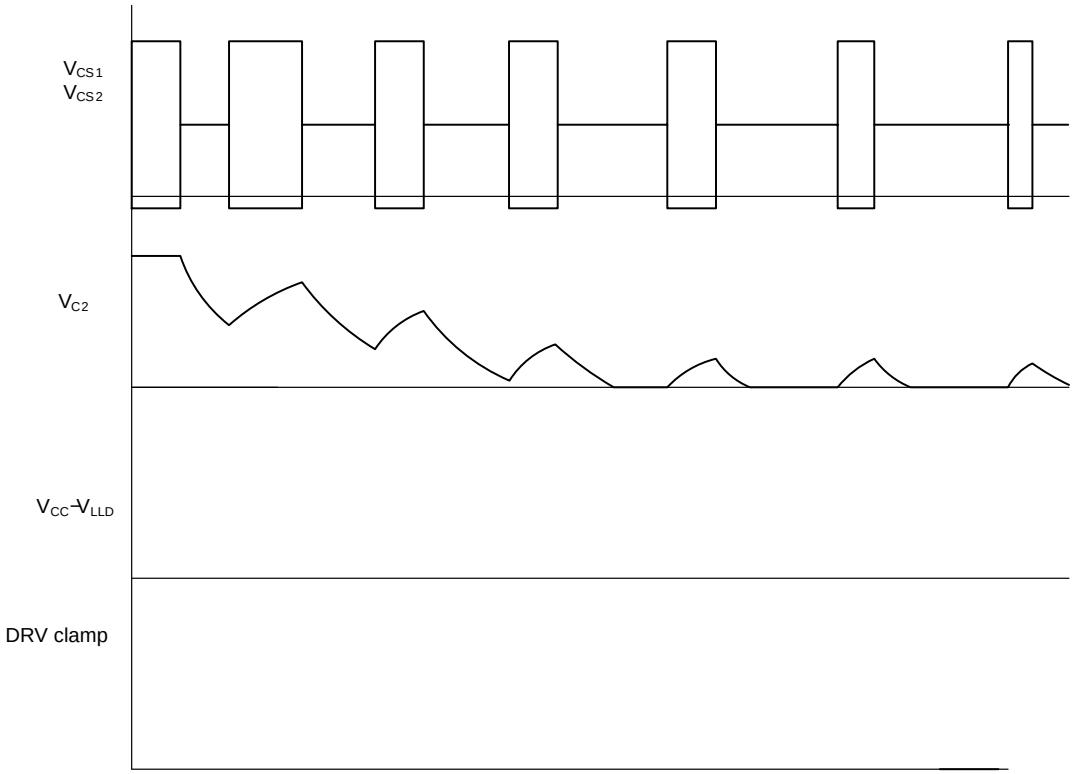


Figure 78. NCP4305 Driver Clamp Modulation Circuitry Transfer Characteristic in Flyback Application


V_{CS1}
V_{CS2}
V_{C2}
V_{CC}-V_{LLD}
DRV clamp

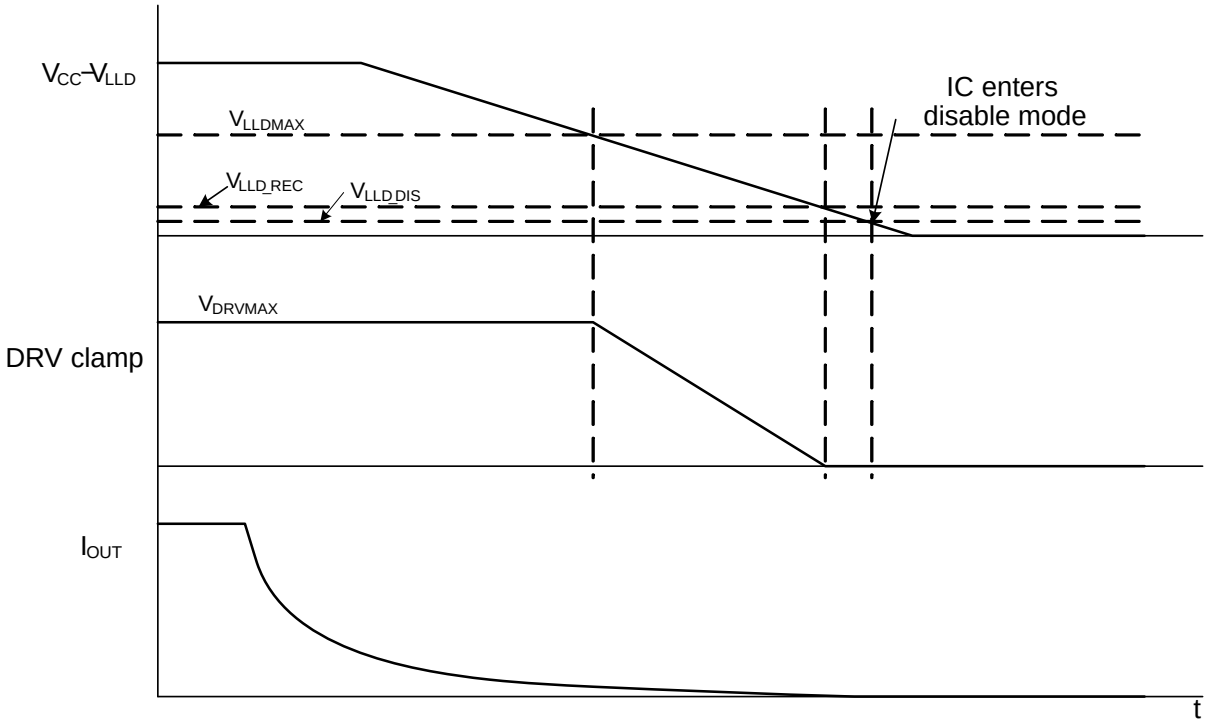
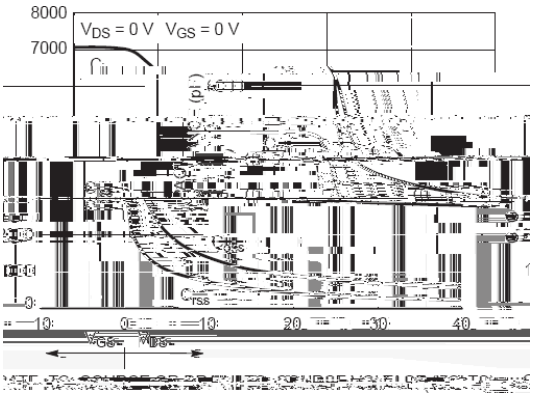
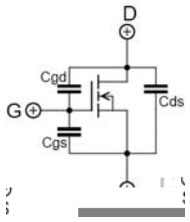


Figure 81. NCP4305 Driver Clamp Modulation Circuitry Characteristic in LLC Application

There exist some LLC applications where behavior described above is not the best choice. These applications transfer significant portion of energy in a few first pulses in skip burst. It is good to keep SR fully working during skip mode to improve efficiency. There can be still saved some energy using LLD function by activation disable mode between skip bursts. Simplified schematic for this LLD behavior is shown in Figure 46. Operation waveforms for this option are provided in Figure 83. Capacitor C2 is charged to





$$C_{iss} = C_{gs} + C_{gd}$$

$$C_{rss} = C_{gd}$$

$$C_{oss} = C_{ds} + C_{gd}$$

Figure 84. Typical MOSFET Capacitances Dependency on V_{DS} and V_{GS} Voltages

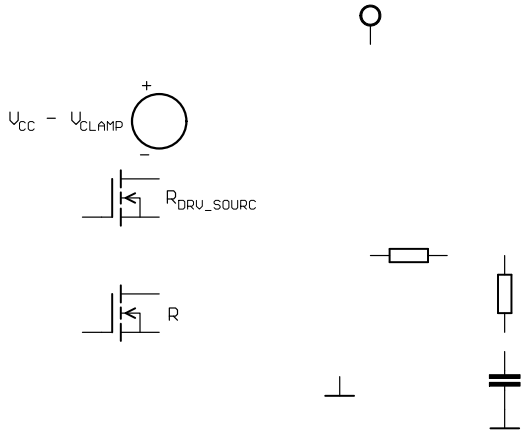


Figure 85. Equivalent Schematic of Gate Drive Circuitry

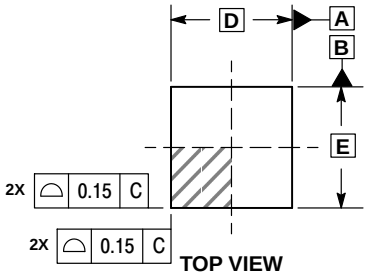
PRODUCT OPTIONS

OPN	Package	UVLO [V]	DRV clamp [V]	Pin 5 function	Usage
NCP4305ADR2G	SOIC8	4.5	4.7	TRIG	LLC, CCM flyback, DCM flyback, forward, QR, QR with primary side CCM control
NCP4305AMTTWG	WDFN8	4.5	4.7	TRIG	
NCP4305DDR2G	SOIC8	4.5	9.5	TRIG	
NCP4305DMNTWG	DFN8	4.5	9.5	TRIG	
NCP4305DMTTWG	WDFN8	4.5	9.5	TRIG	
NCP4305QDR2G	SOIC8	4.5	9.5	MAX_TON	QR with forced CCM from secondary side

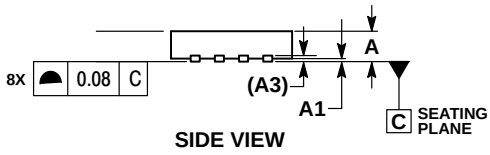
ORDERING INFORMATION

Device	Package	Package marking	Packing	Shipping†
NCP4305ADR2G	SOIC8	NCP4305A	SOIC−8 (Pb−Free)	

DFN8, 4x4

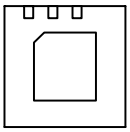


TOP VIEW

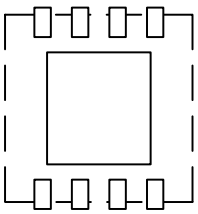


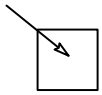
SIDE VIEW

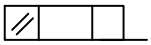
DIM	MILLIMETERS MIN	MAX
A		
A1		
A3		
b		
D		
D2		
E		
E2		
e		
K		---
L		

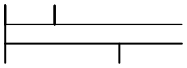


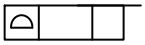
BOTTOM VIEW



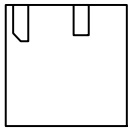


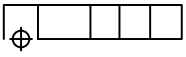






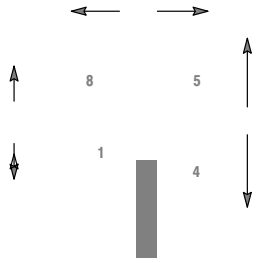

e

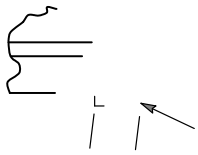




SOIC 8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011





SEATING
PLANE