NCP4308

S nchrono Rec ifier Con roller

The NCP4308 is a synchronous rectifier controller for switch mode power supplies. The controller enables high efficiency designs for flyback, quasi resonant flyback and LLC topologies.

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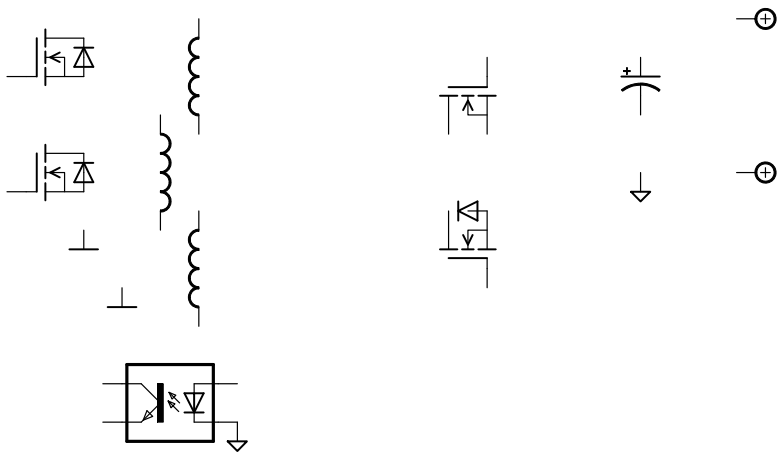


Figure 1. Typical Application Example − LLC Converter

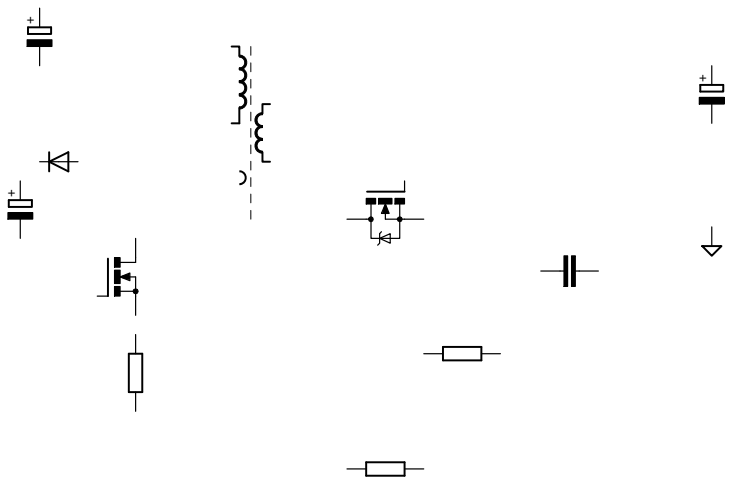


Figure 3. Typical Application Example − Primary Side Flyback Converter

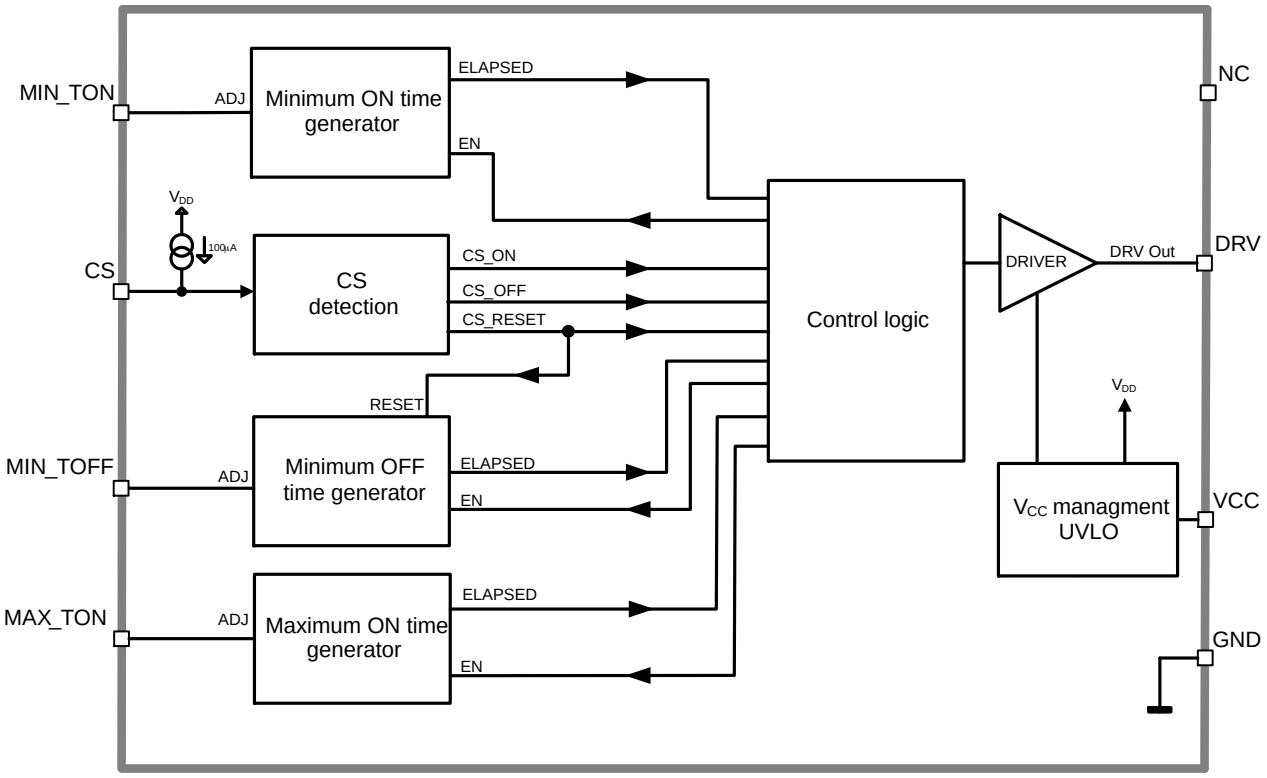


Figure 6. Internal Circuit Architecture − NCP4308Q (CCM QR) with MAX_TON

ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 125°C$; V_{CC} = 12 V; C_{DRV} = 0 nF; $R_{MIN_TON} = R_{MIN_TOFF}$ = 10 kΩ; V_{CS} = −1 to +4 V; f_{CS} = 100 kHz, DC_{CS} = 50%, unless otherwise noted. Typical values are at T_J = +25°C

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
MINIMUM t_{ON} and t_{OFF} ADJUST						
Minimum t_{ON} time	R_{MIN_TON} = 0 Ω	t_{ON_MIN}	35	55	75	ns
	R_{MIN_TON} = 0 Ω, DFN8, WDFN8	t_{ON_MIN}	25	50	75	ns
Minimum t_{OFF} time	R_{MIN_TOFF} = 0 Ω	t_{OFF_MIN}	190	245	290	ns
	R_{MIN_TOFF} = 0 Ω, DFN8, WDFN8	t_{OFF_MIN}	160	245	290	ns
Minimum t_{ON} time	R_{MIN_TON} = 10 kΩ	t_{ON_MIN}	0.92	1.00	1.08	μs
Minimum t_{OFF} time	R_{MIN_TOFF} = 10 kΩ	t_{OFF_MIN}	0.92	1.00	1.08	μs
Minimum t_{ON} time	R_{MIN_TON} = 50 kΩ	t_{ON_MIN}	4.62	5.00	5.38	μs
Minimum t_{OFF} time	R_{MIN_TOFF} = 50 kΩ	t_{OFF_MIN}	4.62	5.00	5.38	μs
MAXIMUM t_{ON} ADJUST						
Maximum t_{ON} Time	V_{MAX_TON} = 3 V	t_{ON_MAX}	4.3	4.8	5.3	μs
Maximum t_{ON} Time	V_{MAX_TON} = 0.3 V	t_{ON_MAX}	41	48	55	μs
Maximum t_{ON} Output Current	V_{MAX_TON} = 0.3 V	I_{MAX_TON}	−105	−100	−95	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

TYPICAL CHARACTERISTICS

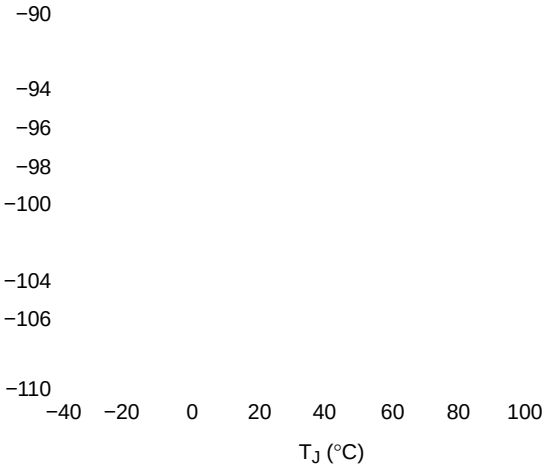


Figure 13. CS Current, V_{CS} = −20 mV

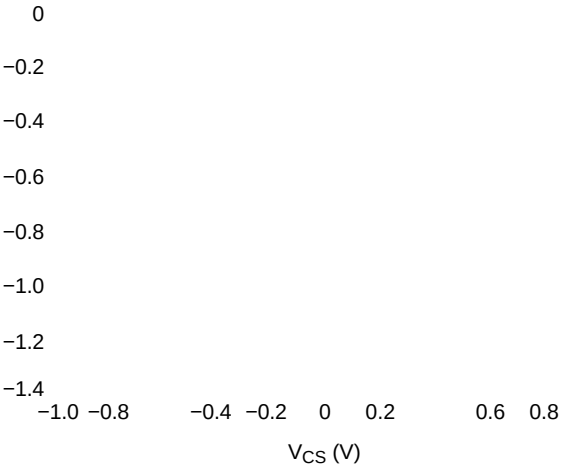


Figure 14. CS Current, V_{CC} = 12 V

V_{CS}

Figure 15. Supply Current vs. CS Voltage, V_{CC} = 12 V

Figure 16. CS Turn−on Threshold

TYPICAL CHARACTERISTICS

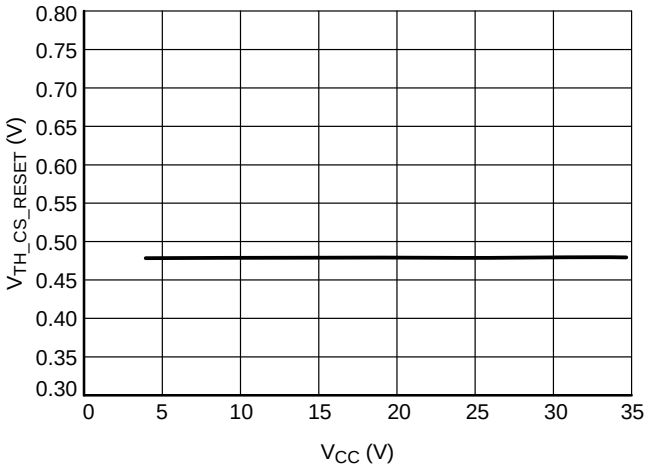


Figure 19. CS Reset Threshold

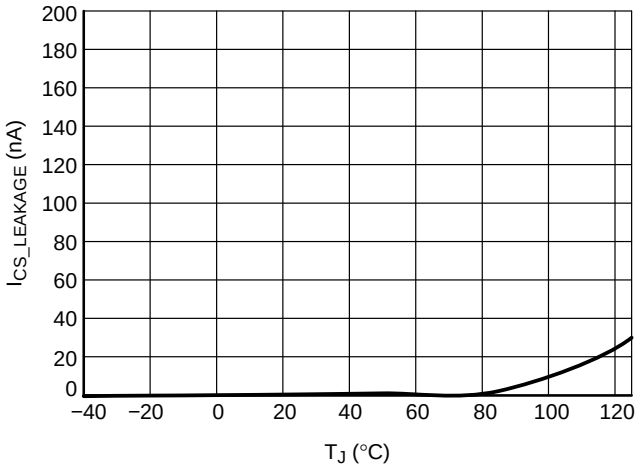


Figure 20. CS Leakage, V_{CS} = 150 V

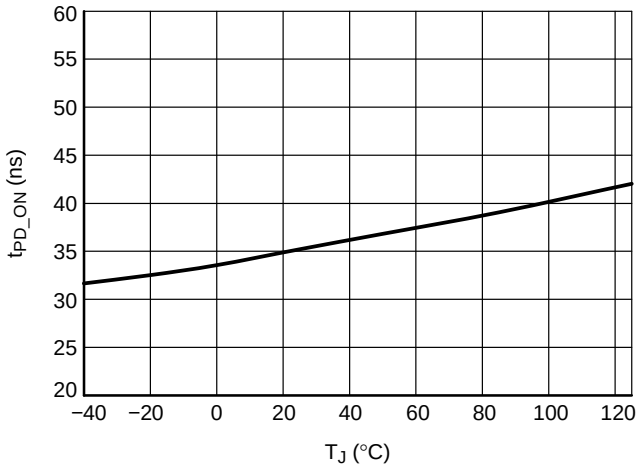


Figure 21. Propagation Delay from CS to DRV Output On

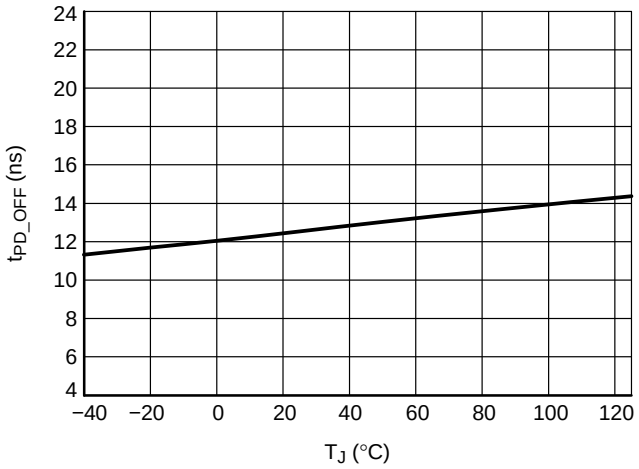


Figure 22. Propagation Delay from CS to DRV Output Off

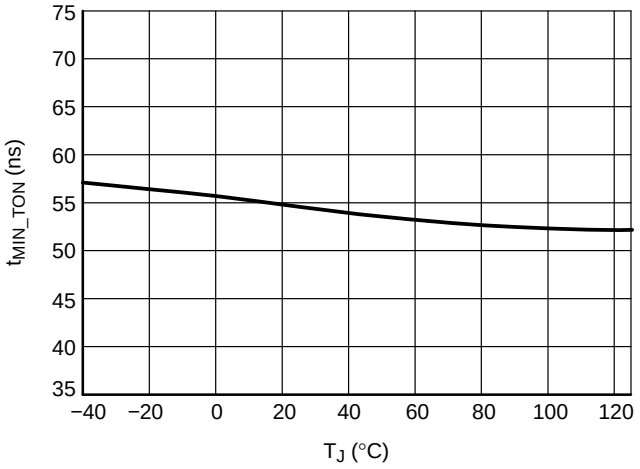


Figure 23. Minimum On−time R_{MIN_TON} = 0 Ω

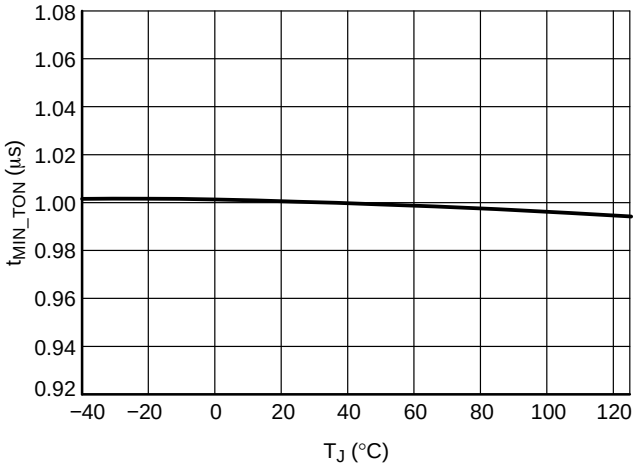


Figure 24. Minimum On−time R_{MIN_TON} = 10 kΩ

TYPICAL CHARACTERISTICS

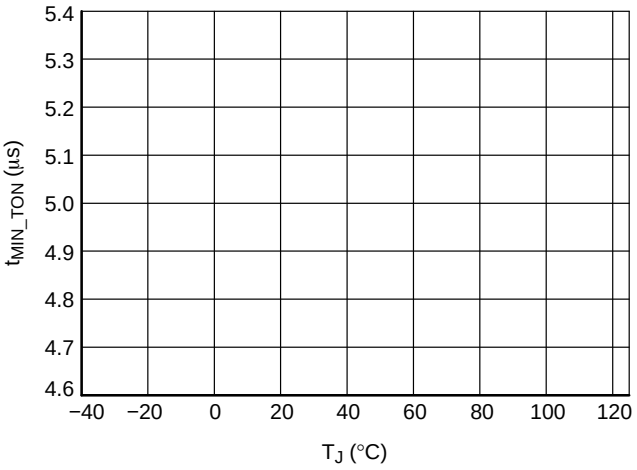


Figure 25. Minimum On−time R_{MIN_TON} = 50 kΩ

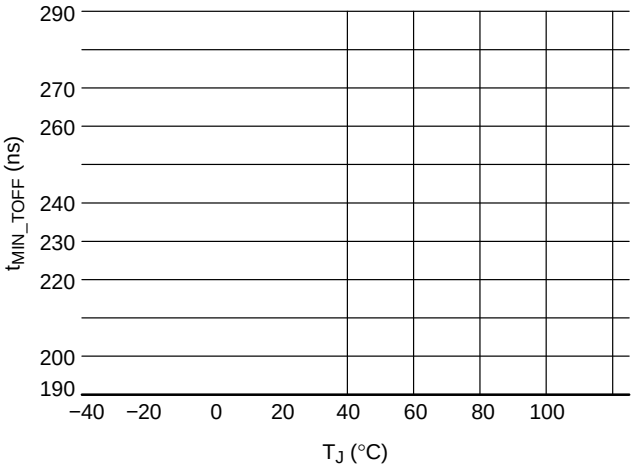


Figure 26. Minimum Off−time R_{MIN_TOFF} = 0 Ω

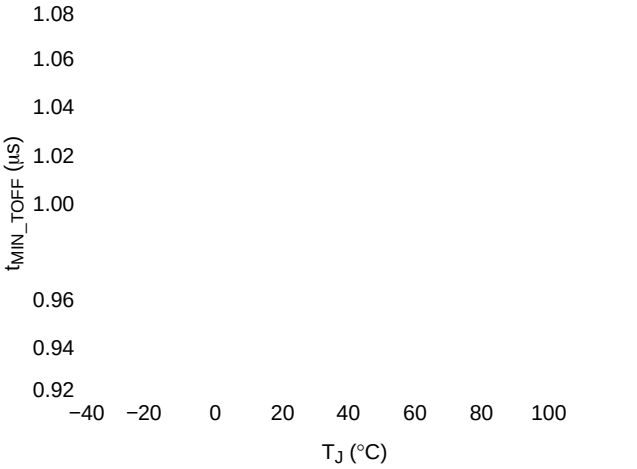


Figure 27. Minimum Off−time R_{MIN_TOFF} = 10 kΩ

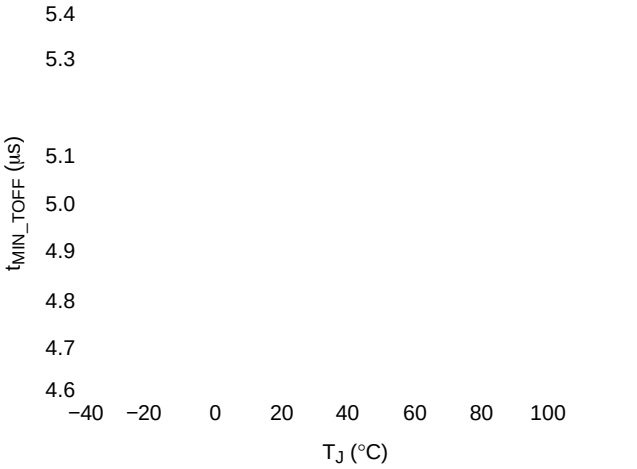


Figure 28. Minimum Off−time R_{MIN_TOFF} = 50 kΩ

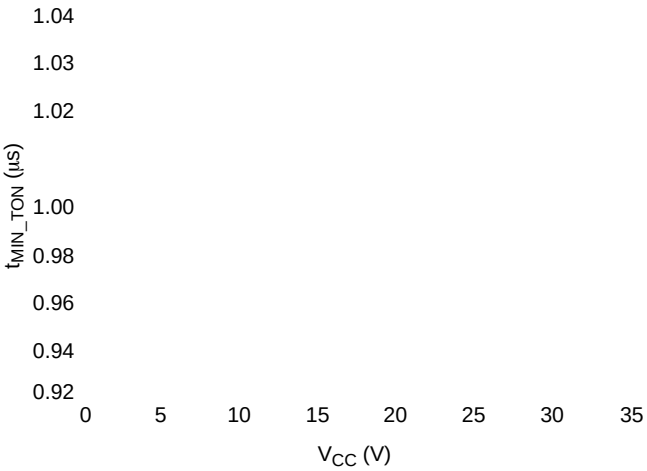


Figure 29. Minimum On−time R_{MIN_TON} = 10 kΩ

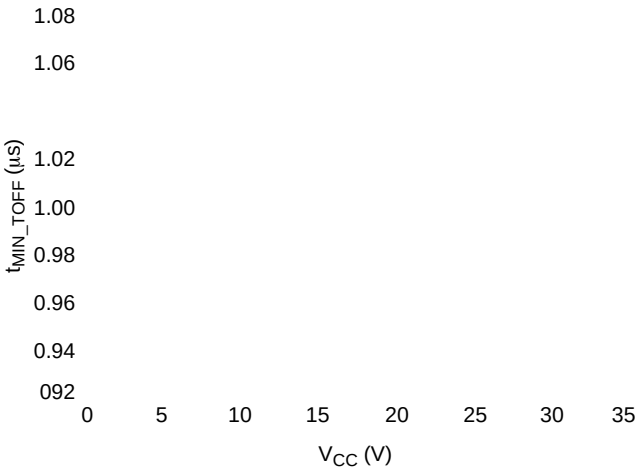


Figure 30. Minimum Off−time R_{MIN_TOFF} = 10 kΩ

TYPICAL CHARACTERISTICS

APPLICATION INFORMATION

General description

The NCP4308 is designed to operate either as a standalone IC or as a companion IC to a primary side controller to help achieve efficient synchronous rectification in switch mode power supplies. This controller features a high current gate driver along with high−speed logic circuitry to provide appropriately timed drive signals to a synchronous rectification MOSFET. With its novel architecture, the NCP4308 has enough versatility to keep the synchronous rectification system efficient under any operating mode.

The NCP4308 works from an available voltage with range from 4 V (A, D & Q options) or 8 V (B & C options) to 35 V (typical). The wide V_{CC} range allows direct connection to the SMPS output voltage of most adapters such as notebooks, cell phone chargers and LCD TV adapters.

Precise turn-off threshold of the current sense comparator together with an accurate offset current source allows the user to adjust for any required turn-of

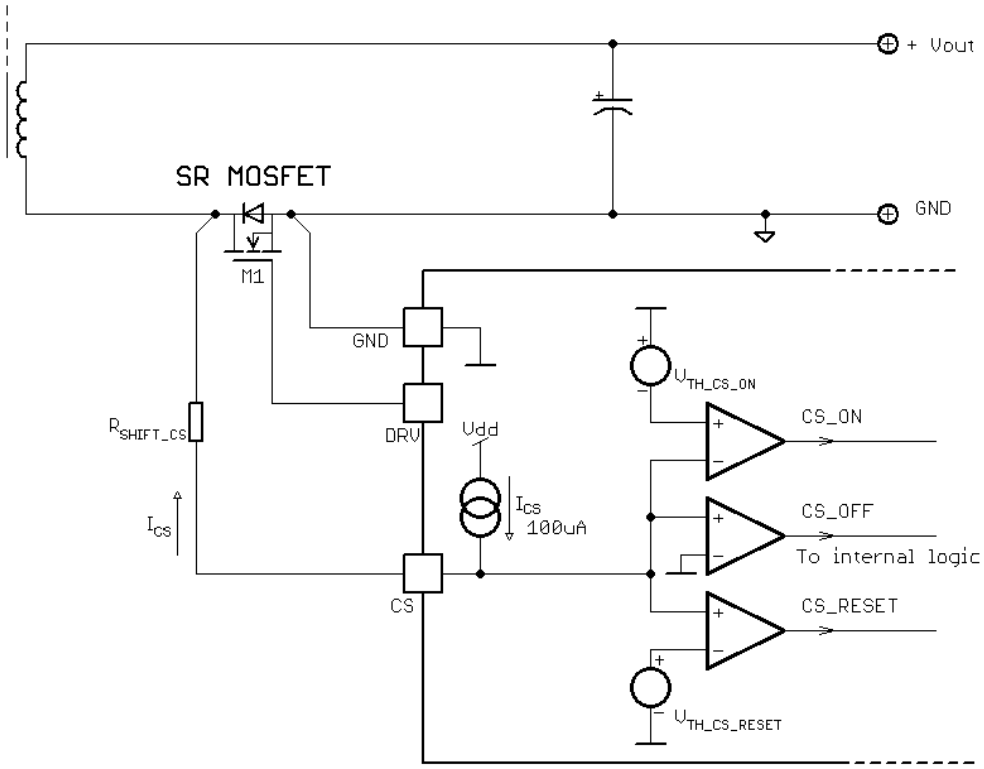
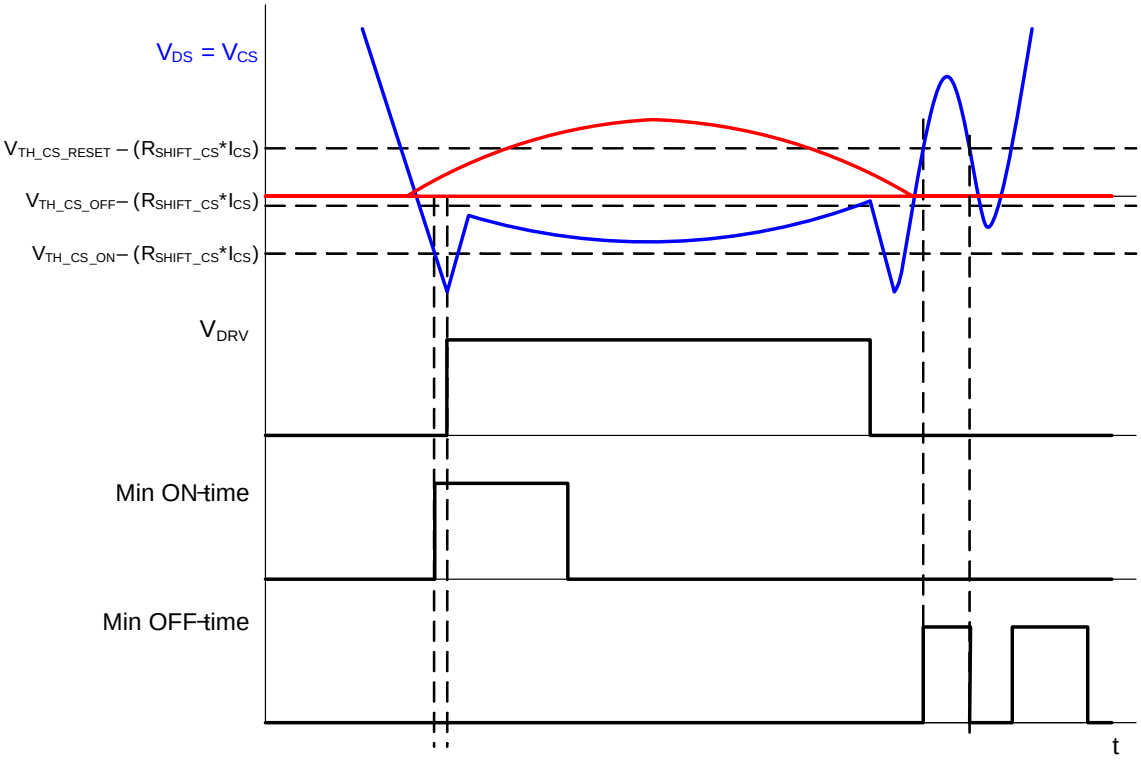


Figure 36. Current Sensing Circuitry Functionality

The SR MOSFET is turned-off as soon as the voltage on the CS pin is higher than $V_{TH_CS_OFF}$ (typically −0.5 mV minus any voltage dropped on the optional R_{SHIFT_CS}). For the same ringing reason, a minimum off-time timer is asserted once the V_{CS} goes above $V_{TH_CS_RESET}$. The minimum off-time can be externally adjusted using R_{MIN_TOFF} resistor. The minimum off−time generator can be re−triggered by MIN_TOFF reset comparator if some spurious ringing occurs on the CS input after SR MOSFET turn−off event. This feature significantly simplifies SR system implementation in flyback converters.

In an LLC converter the SR MOSFET M1 channel conducts while secondary side current is decreasing (refer to Figure 37). Therefore the turn−off current depends on MOSFET R_{DSON}. The −0.5 mV threshold provides an optimum switching period usage while keeping enough time margin for the gate turn-off. The R_{SHIFT_CS} resistor provides the designer with the possibility to modify (increase) the actual turn−on and turn−off secondary current thresholds. To ensure proper switching, the min_t_{OFF} timer is reset, when the V_{DS} of the MOSFET rings and falls down past the $V_{TH_CS_RESET}$. The minimum off−time needs to expire before another drive pulse can be initiated. Minimum off−time timer is started again when V_{DS} rises above $V_{TH_CS_RESET}$.


$V_{DS} = V_{CS}$
$V_{TH_CS_RESET} - (R_{SHIFT_CS} * I_{CS})$
$V_{TH_CS_OFF} - (R_{SHIFT_CS} * I_{CS})$
$V_{TH_CS_ON} - (R_{SHIFT_CS} * I_{CS})$
V_{DRV}
Min ON-time
Min OFF-time
t

If no R_{SHIFT_CS} resistor is used, the turn-on, turn-off and $V_{TH_CS_RESET}$ thresholds are fully given by the CS input specification (please refer to electrical characteristics table). The CS pin offset current causes a voltage drop that is equal to:

$$V_{RSHIFT_CS} = R_{SHIFT_CS} * I_{CS} \quad \text{(eq. 1)}$$

Final turn−on and turn off thresholds can be then calculated as:

$$V_{CS_TURN_ON} = V_{TH_CS_ON} - \left(R_{SHIFT_CS} * I_{CS}\right) \quad \text{(eq. 2)}$$

$$V_{CS_TURN_OFF} = V_{TH_CS_OFF} - \left(R_{SHIFT_CS} * I_{CS}\right) \quad \text{(eq. 3)}$$

$$V_{CS_RESET} = V_{TH_CS_RESET} - \left(R_{SHIFT_CS} * I_{CS}\right) \quad \text{(eq. 4)}$$

Note that R_{SHIFT_CS} impact on turn-on and $V_{TH_CS_RESET}$ thresholds is less critical than its effect on the turn−off threshold.

It should be noted that when using a SR MOSFET in a through hole package the parasitic inductance of the MOSFET package leads (refer to Figure 39) causes a turn−off current threshold increase. The current that flows through the SR MOSFET experiences a high $\Delta i(t)/\Delta t$ that induces an error voltage on the SR MOSFET leads due to their parasitic inductance. This error voltage is proportional to the derivative of the SR MOSFET current; and shifts the CS input voltage to zero when significant current still flows through the MOSFET channel. As a result, the SR MOSFET is turned−off prematurely and the efficiency of the SMPS is not optimized − refer to Figure 40 for a better understanding.

Figure 39. SR System Connection Including MOSFET and Layout Parasitic Inductances in LLC Application

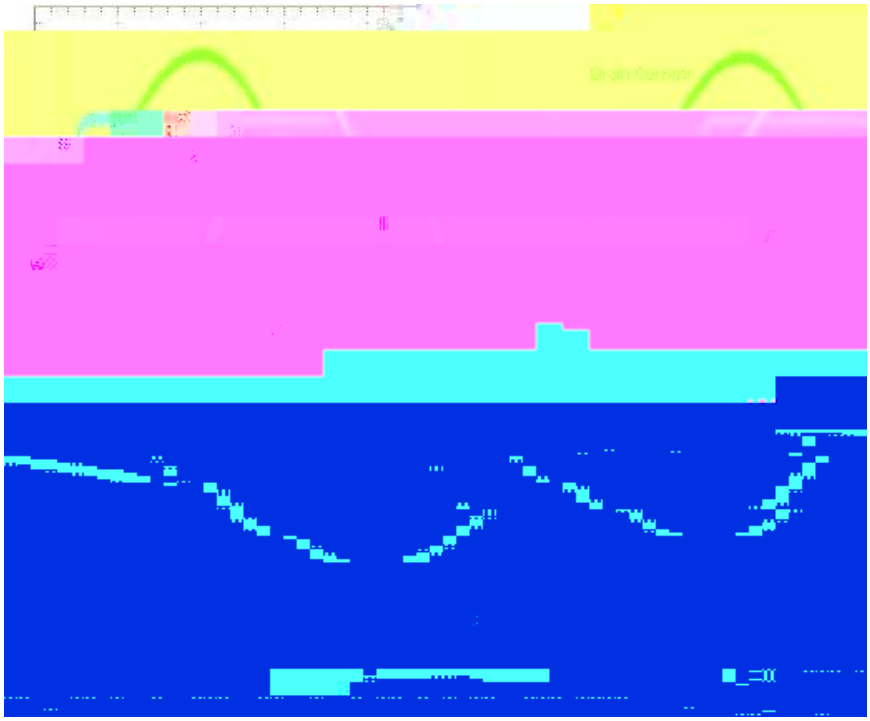


Figure 40. Waveforms From SR System Implemented in LLC Application and Using MOSFET in TO220 Package With Long Leads − SR MOSFET channel Conduction Time is Reduced

Note that the efficiency impact caused by the error voltage due to the parasitic inductance increases with lower MOSFETs $R_{DS(on)}$ and/or higher operating frequency.

It is thus beneficial to minimize SR MOSFET package leads length in order to maximize application efficiency. The optimum solution for applications with high secondary current $\Delta i/\Delta t$ and high operating frequency is to use lead−less SR MOSFET i.e. SR MOSFET in SMT package. The parasitic inductance of a SMT package is negligible causing insignificant CS turn−off threshold shift and thus minimum impact to efficiency (refer to Figure 41).

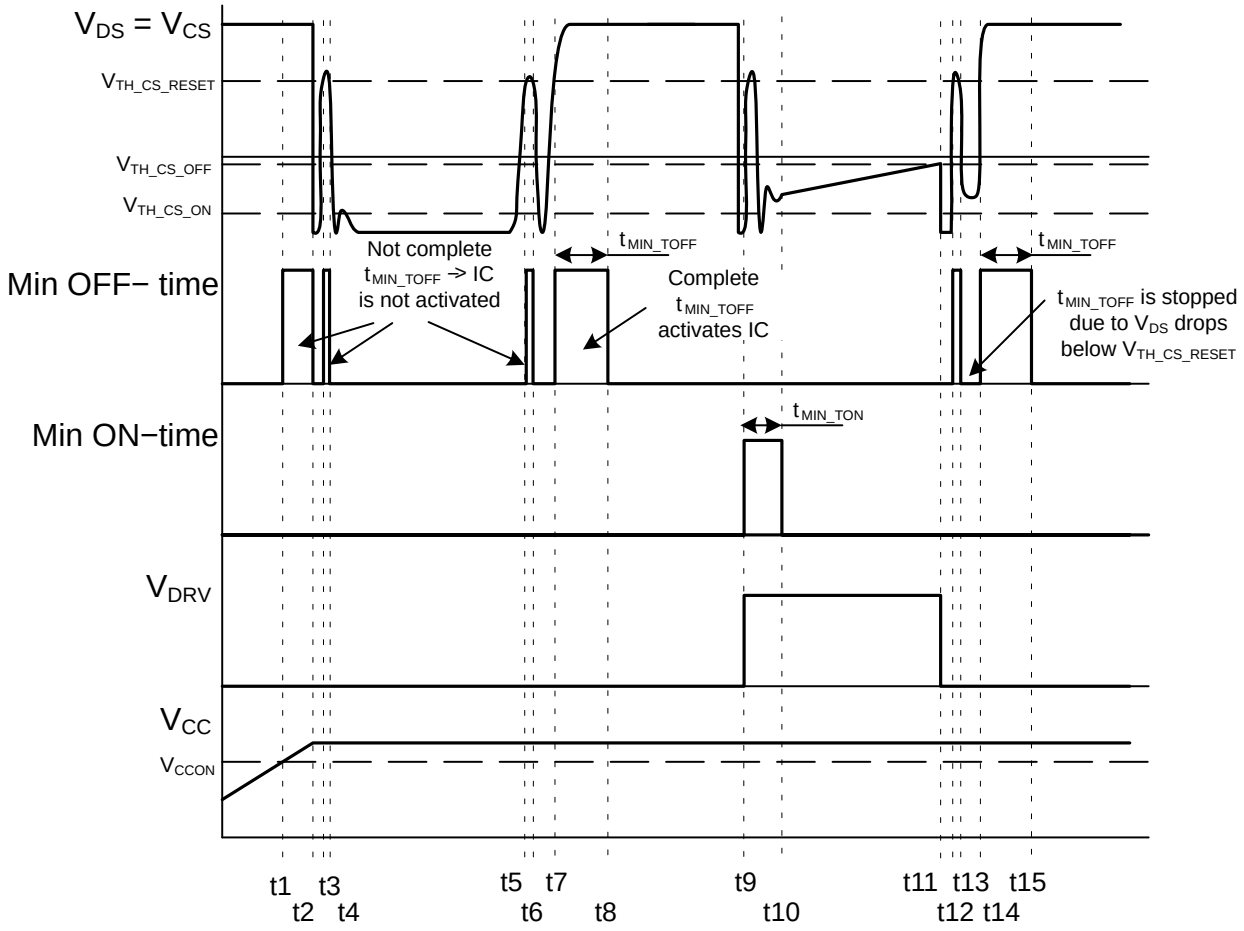


Figure 44. NCP4308 Operation after Start−Up Event

Self Synchronization

Self synchronization feature during start−up can be seen

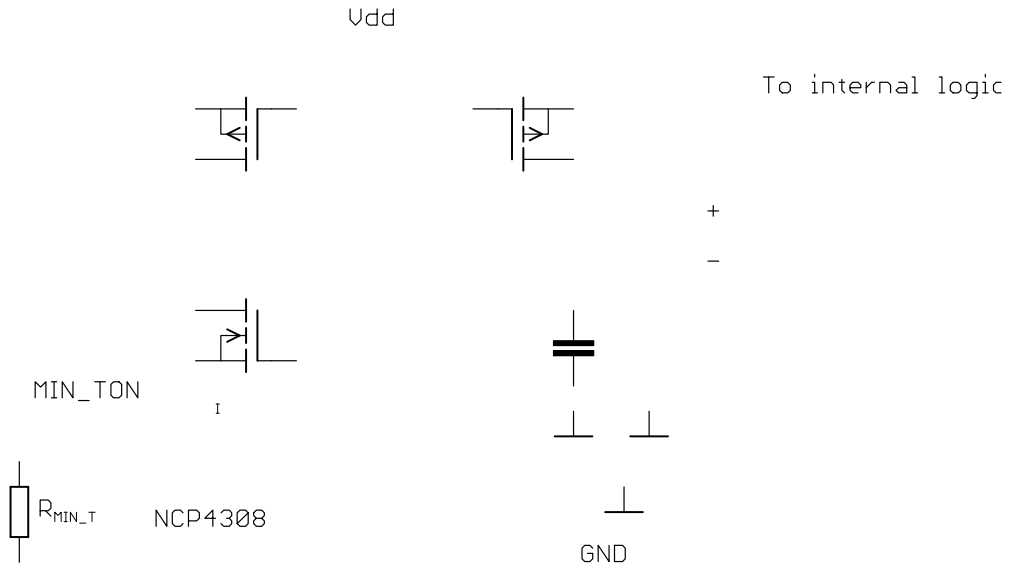


Figure 45. Internal Connection of the MIN_TON Generator (the MIN_TOFF Works in the Same Way)

The absolute minimum t_{ON} duration is internally clamped to 55 ns and minimum t_{OFF} duration to 245 ns in order to prevent any potential issues with the MIN_TON and/or MIN_TOFF pins being shorted to GND.

The NCP4308 features dedicated anti−ringing protection system that is implemented with a MIN_TOFF blank generator. The minimum off−time one−shot generator is restarted in the case when the CS pin voltage crosses $V_{TH_CS_RESET}$ threshold and MIN_TOFF period is active. The total off-time blanking period is prolonged due to the ringing in the application (refer to Figure 37).

Some applications may require adaptive minimum on and off time blanking periods. With NCP4308 it is possible to modulate blanking periods by using an external NPN transistor − refer to Figure 48. The modulation signal can be derived based on the load current, feedback regulator voltage or other application parameter.

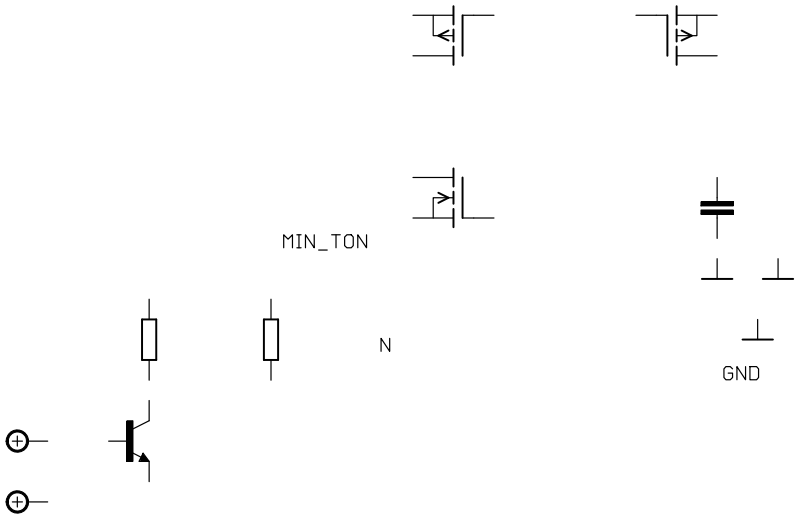


Figure 48. Possible Connection for MIN_T_{ON} and MIN_T_{OFF} Modulation

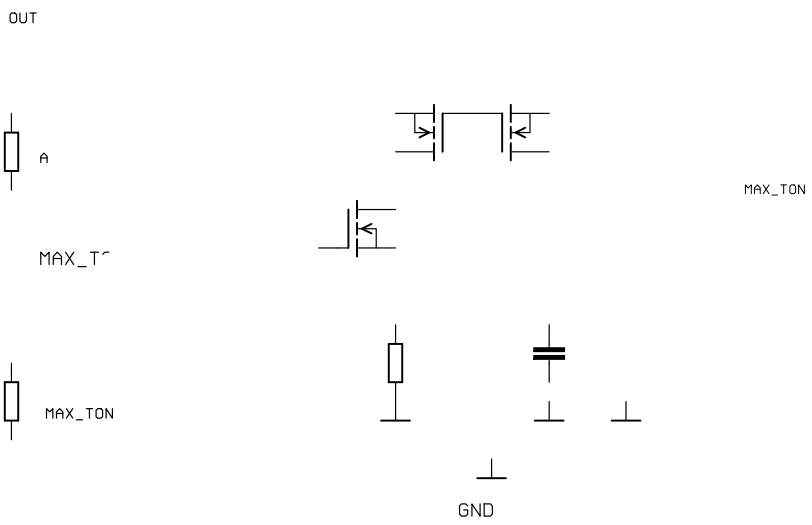


Figure 49. Internal Connection of the MAX_TON Generator, NCP4308Q

Power Dissipation Calculation

It is important to consider the power dissipation in the MOSFET driver of a SR system. If no external gate resistor is used and the internal gate resistance of the MOSFET is very low, nearly all energy losses related to gate charge are dissipated in the driver. Thus it is necessary to check the SR driver power losses in the target application to avoid over temperature and to optimize efficiency.

In SR systems the body diode of the SR MOSFET starts conducting before SR MOSFET is turned−on, because there is some delay from $V_{TH_CS_ON}$ detect to turn−on the driver. On the other hand, the SR MOSFET turn off process always starts before the drain to source voltage rises up significantly. Therefore, the MOSFET switch always operates under Zero Voltage Switching (ZVS) conditions when in a synchronous rectification system.

The following steps show how to approximately calculate the power dissipation and DIE temperature of the NCP4308 controller. Note that real results can vary due to the effects of the PCB layout on the thermal resistance.

Step 1 − MOSFET Gate−to Source Capacitance:

During ZVS operation the gate to drain capacitance does not have a Miller effect like in hard switching systems because the drain to source voltage does not change (or its wwIm8 Do3 3 284.2583 75008 Tm-862 6 Tc108TjET2918

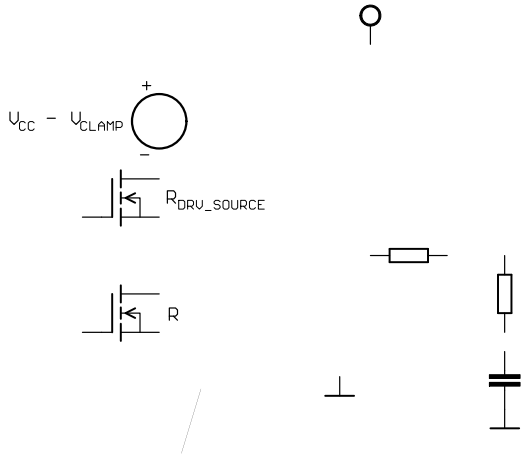


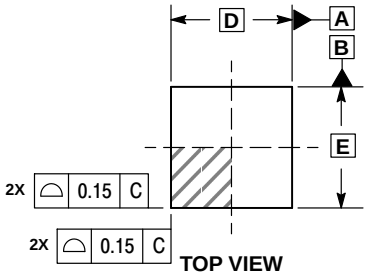
Figure 52. Equivalent Schematic of Gate Drive Circuitry

PRODUCT OPTIONS

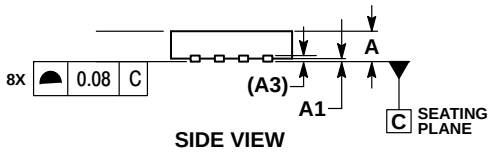
OPN	Package	UVLO [V]	DRV clamp [V]	Pin 5 function	Usage
NCP4308ADR2G	SOIC8	4.5	4.7	NC	LLC, CCM flyback, DCM flyback, QR, QR with primary side CCM control
NCP4308AMTTWG	WDFN8	4.5	4.7	NC	
NCP4308DDR2G	SOIC8	4.5	9.5	NC	
NCP4308DMNTWG	DFN8	4.5	9.5	NC	
NCP4308DMTTWG	WDFN8	4.5	9.5	NC	
NCP4308QDR2G	SOIC8	4.5			

DFN8, 4x4
CASE 488AF
ISSUE C

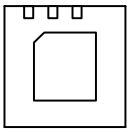
DATE 15 JAN 2009



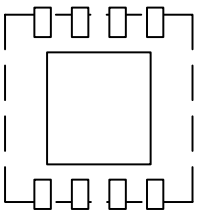
TOP VIEW



SIDE VIEW

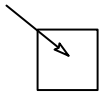


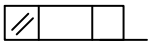
BOTTOM VIEW

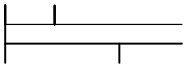


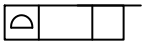
NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS.

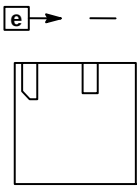
	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	1.91	2.21
E	4.00 BSC	
E2	2.09	2.39
e	0.80 BSC	
K	0.20	---
L	0.30	0.50







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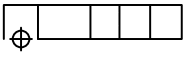

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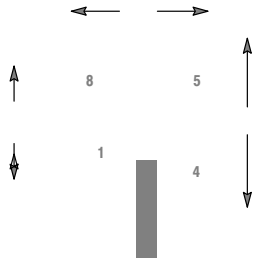

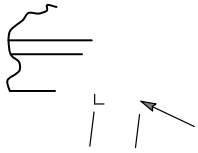

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