C 43080

www.onsemi.com

The NCP43080 is a synchronous rectifier controller for switch mode power supplies. The controller enables high efficiency designs for flyback and quasi resonant flyback topologies.

Externally adjustable minimum off−time and on−time blanking periods provides flexibility to drive various MOSFET package types and PCB layout. A reliable and noise less operation of the SR system is insured due to the Self Synchronization feature. The NCP43080 also utilizes Kelvin connection of the driver to the MOSFET to achieve high efficiency operation at full load and utilizes a light load detection architecture to achieve high efficiency at light load.

The precise turn−off threshold, extremely low turn−off delay time and high sink current capability of the driver allow the maximum synchronous rectification MOSFET conduction time. The high accuracy driver and 5 V gate clamp make it ideally suited for directly driving GaN devices.

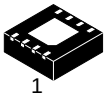
Features

- Self−Contained Control of Synchronous Rectifier in CCM, DCM and QR for Flyback, Forward or LLC Applications
- Precise True Secondary Zero Current Detection
- Rugged Current Sense Pin (up to 150 V)
- Adjustable Minimum ON−Time
- Adjustable Minimum OFF-Time with Ringing Detection
- Adjustable Maximum ON−Time for CCM Controlling of Primary QR Controller
- Improved Robust Self Synchronization Capability
- 8 A / 4 A Peak Current Sink / Source Drive Capability
- Operating Voltage Range up to V_{CC} = 35 V
- Automatic Light−load & Disable Mode
- Adaptive Gate Drive Clamp
- GaN Transistor Driving Capability (options A and C)
- Low Startup and Disable Current Consumption
- Maximum Operation Frequency up to 1 MHz
- SOIC-8 and DFN−8 (4x4) and WDFN8 (2x2) Packages
- These are Pb−Free Devices

Typical Applications

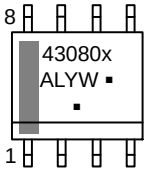
- Notebook Adapters
- High Power Density AC/DC Power Supplies (Cell Phone Chargers)
- LCD TVs
- All SMPS with High Efficiency Requirements

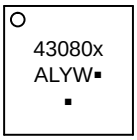
SOIC−8
D SUFFIX
CASE 751



DFN8
MN SUFFIX
CASE 488AF

MARKING DIAGRAMS





43080x	= Specific Device Code x = A, B, C, D or Q
Fx	= Specific Device Code x = A or D
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
M	= Date Code
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 33 of this data sheet.

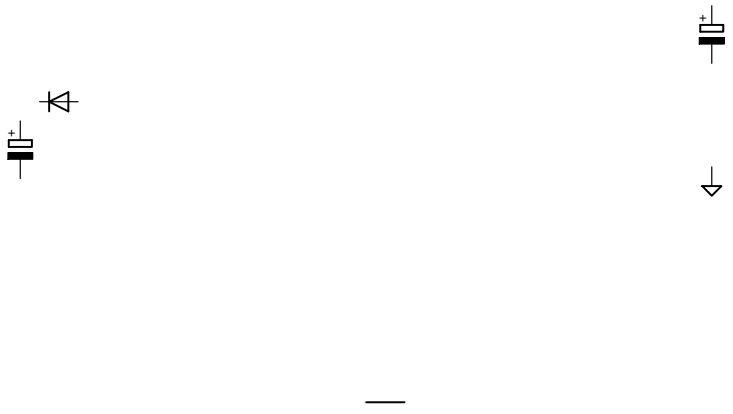


Figure 3. Typical Application Example − Primary Side Flyback Converter with optional LLD

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to 37.0	V
MIN_TON, MIN_TOFF, MAX_TON, LLD Input Voltage	V_{MIN_TON}, V_{MIN_TOFF}, V_{MAX_TON}, V_{LLD}		

Turn On CS Threshold Voltage		$V_{TH\_CS\_ON}$	−120	−75
Turn Off CS Threshold Voltage	Guaranteed by Design	$V_{TH\_CS\_OFF}$	−1	
Turn Off Timer Reset Threshold		$V_{TH\_CS\_RESET}$	0.4	0.5

0.5

ELECTRICAL CHARACTERISTICS

$-40°C \le T_J \le 125°C$; V_{CC} = 12 V; C_{DRV} = 0 nF; $R_{MIN\_TON} = R_{MIN\_TOFF}$ = 10 kΩ; V_{LLD} = 0 V; V_{CS} = −1 to +4 V; f_{CS} = 100 kHz, DC_{CS} = 50%, unless otherwise noted. Typical values are at T_J = +25°C

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
MAXIMUM t_{ON} ADJUST						
Maximum t_{ON} Time	V_{MAX_TON} = 3 V	t_{ON_MAX}	4.3	4.8	5.3	μs
Maximum t_{ON} Time	V_{MAX_TON} = 0.3 V	t_{ON_MAX}	41	48	55	μs
Maximum t_{ON} Output Current	V_{MAX_TON} = 0.3 V, V_{CS} = 0 V	I_{MAX_TON}	−105	−100	−95	μA
LLD INPUT						
Disable Threshold	$V_{LLD\_DIS} = V_{CC} - V_{LLD}$	V_{LLD_DIS}	0.8	0.9	1.0	V
Recovery Threshold						

TYPICAL CHARACTERISTICS

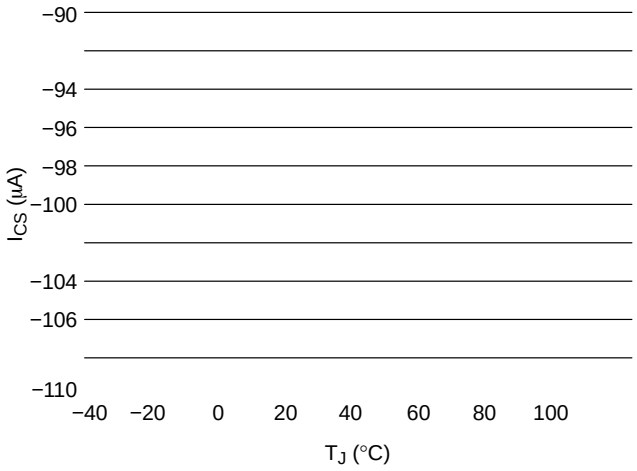


Figure 14. CS Current, V_{CS} = −20 mV

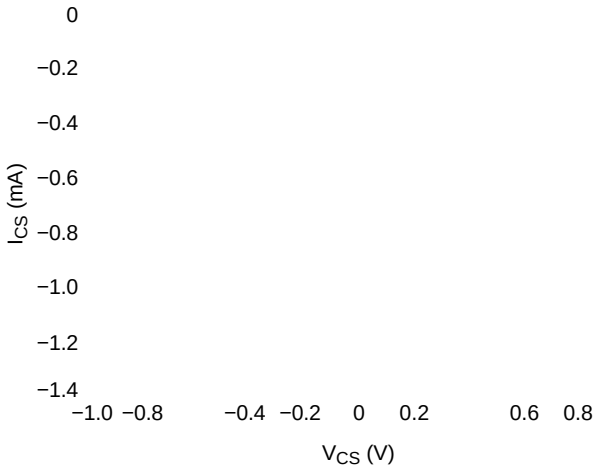


Figure 15. CS Current, V_{CC} = 12 V

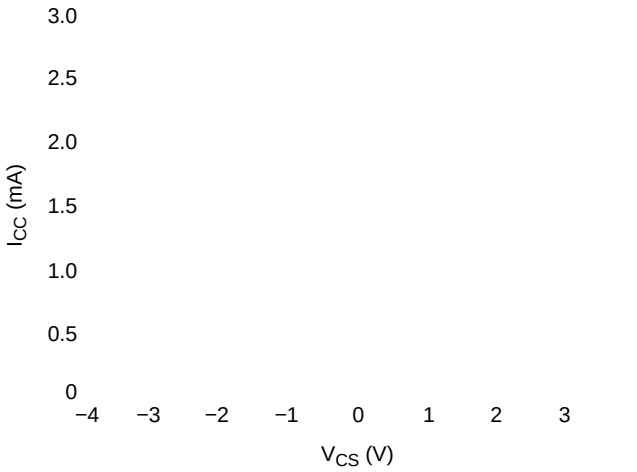


Figure 16. Supply Current vs. CS Voltage, V_{CC} = 12 V

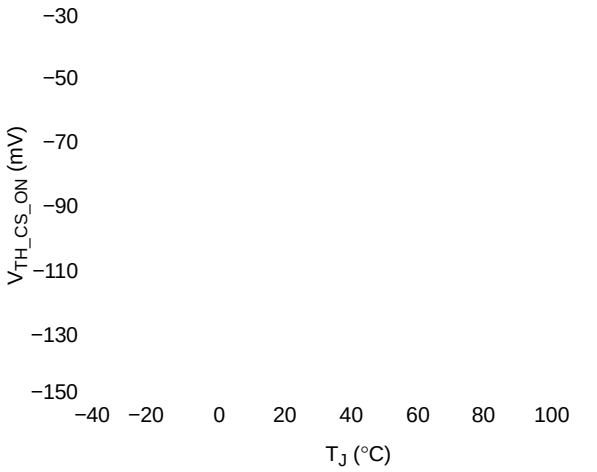


Figure 17. CS Turn−on Threshold

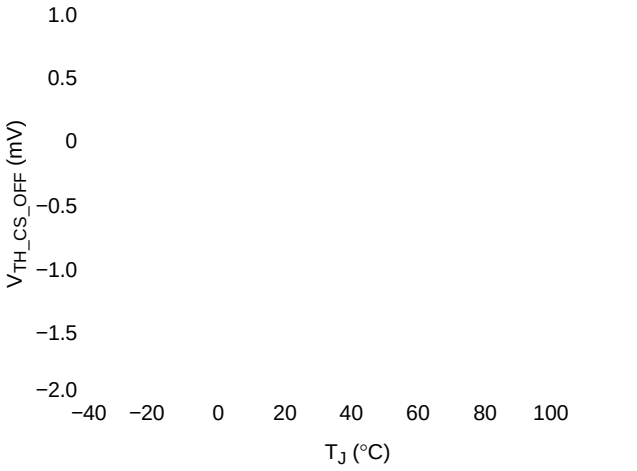


Figure 18. CS Turn−off Threshold

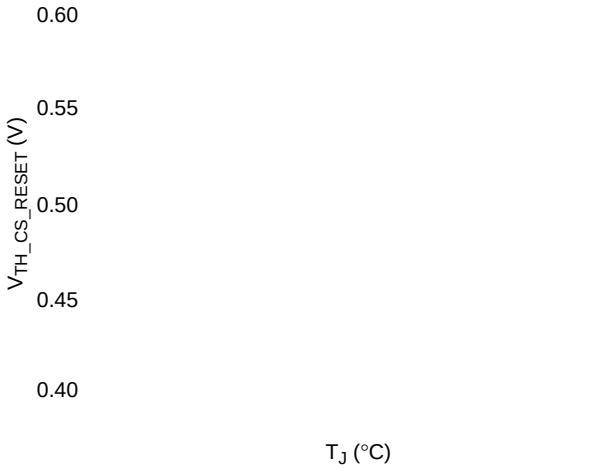


Figure 19. CS Reset Threshold

TYPICAL CHARACTERISTICS

T_J (°C)

Figure 26. Minimum On−time R_{MIN_TON} = 50 kΩ

T_JT

Figure 27. Minimum Off−time R_{MIN_TOFF} = 0 Ω

TYPICAL CHARACTERISTICS

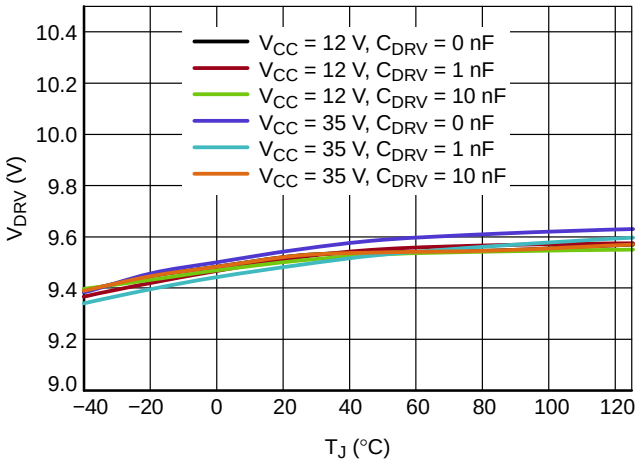


Figure 32. Driver and Output Voltage, ver. B, D and Q

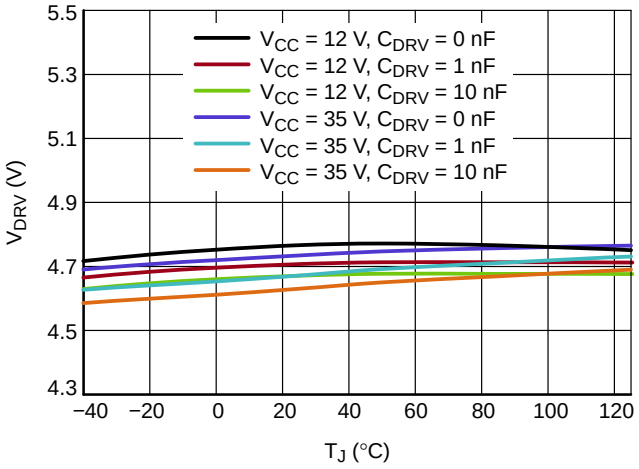


Figure 33. Driver Output Voltage, ver. A and C

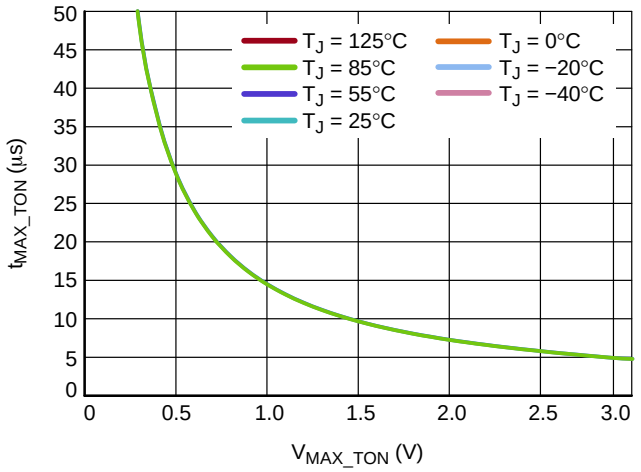


Figure 34. Maximum On−time, ver. Q

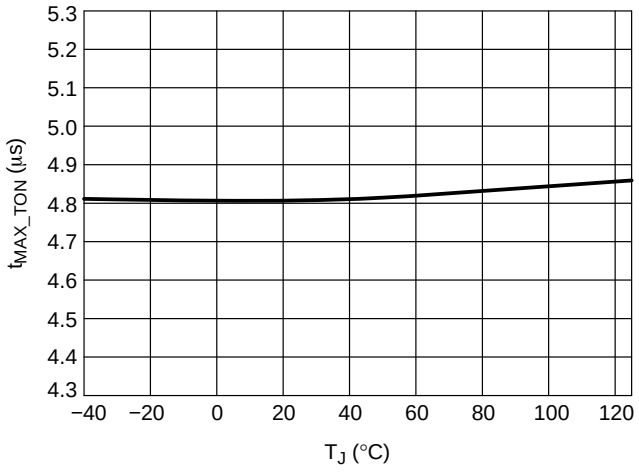


Figure 35. Maximum On−time, V_{MAX_TON} = 3 V, ver. Q

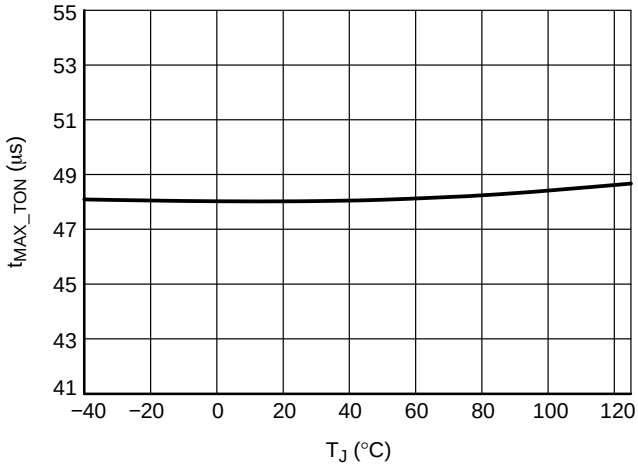


Figure 36. Maximum On−time, V_{MAX_TON} = 0.3 V, ver. Q

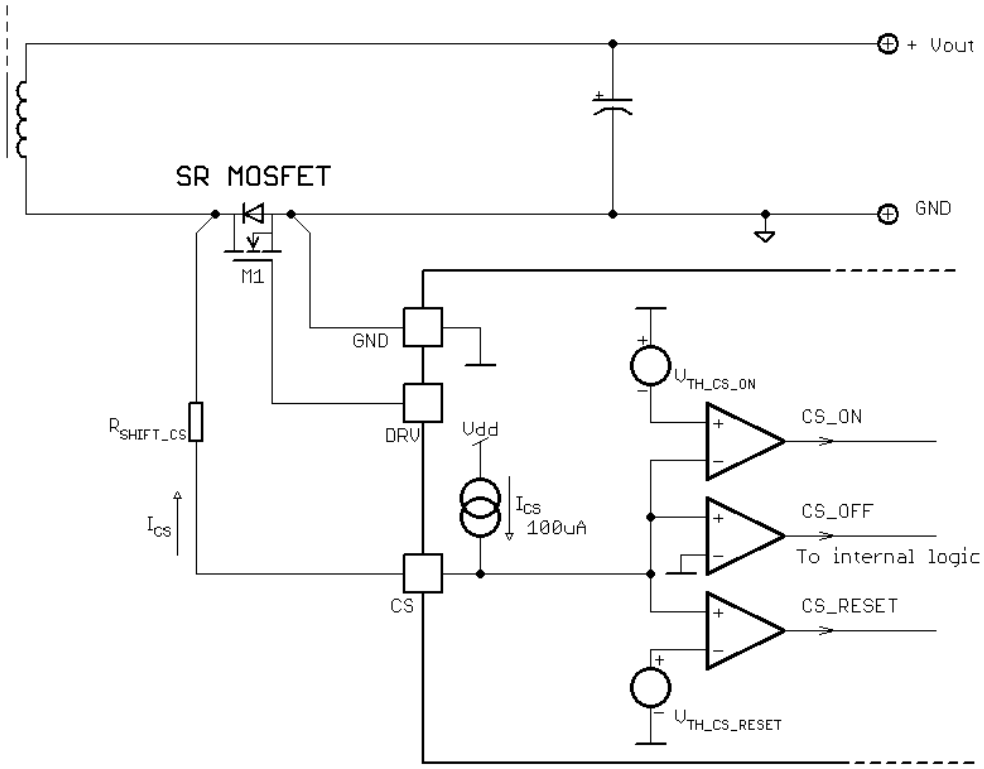
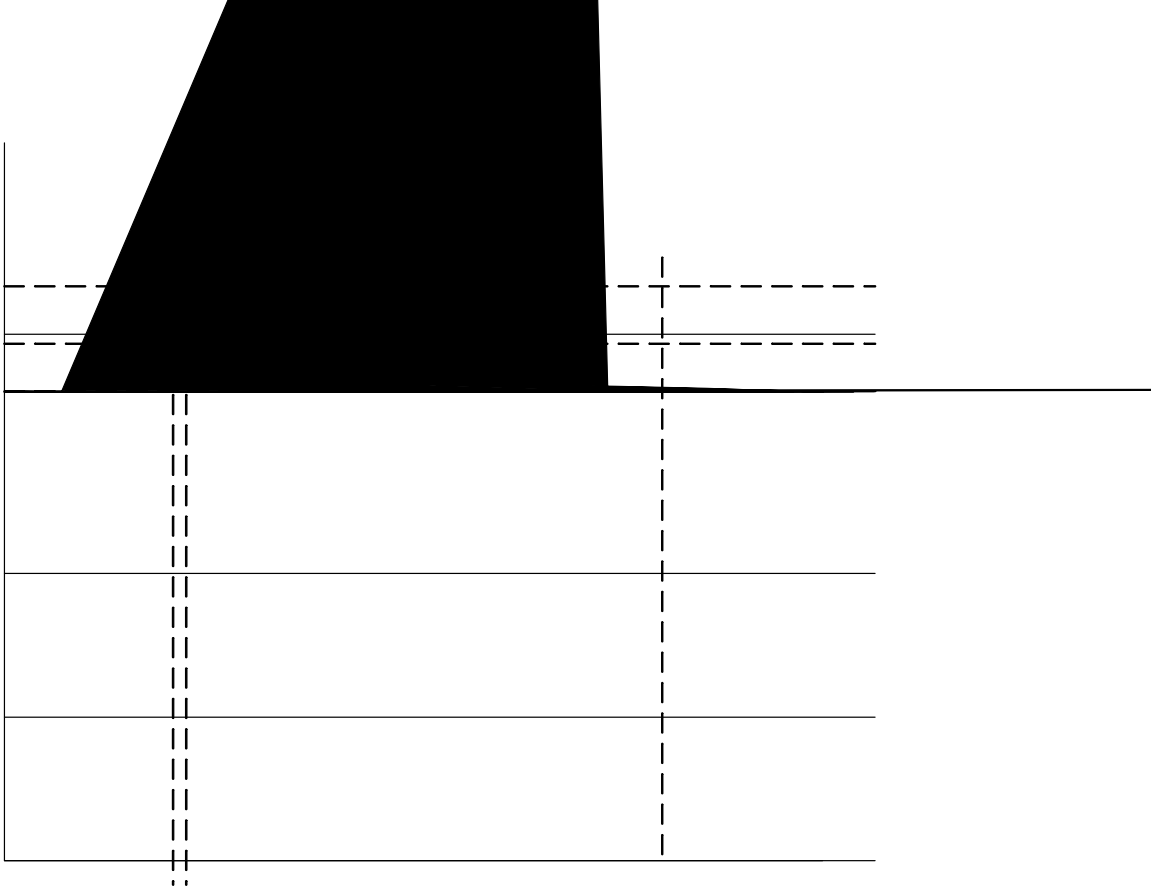


Figure 37. Current Sensing Circuitry Functionality

The SR MOSFET is turned-off as soon as the voltage on the CS pin is higher than $V_{TH\_CS\_OFF}$ (typically −0.5 mV minus any voltage dropped on the optional R_{SHIFT_CS}). For the same ringing reason, a minimum off-time timer is asserted once the V_{CS} goes above $V_{TH\_CS\_RESET}$. The minimum off-time can be externally adjusted using R_{MIN_TOFF} resistor. The minimum off−time generator can be re−triggered by MIN_TOFF reset comparator if some spurious ringing occurs on the CS input after SR MOSFET turn−off event. This feature significantly simplifies SR system implementation in flyback converters.

In an LLC converter the SR MOSFET M1 channel conducts while secondary side current is decreasing (refer to Figure 38). Therefore the turn−off current depends on MOSFET R_{DSON}. The −0.5 mV threshold provides an optimum switching period usage while keeping enough time margin for the gate turn-off. The R_{SHIFT_CS} resistor provides the designer with the possibility to modify (increase) the actual turn−on and turn−off secondary current thresholds. To ensure proper switching, the min_t_{OFF} timer is reset, when the V_{DS} of the MOSFET rings and falls down past the $V_{TH\_CS\_RESET}$. The minimum off−time needs to expire before another drive pulse can be initiated. Minimum off−time timer is started again when V_{DS} rises above $V_{TH\_CS\_RESET}$.



If no R_{SHIFT_CS} resistor is used, the turn-on, turn-

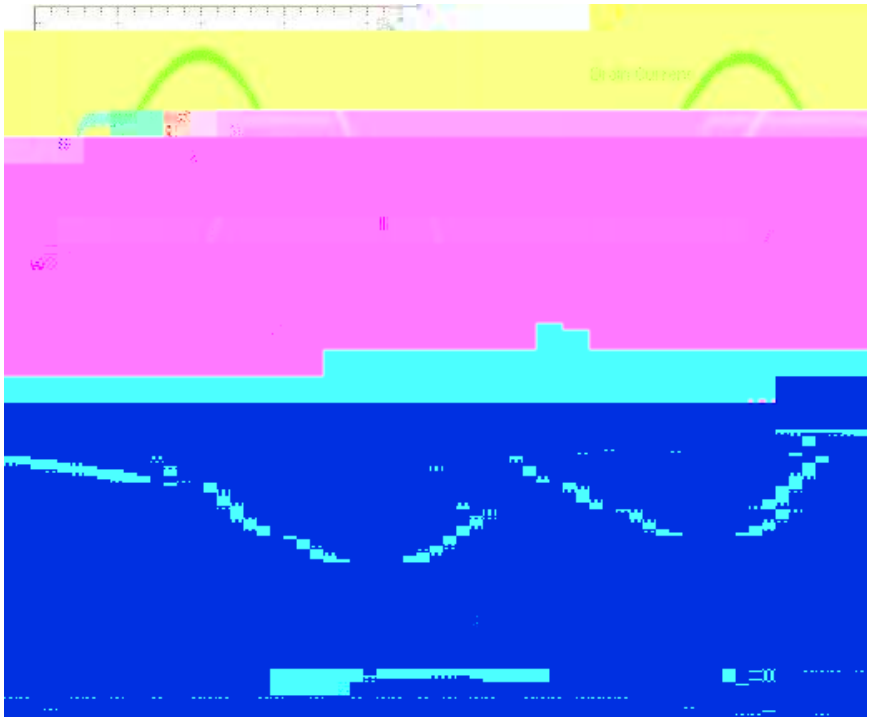


Figure 41. Waveforms From SR System Implemented in LLC Application and Using MOSFET in TO220 Package With Long Leads − SR MOSFET channel Conduction Time is Reduced

Note that the efficiency impact caused by the error voltage due to the parasitic inductance increases with lower MOSFETs $R_{DS(on)}$ and/or higher operating frequency.

It is thus beneficial to minimize SR MOSFET package leads length in order to maximize application efficiency. The optimum solution for applications with high secondary current $\Delta i/\Delta t$ and high operating frequency is to use lead−less SR MOSFET i.e. SR MOSFET in SMT package. The parasitic inductance of a SMT package is negligible causing insignificant CS turn−off threshold shift and thus minimum impact to efficiency (refer to Figure 42).

Figure 42. Waveforms from SR System Implemented in LLC Application and Using MOSFET in SMT Package with Minimized Parasitic Inductance − SR MOSFET Channel Conduction Time is Optimized

It can be deduced from the above paragraphs on the induced error voltage and parameter tables that turn−off threshold precision is quite critical. If we consider a SR MOSFET with $R_{DS(on)}$ of 1 mΩ, the 1 mV error voltage on the CS pin results in a 1 A turn-off current threshold difference; thus the PCB layout is very critical when implementing the SR system. Note that the CS turn-off comparator is referred to the GND pin. Any parasitic impedance (resistive or inductive − even on the magnitude of mΩ and nH values) can cause a high error voltage that is then evaluated by the CS comparator. Ideally the CS turn−off comparator should detect voltage that is caused by secondary current directly on the SR MOSFET channel resistance. In reality there will be small parasitic impedance on the CS path due to the bonding wires, leads and soldering. To assure the best efficiency results, a Kelvin connection of the SR controller to the power circuitry should be implemented. The GND pin should be connected to the SR MOSFET source soldering point and current sense pin should be connected to the SR MOSFET drain soldering point − refer to Figure 40. Using a Kelvin connection will avoid any impact of PCB layout parasitic elements on the SR controller functionality; SR MOSFET parasitic elements will still play a role in attaining an error voltage. Figure 44 and Figure 43 show examples of SR system layouts using MOSFETs in TO220 and SMT packages. It is evident that the MOSFET leads should be as short as possible to minimize parasitic inductances when using packages with leads (like TO220). Figure 43 shows how to layout design with two SR MOSFETs in parallel. It has to be noted that it is not easy task and designer has to paid lot of attention to do symmetric Kelvin connection.

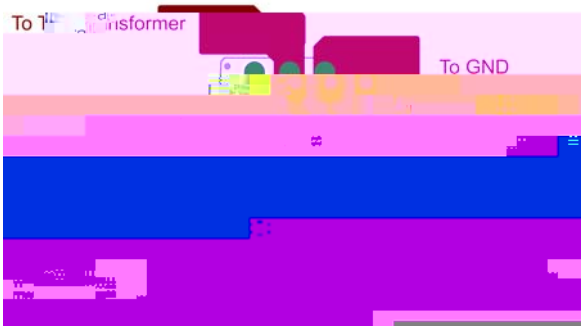


Figure 44. Recommended Layout When Using SR MOSFET in TO220 Package

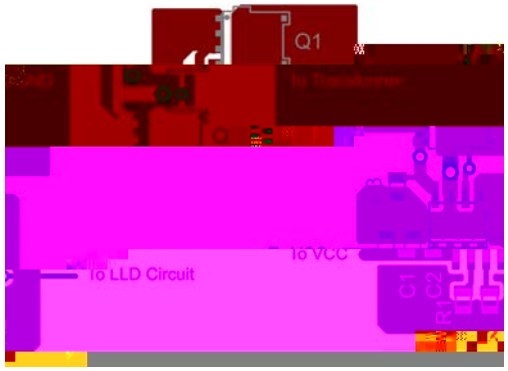


Figure 43. Recommended Layout When Using SR MOSFET in SMT Package (2x SO8 FL)

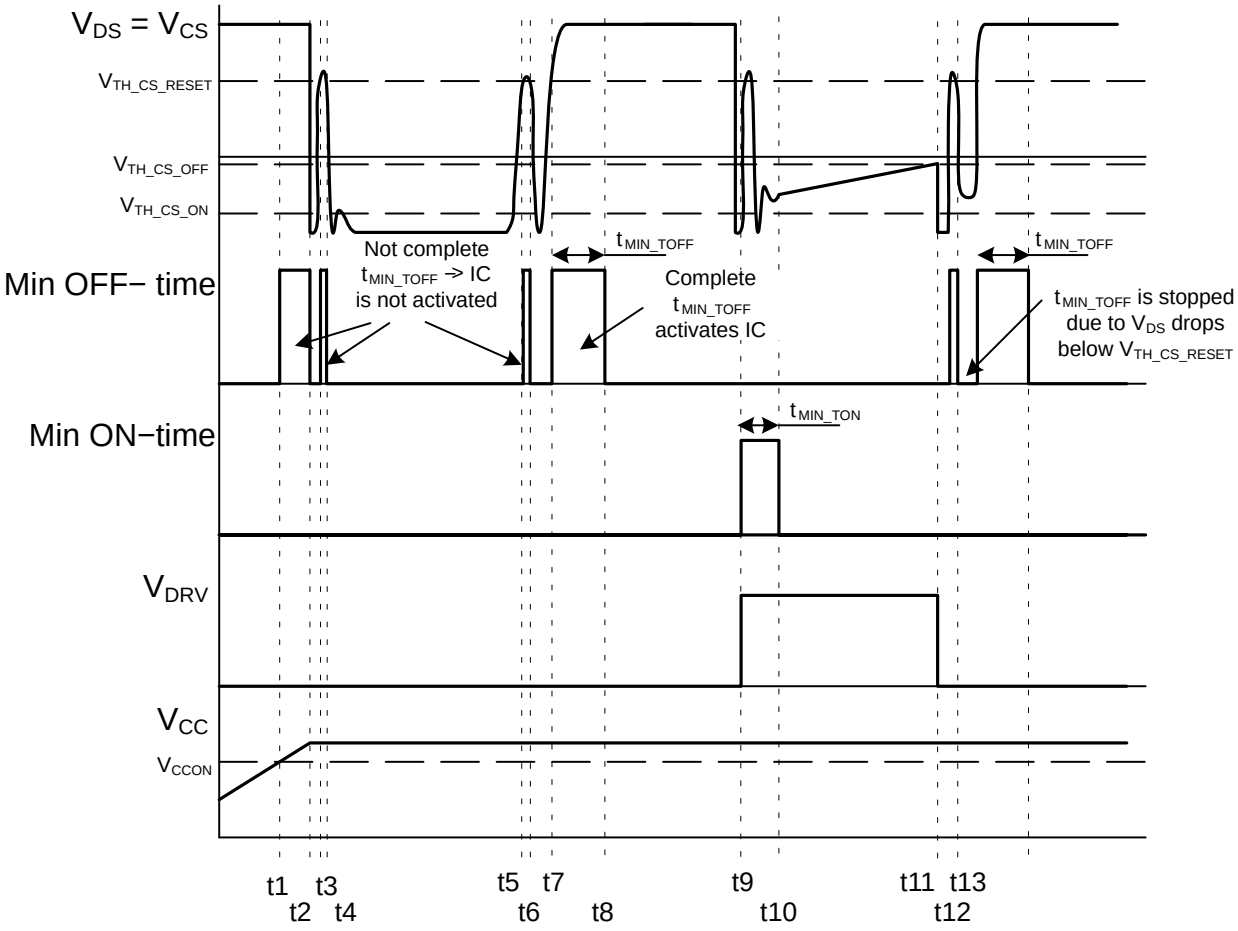


Figure 45. NCP43080 Operation after Start−Up Event

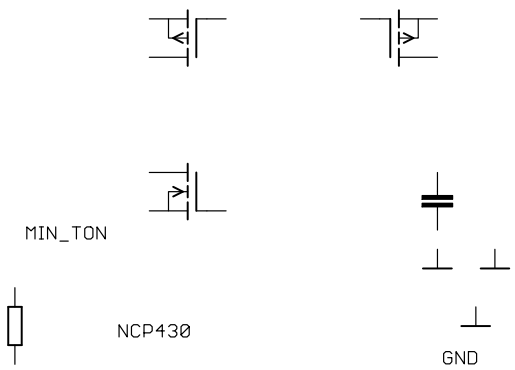


Figure 46. Internal Connection of the MIN_TON Generator (the MIN_TOFF Works in the Same Way)

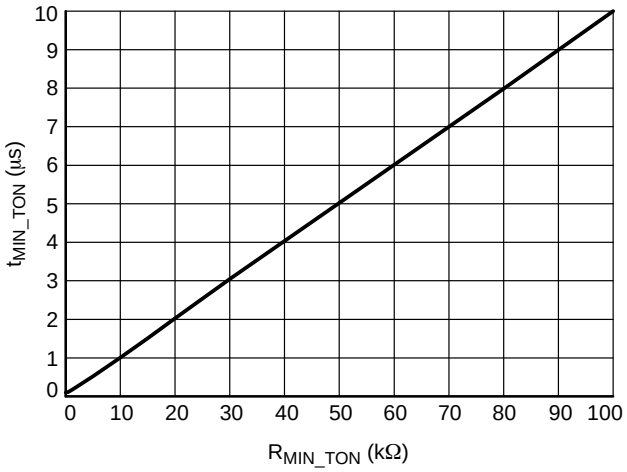


Figure 47. MIN_TON Adjust Characteristics

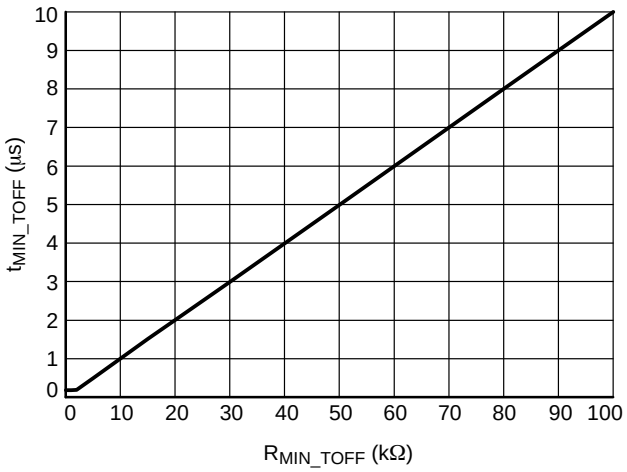


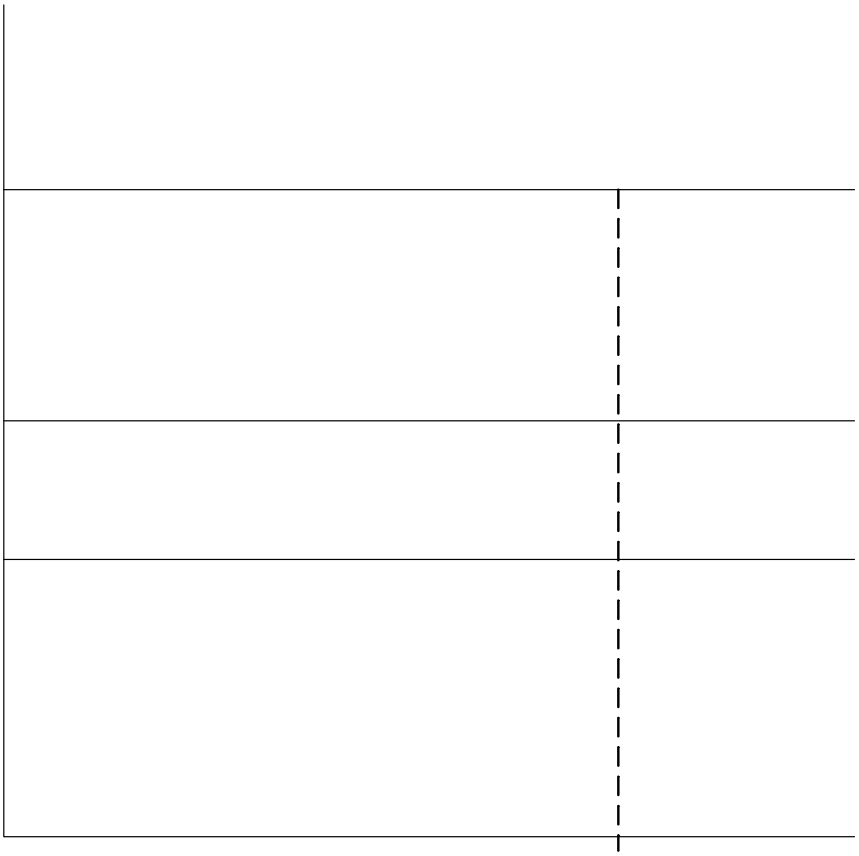
Figure 48. MIN_TOFF Adjust Characteristics

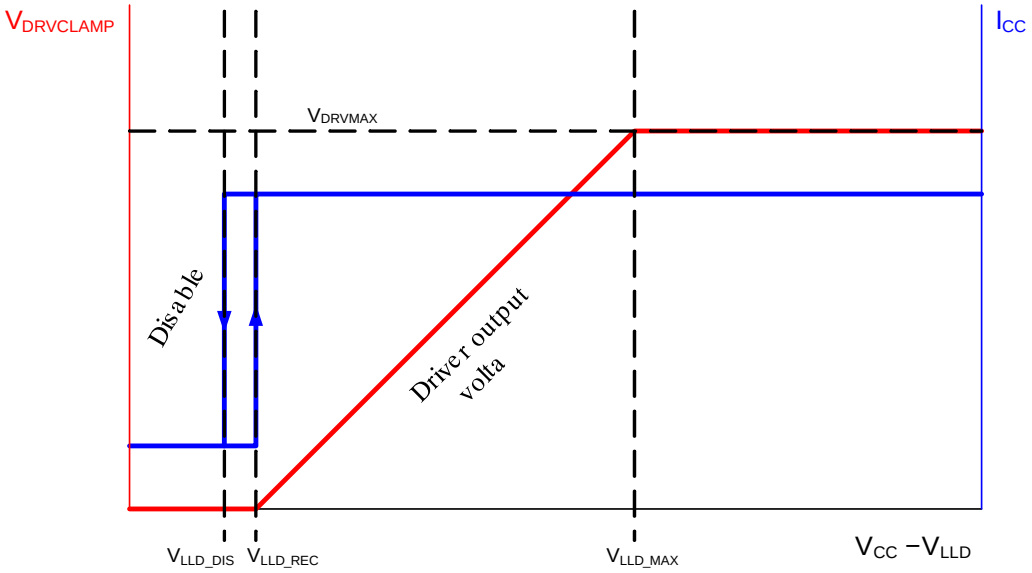
The absolute minimum t_{ON} duration is internally clamped to 55 ns and minimum t_{OFF}

Maximum t_{ON} adjustment

The NCP43080Q offers an adjustable maximum on−time (like the min_t_{ON} and min_t_{OFF} settings shown above) that can be very useful for QR controllers at high loads. Under high load conditions the QR controller can operate in CCM thanks to this feature. The NCP43080Q version has the ability to turn−off the DRV signal to the SR MOSFET before the secondary side current reaches zero. The DRV signal from the NCP43080Q can be fed to the primary side through a pulse transformer (see Figure 4 for detail) to a transistor on the primary side to emulate a ZCD event before an actual ZCD event occurs. This feature helps to keep the minimum switching frequency up so that there is better energy transfer through the transformer (a smaller transformer core can be used). Also another advantage is that the IC controls the SR MOSFET and turns off from secondary side before the primary side is turned on in CCM to ensure no cross conduction. By controlling the SR MOSFET's turn off before the primary side turn off, producing a zero cross conduction operation, this will improve efficiency.

The Internal connection of the MAX_TON feature is shown in Figure 50. Figure 50 shows a method that allows for a modification of the maximum on−time according to




VDRVCLAMP
ICC
VDRVMAX
Disable
Driver output volta
VLLD_DIS
VLLD_REC
VLLD_MAX
VCC −VLLD

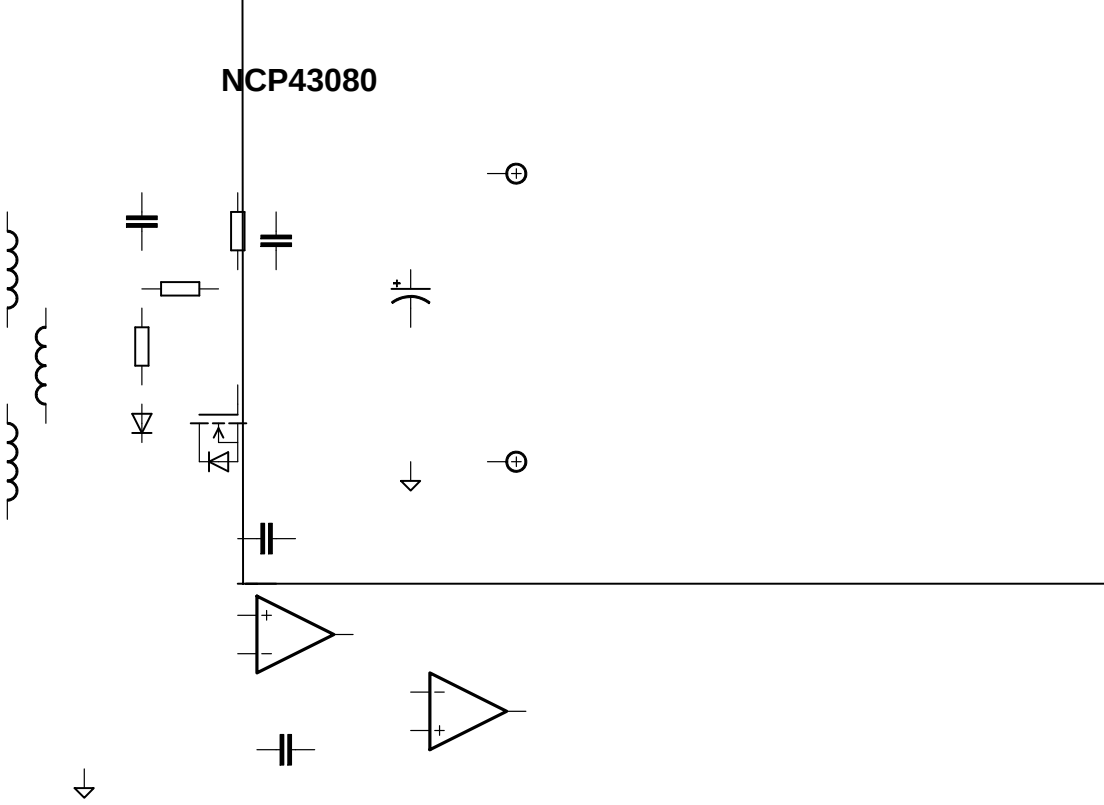


Figure 54. NCP43080 Light Load and No Load Detection Principle in Flyback Topologies

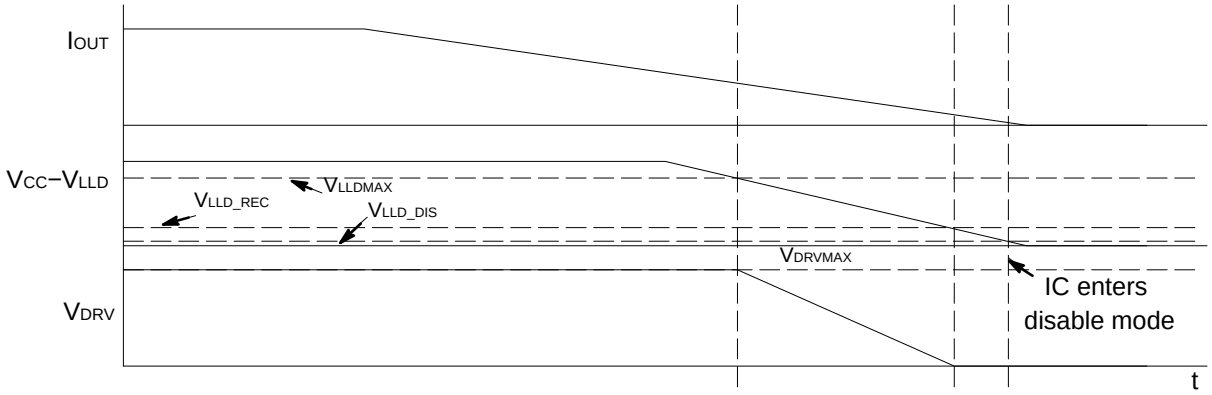
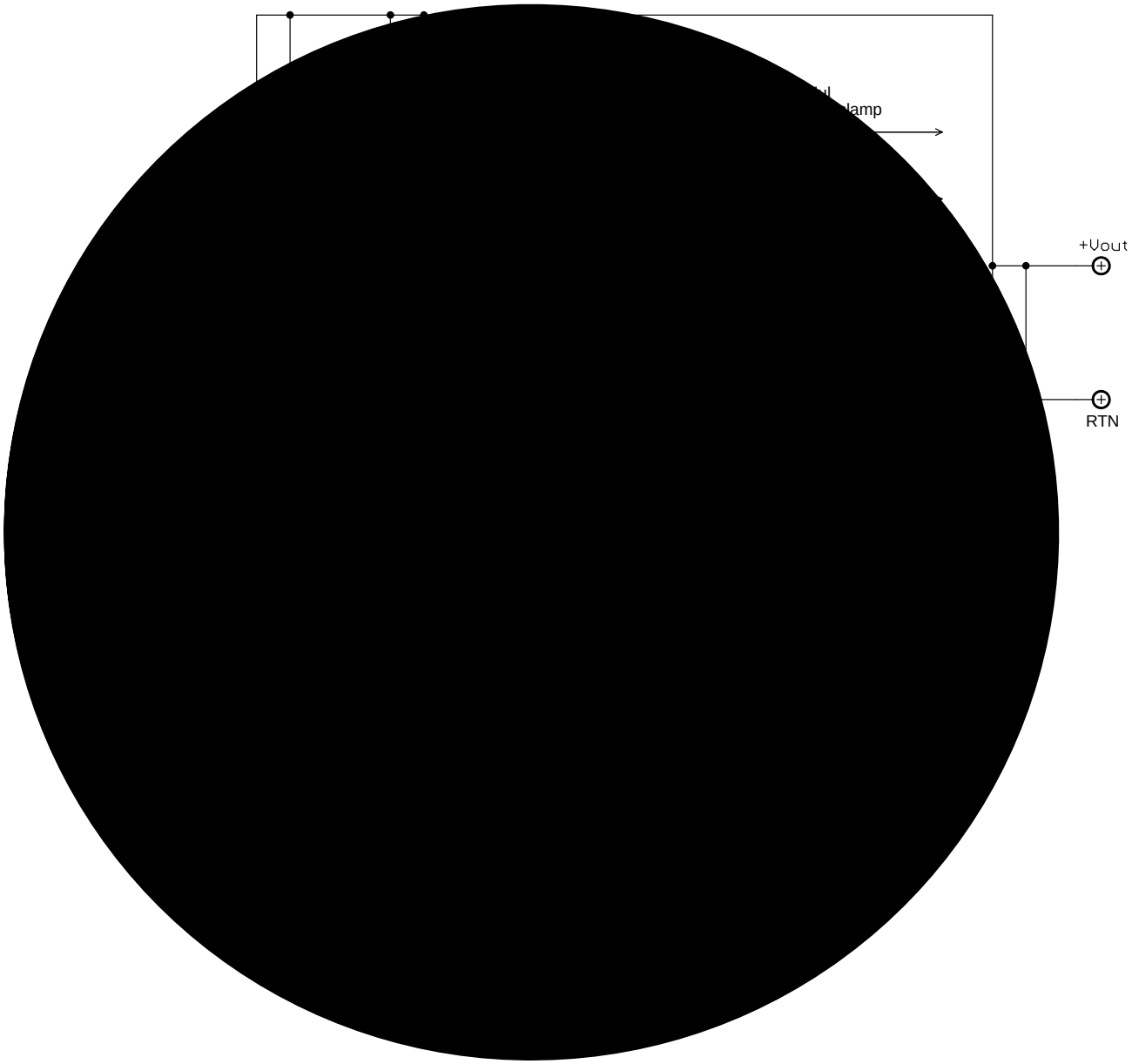


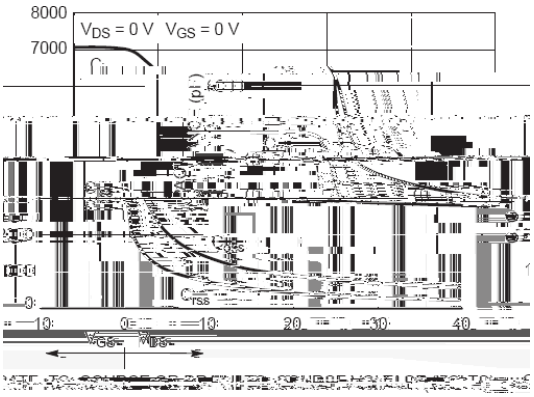
Figure 56. NCP43080 Driver Clamp Modulation Circuitry Transfer Characteristic in Flyback Application

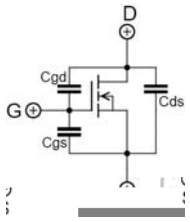
The technique used for LLD detection in LLC is similar to the LLD detection method used in a flyback with the exception the D1 and D2 OR−ing diodes are used to measure the total duty cycle to see if it is operating in skip mode.



There exist some LLC applications where behavior described above is not the best choice. These applications transfer significant portion of energy in a few first pulses in skip burst. It is good to keep SR fully working during skip mode to improve efficiency. There can be still saved some energy using LLD function by activation disable mode between skip bursts. Simplified schematic for this LLD behavior is shown in Figure 60. Operation waveforms for this option are provided in Figure 61. Capacitor C2 is charged to maximum voltage when LLC is switching. When there is no switching in skip, capacitor C2 is discharged by R2 and when LLD voltage referenced to VCC falls below V_{LLD_DIS}

V





$$C_{iss} = C_{gs} + C_{gd}$$

$$C_{rss} = C_{gd}$$

$$C_{oss} = C_{ds} + C_{gd}$$

Figure 62. Typical MOSFET Capacitances Dependency on V_{DS} and V_{GS} Voltages

Therefore, the input capacitance of a MOSFET operating in ZVS mode is given by the parallel combination of the gate to source and gate to drain capacitances (i.e. C_{iss} capacitance for given gate to source voltage). The total gate charge, Q_{g_total}, of most MOSFETs on the market is defined for hard switching conditions. In order to accurately calculate the driving losses in a SR system, it is necessary to determine the gate charge of the MOSFET for operation specifically in a ZVS system. Some manufacturers define this parameter as Q_{g_ZVS}. Unfortunately, most datasheets do not provide this data. If the C_{iss} (or Q_{g_ZVS}) parameter is not available then it will need to be measured. Please note that the input capacitance is not linear (as shown Figure 62) and it needs to be characterized for a given gate voltage clamp level.

Step 2 − Gate Drive Losses Calculation:

Gate drive losses are affected by the gate driver clamp voltage. Gate driver clamp voltage selection depends on the type of MOSFET used (threshold voltage versus channel resistance). The total power losses (driving loses and conduction losses) should be considered when selecting the gate driver clamp voltage. Most of today's MOSFETs for SR systems feature low $R_{DS(on)}$ for 5 V V_{GS} voltage. The NCP43080 offers both a 5 V gate clamp and a 10 V gate clamp for those MOSFET that require higher gate to source voltage.

The total driving loss can be calculated using the selected gate driver clamp voltage and the input capacitance of the MOSFET:

$$P_{DRV\_total} = V_{CC} \cdot V_{CLAMP} \cdot C_{g\_ZVS} \cdot f_{SW} \quad \text{(eq. 9)}$$

Where:

V_{CC}	is the NCP43080 supply voltage
V_{CLAMP}	is the driver clamp voltage
C_{g_ZVS}	is the gate to source capacitance of the MOSFET in ZVS mode
f_{sw}	is the switching frequency of the target application

The total driving power loss won't only be dissipated in the IC, but also in external resistances like the external gate resistor (if used) and the MOSFET internal gate resistance (Figure 44). Because NCP43080 features a clamped driver, it's high side portion can be modeled as a regular driver switch with equivalent resistance and a series voltage source. The low side driver switch resistance does not drop immediately at turn−off, thus it is necessary to use an equivalent value ($R_{DRV\_SIN\_EQ}$) for calculations. This method simplifies power losses calculations and still provides acceptable accuracy. Internal driver power dissipation can then be calculated using Equation 10:

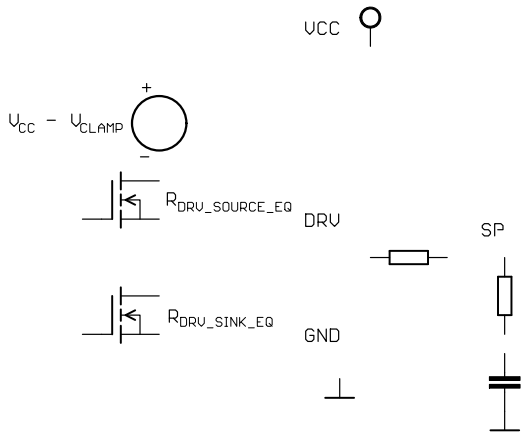


Figure 63. Equivalent Schematic of Gate Drive Circuitry

PRODUCT OPTIONS

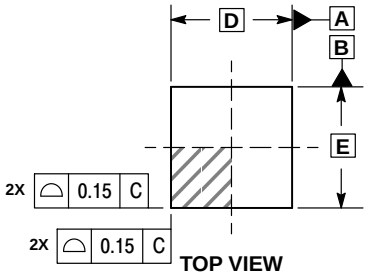
OPN	Package	UVLO [V]	DRV clamp [V]	Pin 5 function	Usage
NCP43080ADR2G	SOIC8	4.5	4.7	NC	LLC, CCM flyback, DCM flyback, forward, QR, QR with primary side CCM control
NCP43080AMTTWG	WDFN8	4.5	4.7	NC	
NCP43080DDR2G	SOIC8	4.5	9.5	NC	
NCP43080DMNTWG	DFN8	4.5	9.5	NC	
NCP43080DMTTWG	WDFN8	4.5	9.5	NC	
NCP43080QDR2G	SOIC8	4.5	9.5	MAX_TON	QR with forced CCM from secondary side

ORDERING INFORMATION

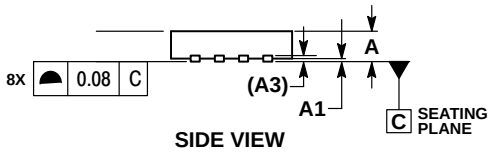
Device	Package	Package marking	Packing	Shipping†
NCP43080ADR2G	SOIC8	43080A	SOIC−8 (Pb−Free)	2500 /Tape & Reel
NCP43080DDR2G		43080D		
NCP43080QDR2G		43080Q		
NCP43080AMTTWG	WDFN8	FA	WDFN−8 (Pb−Free)	3000 /Tape & Reel
NCP43080DMTTWG		FD		
NCP43080DMNTWG	DFN8	43080D	DFN−8 (Pb−Free)	4000 /Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DFN8, 4x4

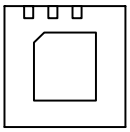


TOP VIEW

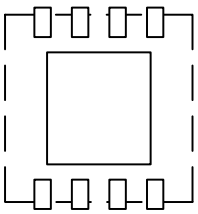


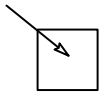
SIDE VIEW

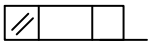
DIM	MILLIMETERS MIN	MAX
A		
A1		
A3		
b		
D		
D2		
E		
E2		
e		
K		---
L		

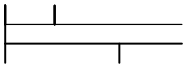


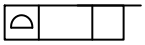
BOTTOM VIEW



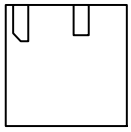


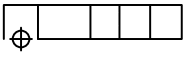






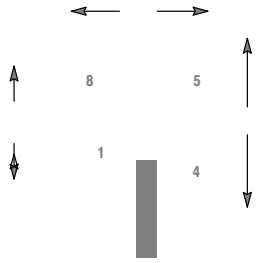

e

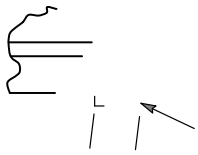




SOIC 8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011





SEATING
PLANE