Table 1. PIN DESCRIPTION

Pin	Name	Function
1, 9	V_{IN}	Drain of MOSFET (0.5 V – 13.5 V), Pin 1 must be connected to Pin 9
2	EN	NCP45520−H & NCP45521−H − Active−

Table 3. OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3	5.5	V
Input Voltage	V_{IN}	0.5	13.5	V
Ground	GND		0	V
Ambient Temperature	T_A	−40	85	C
Junction Temperature	T_J	−40	125	C
OFF to ON Transition Energy Dissipation Limit (See application section)	E_{TRANS}	0	100	mJ

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS (T_J = 25 C unless otherwise specified)

Parameter	Conditions (Note 7)	Symbol	Min	Typ	Max	Unit
MOSFET						
On−Resistance	V_{CC} = 3.3 V; V_{IN} = 1.8 V	R_{ON}		9.5	12.7	mΩ
	V_{CC} = 3.3 V; V_{IN} = 5 V			10.1	13.9	
	V_{CC} = 3.3 V; V_{IN} = 12 V			12.8	22.5	
Leakage Current (Note 8)	V_{EN}= 3.3 V; V					

TYPICAL CHARACTERISTICS

(T_J = 25

TYPICAL CHARACTERISTICS

(T_J = 25 C UNLESS OTHERWISE SPECIFIED)

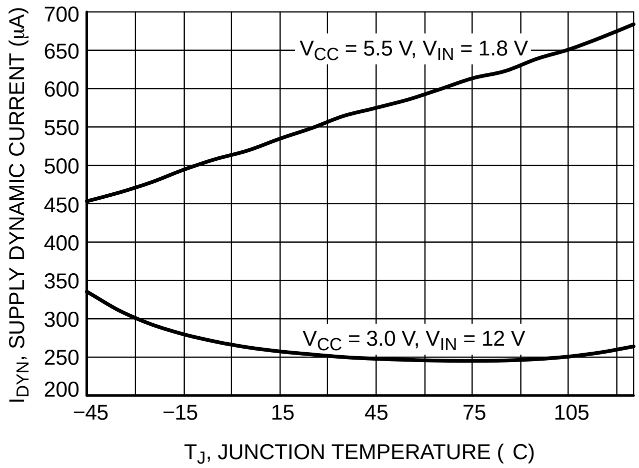


Figure 9. Supply Dynamic Current vs. Temperature

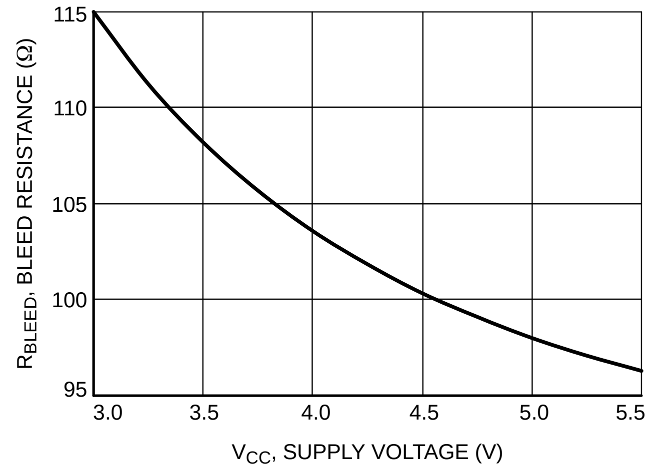


Figure 10. Bleed Resistance vs. Supply Voltage

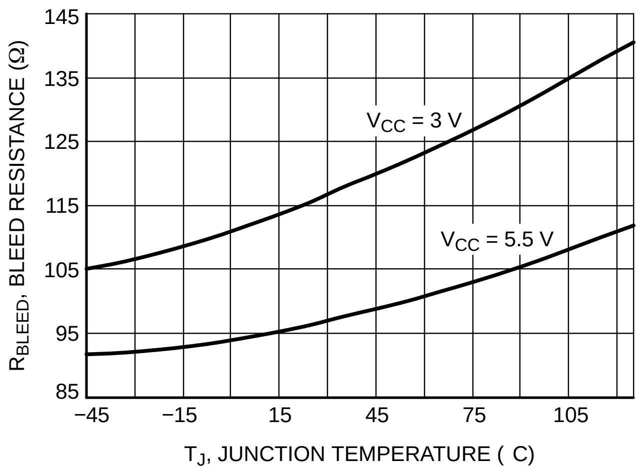


Figure 11. Bleed Resistance vs. Temperature

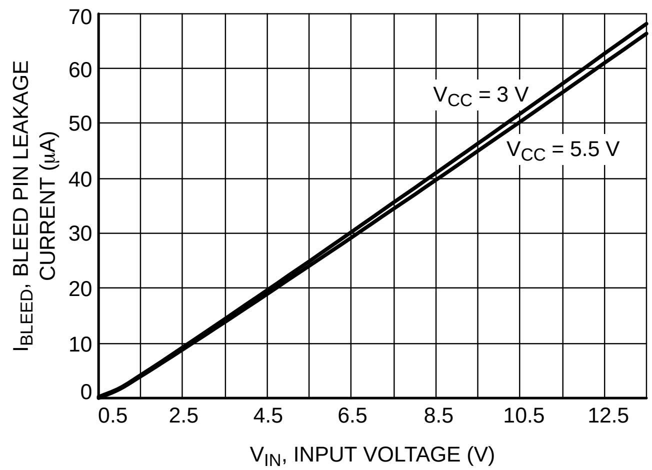


Figure 12. Bleed Pin Leakage Current vs. Input Voltage

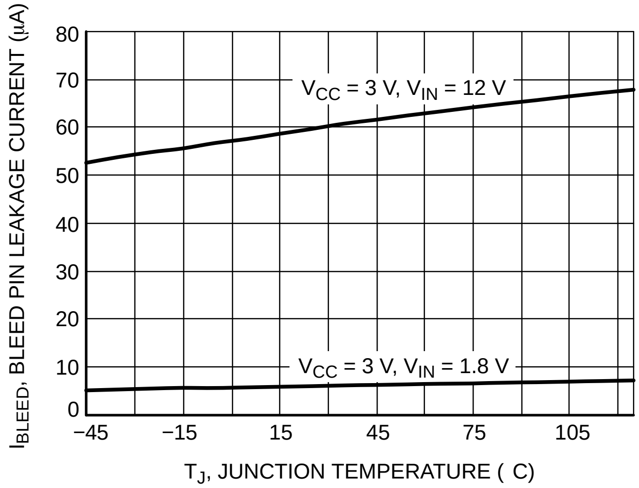


Figure 13. Bleed Pin Leakage Current vs. Temperature

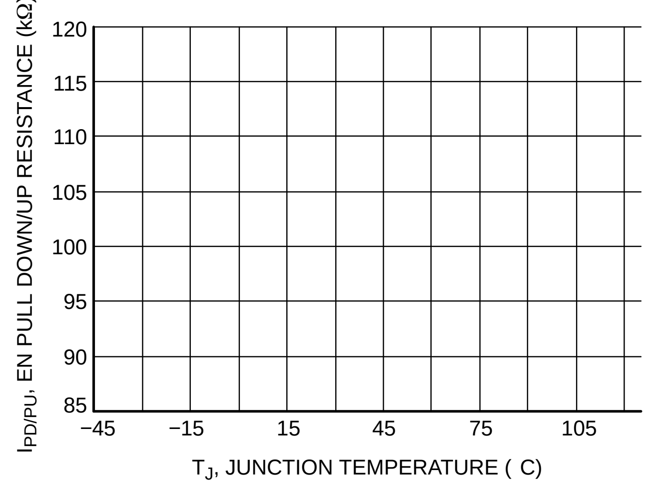


Figure 14. EN Pull Down/Up Resistance vs. Temperature

TYPICAL CHARACTERISTICS

(T_J = 25 C UNLESS OTHERWISE SPECIFIED)

14.0
13.5
13.0
12.5
12.0
11.5
11.0
10.5
−40 −20 0 20 40 60 80 100

T_J, JUNCTION TEMPERATURE (C)

Figure 21. Output Slew Rate vs. Temperature

4.5 6.5 8.5 10.5 12.5

V_{IN}, INPUT VOLTAGE (V)

Figure 22. Output Turn−on Delay vs. Input Voltage

APPLICATIONS INFORMATION

Enable Control

Both the NCP45520 and the NCP45521 have two part numbers, NCP4552x-H and NCP4552x-L, that only differ in the polarity of the enable control.

The NCP4552x-H devices allow for enabling the MOSFET in an active-high configuration. When the V_{CC} supply pin has an adequate voltage applied and the EN pin is at a logic high level, the MOSFET will be enabled. Similarly, when the EN pin is at a logic low level, the MOSFET will be disabled. An internal pull down resistor to ground on the EN pin ensures that the MOSFET will be disabled when not being driven.

The NCP4552xĭL devices allow for enabling the MOSFET in an active-low configuration. When the V_{CC} supply pin has an adequate voltage applied and the EN pin is at a logic low level, the MOSFET will be enabled. Similarly, when the EN pin is at a logic high level, the MOSFET will be disabled. An internal pull up resistor to V_{CC} on the EN pin ensures that the MOSFET will be disabled when not being driven.

Power Sequencing

The NCP4552x devices will function with any power sequence, but the output turnĭon delay performance may vary from what is specified. To achieve the specified performance, there are two recommended power sequences:

1) V_{CC} V_{IN} V_{EN}
2) V_{IN} V_{CC} V_{EN}

V_{CC} must be at 2 V or higher when EN is asserted to ensure that the enable is latched properly for correct operation. If EN comes up before V_{CC} reaches 2 V, then the EN may not take effect.

Load Bleed (Quick Discharge)

The NCP4552x devices have an internal bleed resistor, R_{BLEED}, which is used to bleed the charge off of the load to ground after the MOSFET has been disabled. In series with the bleed resistor is a bleed switch that is enabled whenever the MOSFET is disabled. The MOSFET and the bleed switch are never concurrently active.

It is required that the BLEED pin be connected to V_{OUT} either directly (as shown in Figures 31 and 34) or through an external resistor, R_{EXT} (as shown in Figures 30 and 33). R_{EXT} should not exceed 1 kΩ and can be used to increase the total bleed resistance.

Care must be taken to ensure that the power dissipated across R_{BLEED} is kept at a safe level. The maximum continuous power that can be dissipated across R_{BLEED} is 0.4 W. R_{EXT} can be used to decrease the amount of power dissipated across R_{BLEED}.

Power Good

The NCP45520 devices have a power good output (PG) that can be used to indicate when the gate of the MOSFET is fully charged. The PG pin is an active-high, open-drain output that requires an external pull up resistor, R_{PG}, greater than or equal to 1 kΩ to an external voltage source, V_{TERM}, that is compatible with input levels of all devices connected to this pin (as shown in Figures 30 and 31).

The power good output can be used as the enable signal for other activeĭhigh devices in the system (as shown in Figure 32). This allows for guaranteed by design power sequencing and reduces the number of enable signals needed from the system controller. If the power good feature is not used in the application, the PG pin should be tied to GND.

Slew Rate Control

The NCP4552x devices are equipped with controlled output slew rate which provides soft start functionality. This limits the inrush current caused by capacitor charging and enables these devices to be used in hot swap applications.

The slew rate of the NCP45521 can be decreased with an external capacitor added between the SR pin and ground (as shown in Figures 33 and 34). With an external capacitor present, the slew rate can be determined by the following equation:

$$\text{Slew Rate} = \frac{K_{SR}}{C_{SR}}\ [\text{V/s}] \qquad \text{(eq. 1)}$$

where K_{SR} is the specified slew rate control constant, found in Table 4, and C_{SR} is the slew rate control capacitor added between the SR pin and ground. The slew rate of the device will always be the lower of the default slew rate and the adjusted slew rate. Therefore, if the C_{SR} is not large enough to decrease the slew rate more than the specified default value, the slew rate of the device will be the default value. The SR pin can be left floating if the slew rate does not need to be decreased.

Short−Circuit Protection

The NCP4552x devices are equipped with shortĭcircuit protection that is used to help protect the part and the system from a sudden highĭcurrent event, such as the output, V_{OUT}, being shorted to ground. This circuitry is only active when the gate of the MOSFET is fully charged.

Once active, the circuitry monitors the difference in the voltage on the V_{IN} pin and the voltage on the BLEED pin. In order for the V_{OUT} voltage to be monitored through the BLEED pin, it is required that the BLEED pin be connected to V_{OUT} either directly (as shown in Figures 31 and 34) or through a resistor, R_{EXT} (as shown in Figures 30 and 33), which should not exceed 1 kΩ. With the BLEED pin connected to V_{OUT}, the shortĭcircuit protection is able to monitor the voltage drop across the MOSFET.

If the voltage drop across the MOSFET is greater than or equal to the shortĭcircuit protection threshold voltage, the MOSFET is immediately turned off and the load bleed is activated. The part remains latched in this off state until EN is toggled or V_{CC} supply voltage is cycled, at which point the MOSFET will be turned on in a controlled fashion with the normal output turnĭon delay and slew rate. The current

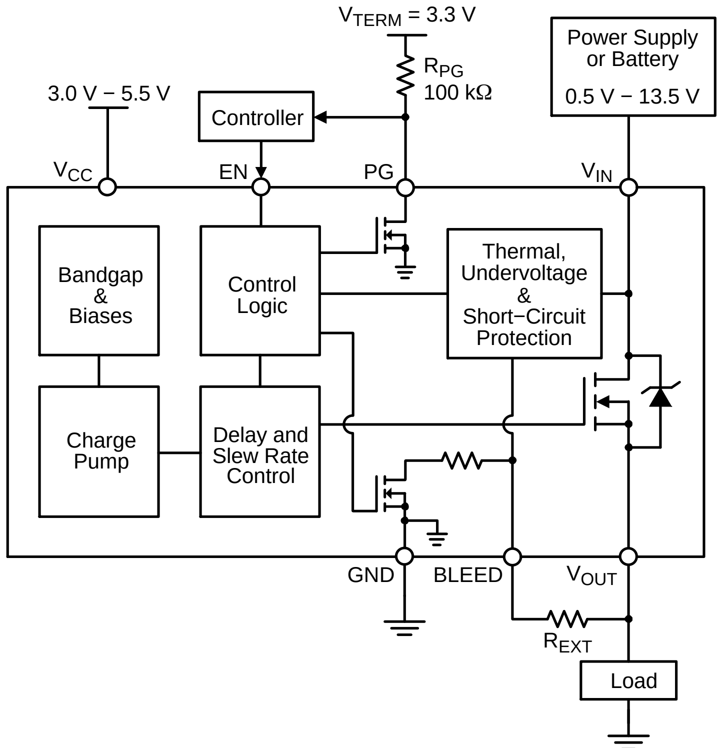


Figure 30. NCP45520 Typical Application Diagram − Load Switch

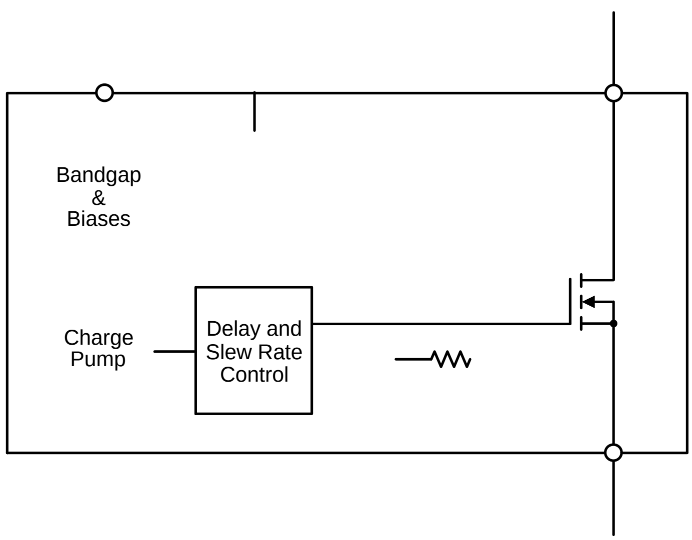


Figure 31. NCP45520 Typical Application Diagram − Hot Swap

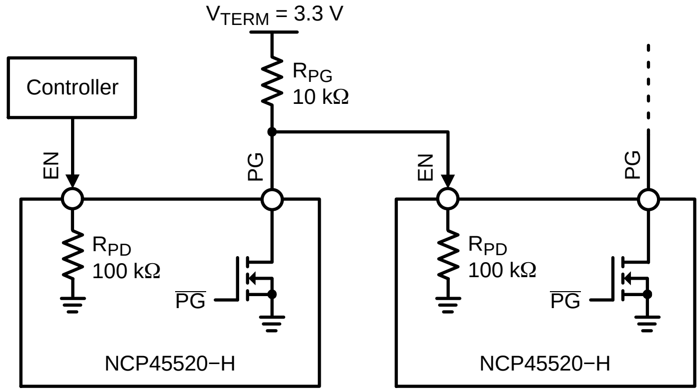


Figure 32. NCP45520 Simplified Application Diagram − Power Sequencing with PG Output

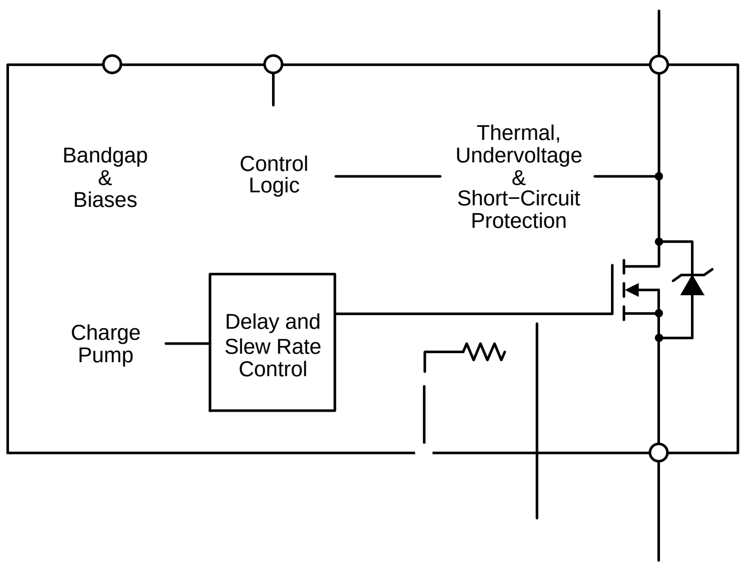
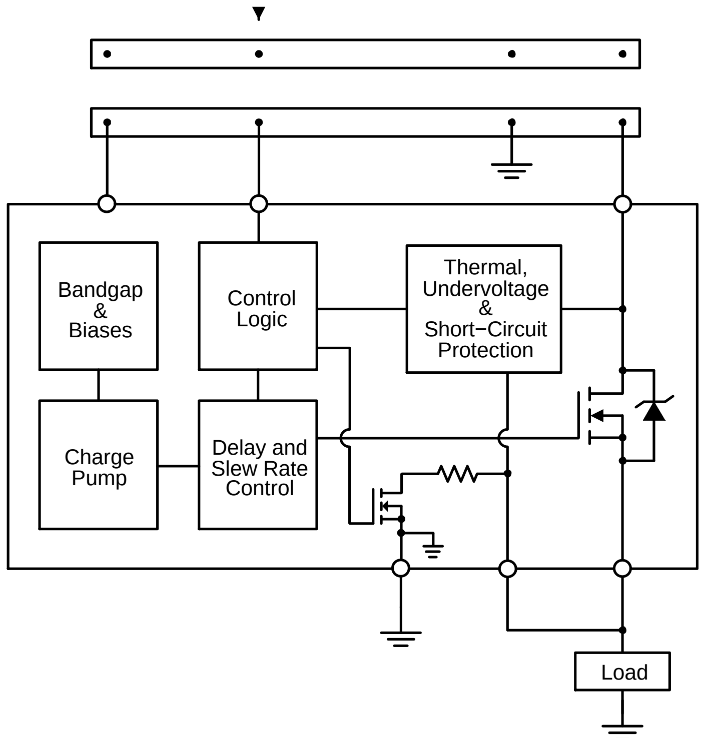


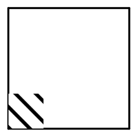
Figure 33. NCP45521 Typical Application Diagram − Load Switch


Bandgap
&
Biases
Control
Logic
Thermal,
Undervoltage
&
Short−Circuit
Protection
Charge
Pump
Delay and
Slew Rate
Control
Load

DFN8 2x2, 0.5P
CASE 506CC
ISSUE A

SCALE 2:1

DATE 24 JUN 2014



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.