C 51145

DD 1.8 A

The NCP51145 is a linear regulator designed to supply a regulated V_{TT} termination voltage for DDR−II, DDR−III, LPDDR−III and DDR−IV memory applications. The regulator is capable of actively sourcing and sinking ±1.8 A peak currents while regulating an output voltage to within ±20 mV. The output termination voltage is regulated to track V_{DDQ} / 2 by two external voltage divider resistors connected to the PV_{CC}, GND, and V_{REF} pins.

The NCP51145 incorporates a high−speed differential amplifier to provide ultra−fast response to line and load transients. Other features include source/sink current limiting, soft−start and on−chip thermal shutdown protection.

Features

- For DDR V_{TT} Applications, Source/Sink Currents:
- Supports DDR−II to ±1.8 A, DDR−III to ±1.5 A
- Supports LPDDR−III and DDR−IV to ±1.2 A
- Stable Using Ceramic−Only (Very Low ESR) Capacitors
- Integrated Power MOSFETs
- High Accuracy V_{TT} Output at Full−Load
- Fast Transient Response
- Built−in Soft−Start
- Shutdown for Standby or Suspend Mode
- Integrated Thermal and Current−Limit Protection
- V_{TT} Remote Sense Available in the DFN8 2x2mm Package
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- DDR−II / DR−III / DDR−IV SDRAM Termination Voltage
- Motherboard, Notebook, and VGA Card Memory Termination
- Set Top Box, Digital TV, Printers
- Low Power DDR−3LP

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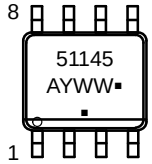
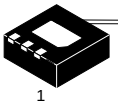
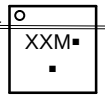
MARKING DIAGRAMS

SOIC−8 EP
D SUFFIX
CASE 751BU



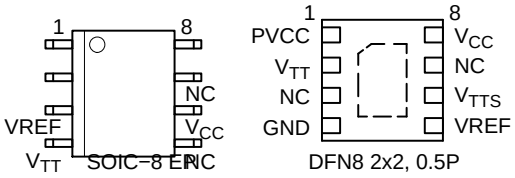


DFN8
MN SUFFIX
CASE 506AA



51145	= Specific Device Code
XX	= Specific Device Code
M	= Date Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)



(Top Views)

ORDERING INFORMATION

Device	Package	Shipping†
NCP51145PDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP51145MNTAG	DFN−8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

C1 = 1 to 100 nF Ceramic
C2 = 10 μF Ceramic
C4 = 10 μF Ceramic
R3 = Optional V_{TT} Discharge Resistor

ELECTRICAL CHARACTERISTICS

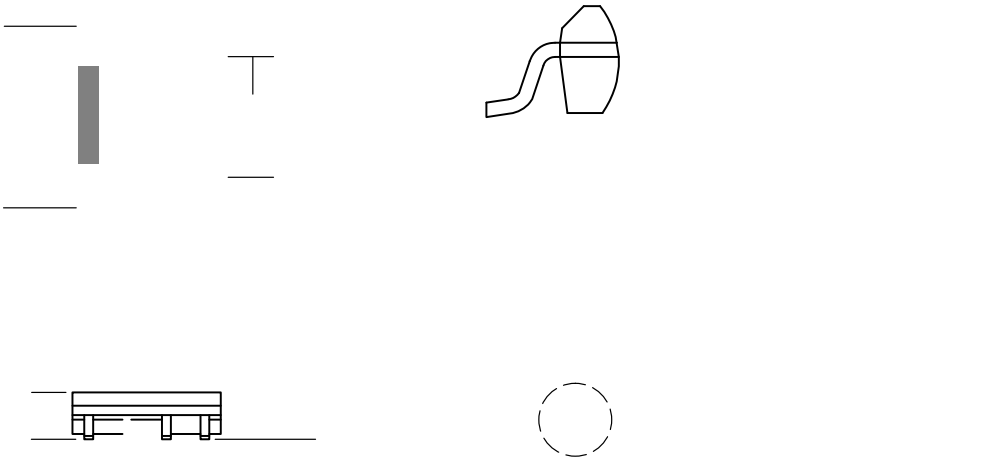
PV_{CC} = 1.8 V / 1.5 V; V_{CC} = 5 V; V_{REF} = 0.9 V / 0.75 V; C_{TT} = 10 μF (Ceramic), T_A = +25°C, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT						
Output Offset Voltage	I_{out} = 0 A	V_{OS}	−16	−	+16	mV
Load Regulation	I_{out} = ±1.8 A, PV_{CC} = 1.8 V, V_{REF} = 0.9 V	Reg_{load}	−4	−	+4	mV
	I_{out} = ±1.5 A, PV_{CC} = 1.5 V, V_{REF} = 0.75 V					
	I_{out} = ±1.2 A, PV_{CC} = 1.35 V, V_{REF} = 0.675 V					
	I_{out} = ±1.2 A, PV_{CC} = 1.2 V, V_{REF} = 0.6 V					
INPUT AND STANDBY CURRENTS						
Bias Supply Current	I_{out} = 0 A	I_{BIAS}	−	1	2.5	mA
Standby Current	V_{REF} < 0.2 V (Shutdown), R_{LOAD} = 180Ω	I_{STB}	−	2	90	μA
CURRENT LIMIT PROTECTION						
Current Limit	PV_{CC} = 1.8 V, V_{REF} = 0.9 V	I_{LIM}	2	−	3.5	A
	PV_{CC} = 1.5 V, V_{REF} = 0.75 V		1.5	−	3.5	
SHUTDOWN THRESHOLDS						
Shutdown Threshold Voltage	Enable	V_{IH}	0.45	−	−	V
	Shutdown	V_{IL}	−	−	0.15	
THERMAL SHUTDOWN						
Thermal Shutdown Temperature	V_{CC} = 5 V	T_{SD}	−	125	−	°C
Thermal Shutdown Hysteresis	V_{CC} = 5 V	T_{SH}	−	35	−	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

PACKAGE DIMENSIONS

SOIC8−NB EP
CASE 751BU
ISSUE E

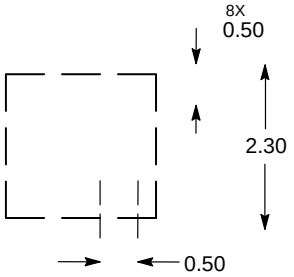


DFN8 2x2, 0.5P
CASE 506AA
ISSUE F

DATE 04 MAY 2016

1
SCALE 4:1

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.