NCP51190, NCV51190

1.5A DDR Memory Termination Regulator

The NCP/NCV51190 is a simple, cost−effective, high−speed linear regulator designed to generate the V_{TT} termination voltage rail for DDR−I, DDR−II and DDR−III memory. The regulator is capable of actively sourcing or sinking up to ±1.5 A for DDR−I, or up to ±0.5 A for DDR−II /−III while regulating the output voltage to within ±30 mV.

The output termination voltage is tightly regulated to track $V_{TT} = (V_{DDQ} / 2)$ over the entire current range.

The NCP/NCV51190 incorporates a high−speed differential amplifier to provide ultra−fast response to line and load transients. Other features include extremely low initial offset voltage, excellent load regulation, source/sink soft−start and on−chip thermal shut−down protection.

The NCP/NCV51190 features the power−saving Suspend To Ram (STR) function which will tri−state the regulator output and lower the quiescent current drawn when the /SS pin is pulled low.

The NCP/NCV51190 is available in a DFN8 package.

Features

- Generate DDR Memory Termination Voltage (V_{TT})
- For DDR−I, DDR−II, DDR−III Source / Sink Currents
- Supports DDR−I to ±1.5 A, DDR−II, DDR−III to ±0.5 A (peak)
- Integrated Power MOSFETs with Thermal Protection
- Stable with 10 μF Ceramic V_{TT} Capacitor
- High Accuracy Output Voltage at Full−Load
- Minimal External Component Count
- Shutdown for Standby or Suspend to RAM (STR) mode
- Built−in Soft Start
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

Appications

- Desktop PC's, Notebooks, and Workstations
- Graphics Card DDR Memory Termination
- Set Top Boxes, Digital TV's, Printers
- Embedded Systems
- Active Bus Termination

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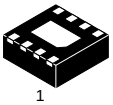
MARKING DIAGRAM



DFN8
MN SUFFIX
CASE 506AA

XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

(Note: Microdot may be in either location)

PIN CONNECTION

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 8 of this data sheet.

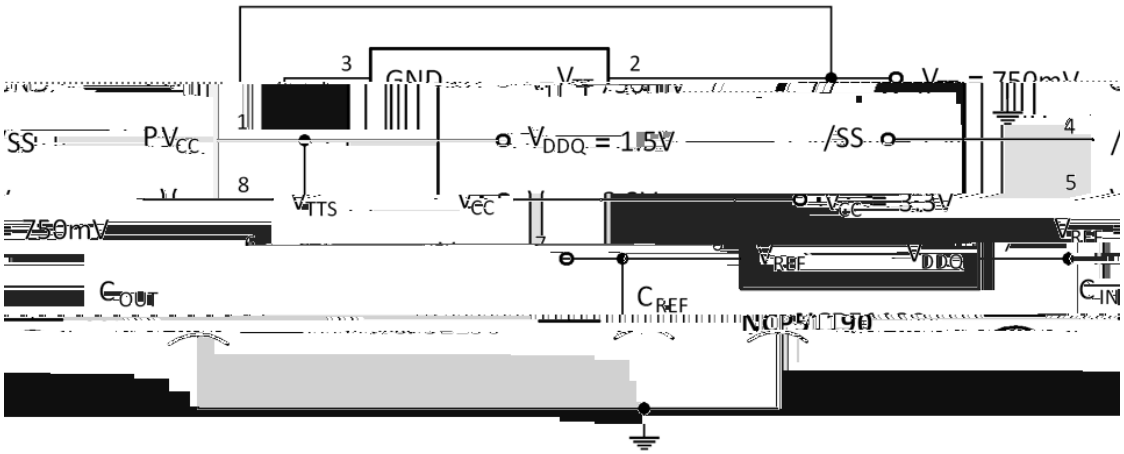


Figure 1. Typical Application Schematic

PIN FUNCTION DESCRIPTION – NCP51190

Pin Number	Pin Name	Pin Function

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC}, PV_{CC} ,V_{DDQ}, /SS to GND (Note 1)		−0.3 to +6	V
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C

ELECTRICAL CHARACTERISTICS

$-40°C \le T_J \le 125°C$; $V_{CC} = PV_{CC} = V_{DDQ} = 2.5$ V; unless otherwise noted. Typical values are at $T_J = +25°C$

Parameter	Max	Unit

TYPICAL PERFORMANCE CHARACTERISTICS

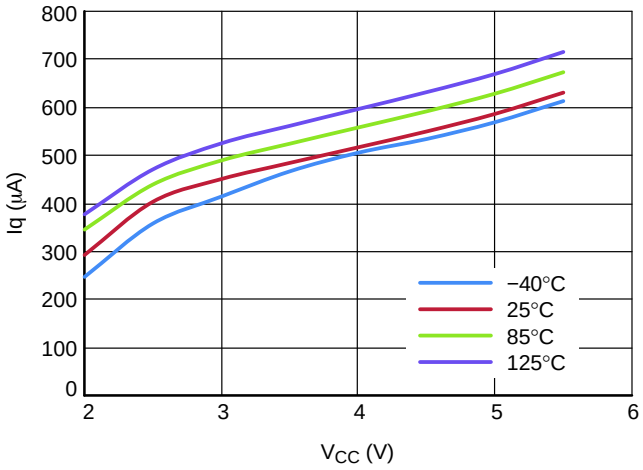


Figure 8. Iq vs. V_{CC} over Temperature

General

The NCP/NCV51190 is a bus termination, linear regulator designed to meet the JEDEC requirements for DDR−I, DDR−II and DDR−III memory termination. The NCP/NCV51190 is capable of sourcing and sinking current while accurately tracking and regulating the V_{TT} output voltage equal to (V_{DDQ} / 2). The output stage has been designed to maintain excellent load regulation and preventing shoot−through. The NCP/NCV51190 uses two distinct

Table 1. ORDERING INFORMATION

Device	Marking	Package	Shipping †
NCP51190MNTAG	A5	DFN8 (Pb-Free)	3000 / Tape & Reel
NCV51190MNTAG*	CC		

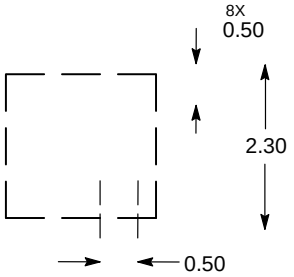
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV

DFN8 2x2, 0.5P
CASE 506AA
ISSUE F

DATE 04 MAY 2016

1
SCALE 4:1

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.