1.

11 , 11

The NCP/NCV51198 is a simple, cost−effective, high−speed linear regulator designed to generate the V_{TT} termination voltage rail for DDR−I, DDR−II and DDR−III memory. The regulator is capable of actively sourcing or sinking up to ±1.5 A for DDR−I, or up to ±0.5 A for DDR−II /−III while regulating the output voltage to within ±30 mV.

The output termination voltage is tightly regulated to track V_{TT} = (V_{DDQ} / 2) over the entire current range.

The NCP/NCV51198 incorporates a high−speed differential amplifier to provide ultra−fast response to line and load transients. Other features include extremely low initial offset voltage, excellent load regulation, source/sink soft−start and on−chip thermal shut−down protection.

The NCP/NCV51198 features the power−saving Suspend To Ram (STR) function which will tri−state the regulator output and lower the quiescent current drawn when the /SS pin is pulled low.

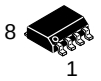
The NCP/NCV51198 is available in a SOIC−8 Exposed Pad package.

Features

- Generate DDR Memory Termination Voltage (V_{TT})
- For DDR−I, DDR−II, DDR−III Source / Sink Currents
- Supports DDR−I to ±1.5 A, DDR−II to ±0.5 A (peak)
- Integrated Power MOSFETs with Thermal Protection
- Stable with 10 μF Ceramic V_{TT} Capacitor
- High Accuracy Output Voltage at Full−Load
- Minimal External Component Count
- Shutdown for Standby or Suspend to RAM (STR) mode
- Built−in Soft Start
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

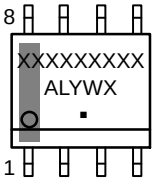
Appications

- Desktop PC's, Notebooks, and Workstations
- Graphics Card DDR Memory Termination
- Set Top Boxes, Digital TV's, Printers
- Embedded Systems
- Active Bus Termination



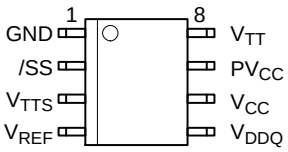
SOIC8−NB EP
PD SUFFIX
CASE 751BU

MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTION



SOIC−8 EP

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 8 of this data sheet.

1.5 A, DDR−I /−II /−III TERMINATION REGULATOR

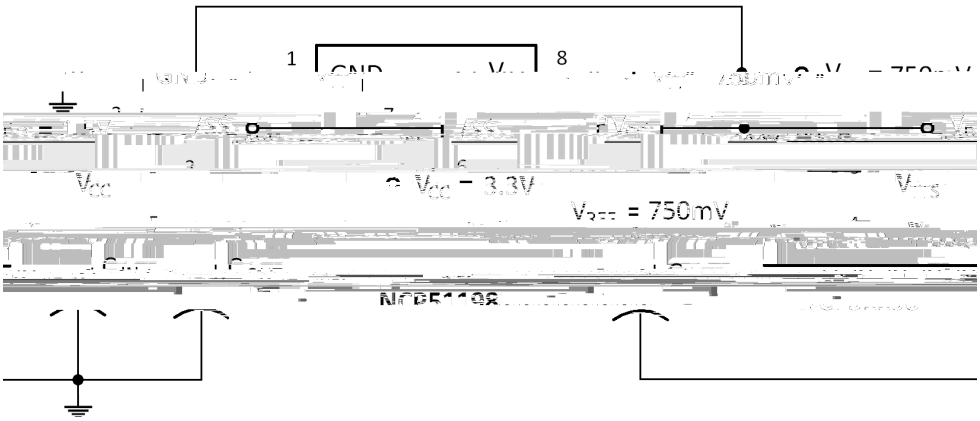


Figure 1. Typical Application Schematic

PIN FUNCTION DESCRIPTION – NCP51198

Pin Number SO8−EP	Pin Name	Pin Function
1	GND	Common Ground.
2	/SS	Suspend Shutdown supports Suspend To RAM function. CMOS compatible input sets V_{TT} output to high impedance state. Logic HI = Enable, Logic LO = Shutdown.
3	V_{TTS}	V_{TTS} is the V_{TT} sense input.
4	V_{REF}	V_{REF} is an output pin that provides the buffered output of the internal reference voltage equal to half of V_{DDQ}. Two resistors dividing down the V_{DDQ} voltage on the pin to create the regulated output voltage.
5	V_{DDQ}	The V_{DDQ} pin is an input pin for creating the internal reference voltage to regulate V_{TT}. The V_{DDQ} voltage is connected to an internal resistor divider. The central tap of resistor divider (V_{DDQ} /2) is connected to the internal voltage buffer, which output is connected to V_{REF} pin and the non−inverting input of the error amplifier as the reference voltage.
6	V_{CC}	Power for the analog control circuitry.
7	PV_{CC}	The PV_{CC} pin provides the rail voltage from where the V_{TT} pin draws load curren TD-.0019 Tc(pin S-0C2T2 1 Tf6.5 (limita

UTE MAXIMUM RATING

R	mbol	Value	Unit
PV$_{CC}$,V$_{DDQ}$, /SS to GND (Note 1)		−0.3 to +6	V
ge Temperature	g	−65 to +150	°C
ating Junction Temperature Range		−40 to +125	°C
mal Characteristics, SO8−EP Therm ance, Junction−to−Air wer Rating at 25°C ambient − 2.3 W 3 mW/°C	A	43	°C/W
Capability, Human Body Model (No	BM	2000	V
Capability, Machine Model (Note 2)	MM	150	V

es exceeding those listed in the Max ngs table may damage the devi f these limits are exceeded, device functionality not be assumed, damage may occ ability may be affected.
bin to exceed V$_{CC}$. Refer to ELECT HARACTERISTICS and APPLI FORMATION for Safe Operating Area.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Bias Supply Voltage	V$_{CCi}$		

ELECTRICAL CHARACTERISTICS

$-40°C \le T_J \le 125°C$; $V_{CC} = PV_{CC} = V_{DDQ} = 2.5$ V; unless otherwise noted. Typical values are at $T_J = +25°C$

Parameter	Condition	Symbol	Min	Typ	Max	Unit
V_{TT} Output Voltage (DDR−II)	I_{OUT} = 0 A	V_{TT} (DDR−II)	–	–	–	V
	$PV_{CC} = V_{DDQ}$ = 1.7 V		0.816	0.850	0.881	
	$PV_{CC} = V_{DDQ}$ = 1.8 V		0.866	0.900	0.931	
	$PV_{CC} = V_{DDQ}$ = 1.9 V		0.916	0.950	0.981	
	I_{OUT} = +0.5 A	V_{TT} (DDR−II)	–	–	–	
	$PV_{CC} = V_{DDQ}$ = 1.7 V		0.815	0.851	0.885	
	$PV_{CC} = V_{DDQ}$ = 1.8 V		0.863	0.900	0.933	
	$PV_{CC} = V_{DDQ}$ = 1.9 V		0.914	0.950	0.984	
	I_{OUT} = −0.5 A	V_{TT} (DDR−II)	–	–	–	
	$PV_{CC} = V_{DDQ}$ = 1.7 V		0.814	0.850	0.884	
	$PV_{CC} = V_{DDQ}$ = 1.8 V		0.862	0.900	0.932	
	$PV_{CC} = V_{DDQ}$ = 1.9 V		0.913	0.950	0.983	

TYPICAL PERFORMANCE CHARACTERISTICS

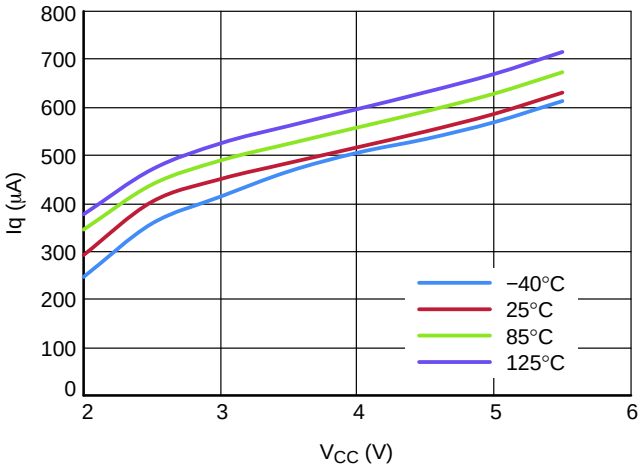


Figure 8. Iq vs. V_{CC} over Temperature

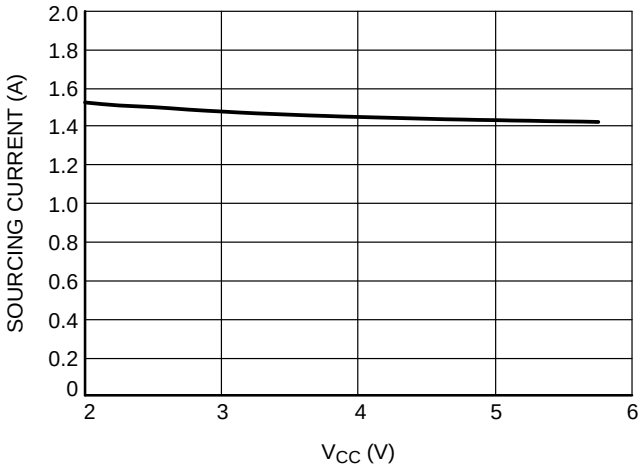


Figure 9. Maximum Sourcing Current vs. V_{CC} (V_{DDQ} = PV_{CC} = 1.8 V)

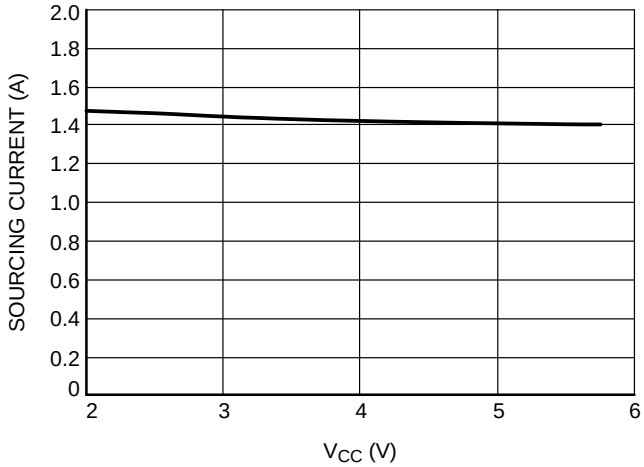


Figure 10. Maximum Sourcing Current vs. V_{CC} (V_{DDQ} = 2.5 V, PV_{CC} = 1.8 V

APPLICATIONS INFORMATION

General

The NCP/NCV51198 is a bus termination, linear regulator designed to meet the JEDEC requirements for DDR−I, DDR−II and DDR−III memory termination. The NCP/NCV51198 is capable of sourcing and sinking current while accurately tracking and regulating the V_{TT} output voltage equal to (V_{DDQ} / 2). The output stage has been designed to maintain excellent load regulation and preventing shoot−through. The NCP/NCV51198 uses two

Table 1. ORDERING INFORMATION

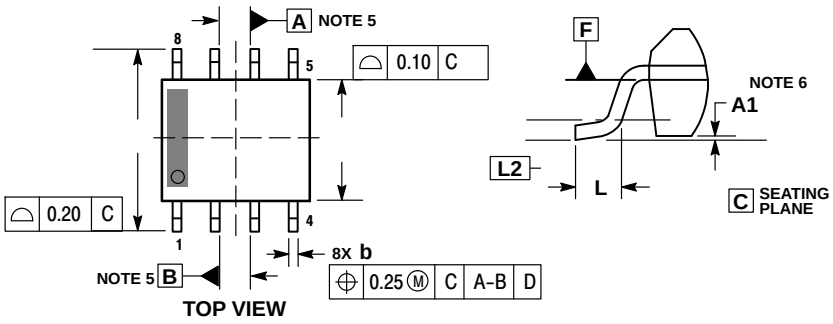
Device	Marking	Package	Shipping †
NCP51198PDR2G	51198	SOIC−8 (Pb-Free)	2500 / Tape & Reel
NCV51198PDR2G*	V51198		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

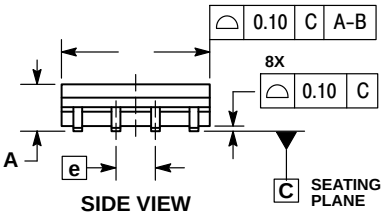
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

SOIC8−NB EP

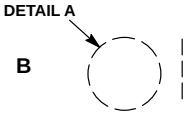
SCALE 1:1



TOP VIEW

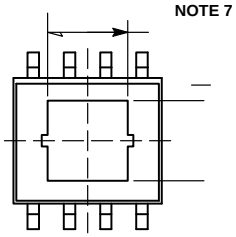


SIDE VIEW



END VIEW

DIM	MILLIMETERS MIN	MAX
A		
A1		
b		
b1		



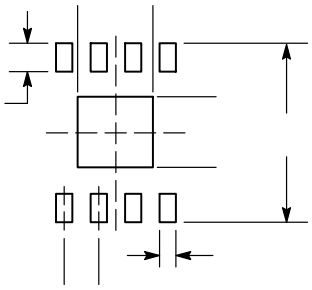
e	

G		
h		

L2	

GENERIC
MARKING DIAGRAM*

RECOMMENDED
SOLDERING FOOTPRINT*



onsemi