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#### **PIN FUNCTION DESCRIPTION**

Pin Number	Pin Name	Pin Function			
1	V <sub>RI</sub>	$V_{TT}$ External Reference Input ( set to $V_{DDQ}$ / 2 thru resistor network ).			
2	PV <sub>CC</sub>	Power input. Internally connected to the output source MOSFET.			
3	V <sub>TT</sub>	Power Output of the Linear Regulator.			
4	P <sub>GND</sub>	Power Ground. Internally connected to the output sink MOSFET.			
5	V <sub>TTS</sub>	$V_{TT}$ Sense Input. The V <sub>TTS</sub> pin provides accurate remote feedback sensing of V <sub>TT</sub> . Connect V <sub>TTS</sub> to the remote DDR termination bypass capacitors.			
6	V <sub>RO</sub>	Independent Buffered V <sub>TT</sub> Reference Output. Sources and sinks over 5 mA. Connect to GND thru 0.1 $\mu F$ ceramic capacitor.			
7	EN	Shutdown Control Input. CMOS compatible input. Logic high = enable, logic low = shutdown. Connect to $V_{DDQ}$ for normal operation.			
8	GND	Common Ground.			
9	P <sub>GOOD</sub>	Power Good (Open Drain output).			
10	V <sub>CC</sub>	Analog power supply input. Connect to GND thru a 1 $4.7 \mu\text{F}$ ceramic capacitor.			
	THERMAL PAD	Pad for thermal connection. The exposed pad must be connected to the ground plane using multiple vias for maximum power dissipation performance.			

#### **ABSOLUTE MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
V <sub>CC</sub> , PV <sub>CC</sub> , V <sub>TT</sub> , V <sub>TTS</sub> , V <sub>RI</sub> , V <sub>RO</sub> (Note 1)		0.3 to 6.0	V
EN, P <sub>GOOD</sub> (Note 1)		0.3 to 6.0	V
P <sub>GND</sub> to GND (Note 1)		0.3 to +0.3	V
Storage Temperature	T <sub>STG</sub>	55 to 150	°C
Operating Junction Temperature Range	TJ	150	°C
ESD Capability, Human Body Model (Note 2)	ESD <sub>HBM</sub>	2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

## **RECOMMENED OPERATING CONDITIONS**

Rating	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	2.375 to 5.5	V
Voltage Range	V <sub>RO</sub>	0.1 to 1.8	V
	V <sub>RI</sub>	0.5 to 1.8	
	$PV_{CC}, V_{TT}, V_{TTS}, EN, P_{GOOD}$	0.1 to 3.5	
	P <sub>GND</sub>	0.1 to +0.1	
Operating Free Air Temperature	T <sub>A</sub>		-

 $\label{eq:construct} \begin{array}{l} \textbf{ELECTRICAL CHARACTERISTICS} \\ 40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq 125^{\circ}\text{C}; \ \text{V}_{\text{CC}} = 3.3 \ \text{V}; \ \text{PV}_{\text{CC}} = 1.8 \ \text{V}; \ \text{V}_{\text{RI}} = \text{V}_{\text{TTS}} = 0.9 \ \text{V}; \ \text{EN} = \text{V}_{\text{CC}}; \ \text{C}_{\text{OUT}} = 3 \ \text{x} \ 10 \ \mu\text{F} \ (\text{Ceramic}); \ \text{unless otherwise noted}. \end{array}$ 

Parameter	neter Conditions Symbol		Min	Тур	Max	Units
P <sub>GOOD</sub> Powergood Comparator						
P <sub>GOOD</sub> Lower Threshold (with respect to V <sub>RO</sub> )			23.5%	20%	17.5 %	V/V
P <sub>GOOD</sub> Upper Threshold (with respect to V <sub>RO</sub> )		17.5%	20%	23.5%		
P <sub>GOOD</sub> Hysteresis				5%		
P <sub>GOOD</sub> Start up Delay	Start up rising edge, $V_{\mbox{TTS}}$ within 15% of $V_{\mbox{RO}}$			2		ms
$ \begin{array}{ll} P_{GOOD} \mbox{ Leakage Current} & V_{TTS} = V_{RI} \left(P_{GOOD} = True\right) \\ P_{GOOD} = V_{CC} + 0.2 \ V \end{array} $				1	μΑ	
P <sub>GOOD</sub> = False Delay	$V_{TTS}$ is beyond $\pm 20\%~P_{GOOD}$ trip thresholds			10		μs

P<sub>GOOD</sub>

#### **ELECTRICAL CHARACTERISTICS**

 $40^{\circ}C \leq T_{A} \leq 125^{\circ}C; \ V_{CC} = 3.3 \ V; \ PV_{CC} = 1.8 \ V; \ V_{RI} = V_{TTS} = 0.9 \ V; \ EN = V_{CC}; \ C_{OUT} = 3 \ x \ 10 \ \mu F \ (Ceramic); \ unless \ otherwise \ noted.$ 

Parameter	Conditions	Symbol	Min	Тур	Max	Units

EN Enable Logic





capacitors, the effective capacitance drops rapidly with the applied DC bias voltage (refer the capacitor's datasheet for details). Larger capacitance and lower ESR improves the load transient response and PSRR. In the PCB layout, design the traces short and wide and place the capacitor at the same PCB layer as the device (do not use layers changing for the traces).

## **PVCC Input Capacitor**

Power input capacitor, connected as close as possible to PVCC and PGND pins, is also necessary to ensure device stability and good transient response. The value of the input capacitor should be 10  $\mu$ F or greater (max. value is not

limited). This capacitor provides needed energy during load transients for output capacitor re-charging and from this point of view, the higher value is better. The good starting value is the half of the output capacitor value. The rules mentioned at VTT capacitor paragraph are applicable for PVCC capacitor as well.

## VCC Input Capacitor

Add a ceramic capacitor, connected as close as possible to VCC and GND pins. The X7R or X5R capacitor should be used with a value in range from 1  $\mu$ F to 10  $\mu$ F is recommended.

Device	Marking Code	Package	Feature	Shipping <sup>†</sup>
NCP51200MNTXG	51200			
NCV51200MNTXG*	51200 MN	DFN10 (Pb Free)		3000 / Tape & Reel
NCV51200MWTXG*	51200 MW		Wettable Flank SFS Process	3000 / Tape & Reel
NCV51200MLTXG*	51200 ML	DFNW10 (Pb Free)	Wettable Flank SLP Process	3000 / Tape & Reel
NCP51200AMNTXG	51200 A	DFN10 (Pb Free)		

#### **DEVICE ORDERING INFORMATION**

DFNW10 3x3, 0.5P CASE 507AM ISSUE A

DATE 12 JUN 2018

GENERIC MARKING DIAGRAM\*

• XXXXX XXXXX ALYW• XXXXX = Specific Device Code

- = Assembly Location
- = Wafer Lot
- = Year

А

L

Υ

W

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- = Work Week
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

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