NCP51400

The NCP51400 is a source/sink Double Data Rate (DDR) termination regulator specifically designed for low input voltage and low−noise systems where space is a key consideration.

The NCP51400 maintains a fast transient response and only requires a minimum output capacitance of 20 μF. The NCP51400 supports a remote sensing function and all power requirements for DDR V_{TT} bus termination. The NCP51400 can also be used in low−power chipsets and graphics processor cores that require dynamically adjustable output voltages.

The NCP51400 is available in the thermally−efficient DFN10 Exposed Pad package, and is available in both Green and Pb−Free Packages.

- NCV51400MWTXG − Wettable Flank Option for Enhanced Optical Inspection
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable*
- These Devices are Pb−Free and are RoHS Compliant

Applications

- DDR Memory Termination
- Desktop PC's, Notebooks, and Workstations
- Servers and Networking equipment
- Telecom/Datacom, GSM Base Station
- Graphics Processor Core Supplies
- Set Top Boxes, LCD−TV/PDP−TV, Copier/Printers
- Chipset/RAM Supplies as Low as 0.5 V
- Active Bus Termination

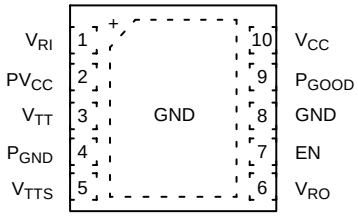
DFN10, 3x3, 0.5P
CASE 506CL

MARKING DIAGRAM

51400	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot (Optional character)
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTION



ORDERING INFORMATION

Device	Package	Shipping†
NCP51400MNTXG	DFN10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Pin Function
1	V_{RI}	V_{TT} External Reference Input (set to V_{DDQ} / 2 thru resistor network).
2	PV_{CC}	Power input. Internally connected to the output source MOSFET.
3	V_{TT}	Power Output of the Linear Regulator.
4	P_{GND}	Power Ground. Internally connected to the output sink MOSFET.
5	V_{TTS}	V_{TT} Sense Input. The V_{TTS} pin provides accurate remote feedback sensing of V

RECOMMENED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	2.375 to 5.5	V
Voltage Range	V_{RO}	−0.1 to 1.8	V
	V_{RI}	0.5 to 1.8	
	PV_{CC}, V_{TT}, V_{TTS}, EN, P_{GOOD}	−0.1 to 3.5	
	P_{GND}	−0.1 to +0.1	
Operating Free−Air Temperature	T_A	−40 to +125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

−40°C ≤ T_A ≤ 125°C; V_{CC} = 3.3 V; PV_{CC} = 1.8 V; V_{RI} = V_{TTS} = 0.9 V; EN = V_{CC}; C_{OUT} = 3 x 10 □F (Ceramic); unless otherwise noted.

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Supply Current						
V_{CC} Supply Current	T_A = +25°C, EN = 3.3 V, No Load	I_{VCC}		0.7	1	mA
V_{CC} Shutdown Current	T_A = +25°C, EN = 0 V, V_{RI} = 0 V, No Load	$I_{VCC\ SHD}$		65	80	□A
	T_A = +25°C, EN = 0 V, V_{RI} > 0.4 V, No Load			200	400	
V_{CC} UVLO Threshold	Wake−up, T_A = +25°C	V_{UVLO}	2.15	2.3	2.375	V
	Hysteresis			50		mV
PV_{CC} Supply Current	T_A = +25°C, EN = 3.3 V, No Load	I_{PVCC}		1	50	□A
PV_{CC} Shutdown Current	T_A = +25°C, EN = 0 V, No Load	$I_{PVCC\ SHD}$		0.1	50	□A
V_{TT} Output						
V_{TT} Output DC Voltage	PV_{CC} = 1.50 V, V_{RO} = 0.75 V, I_{TT} = 0 A	V_{OS}		0.75		V
	PV_{CC} = 1.35 V, V_{RO} = 0.675 V, I_{TT} = 0 A			0.675		
	PV_{CC} = 1.20 V, V_{RO} = 0.60 V, I_{TT} = 0 A			0.60		
V_{TT} Output Voltage Tolerance to V_{RO}	PV_{CC} = 1.50 V, V_{RO} = 0.75 V, −2 A < I_{TT} < 2 A			±18		mV
	PV_{CC} = 1.35 V, V_{RO} = 0.675 V, −2 A < I_{TT} < 2 A			±20		
	PV_{CC} = 1.20 V, V_{RO} = 0.60 V, −2 A < I_{TT} < 2 A			±20		
Source Current Limit	V_{TTS} = 90% * V_{RO}		3		4.5	A
Sink Current Limit	V_{TTS} = 110% * V_{RO}		3.5		5.5	A
Soft−start Current Limit Timeout		T_{SS}		200		□s
Discharge MOSFET On−resistance	V_{RI} = 0 V, V_{TT} = 0.3 V, EN = 0 V, T_A = +25°C	R_{DIS}		18	25	□
V_{RI} Input Reference						
V_{RI} Voltage Range		V_{RI}	0.5		1.8	V
V_{RI} Input−bias Current	EN = 3.3 V	I_{RI}				

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 125°C$; V_{CC} = 3.3 V; PV_{CC} = 1.8 V; $V_{RI} = V_{TTS}$ = 0.9 V; EN = V_{CC}; C_{OUT} = 3 x 10 □F (Ceramic); unless otherwise noted.

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
V_{RO} Voltage Tolerance to V_{RI}	−10 mA < I_{RO} < 10 mA, V_{RI} = 1.25 V		−15		+15	

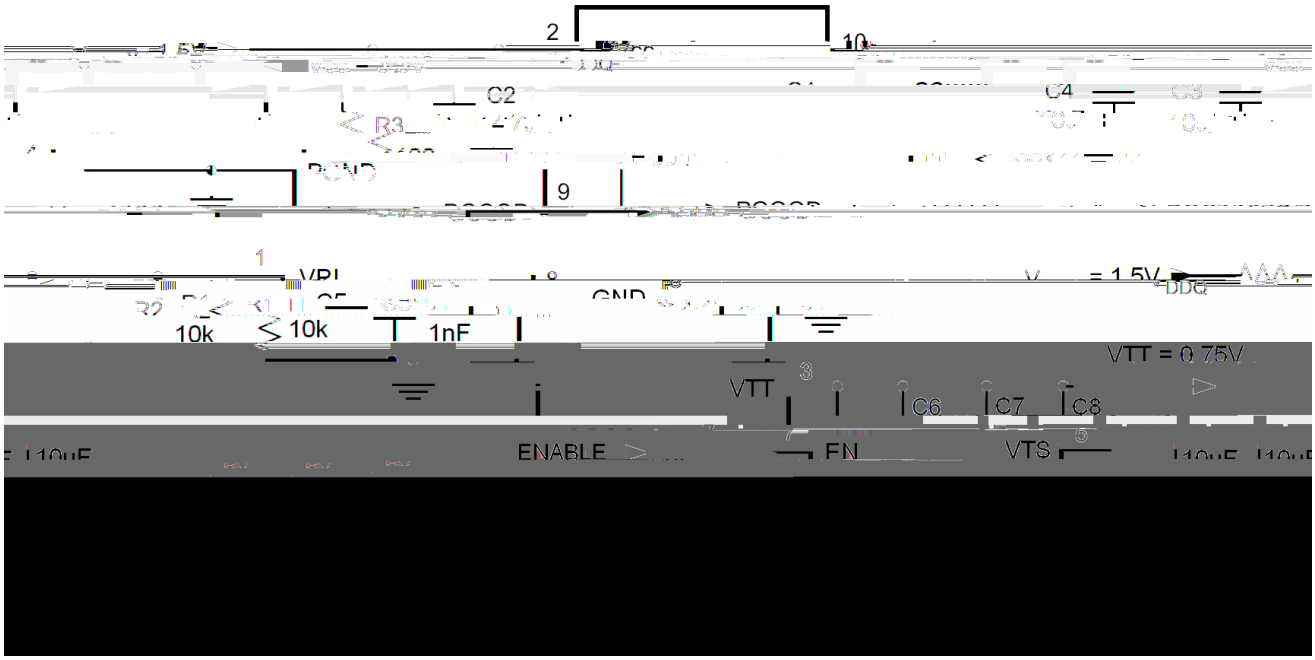


Figure 1. Typical DDR 3 Application Schematic

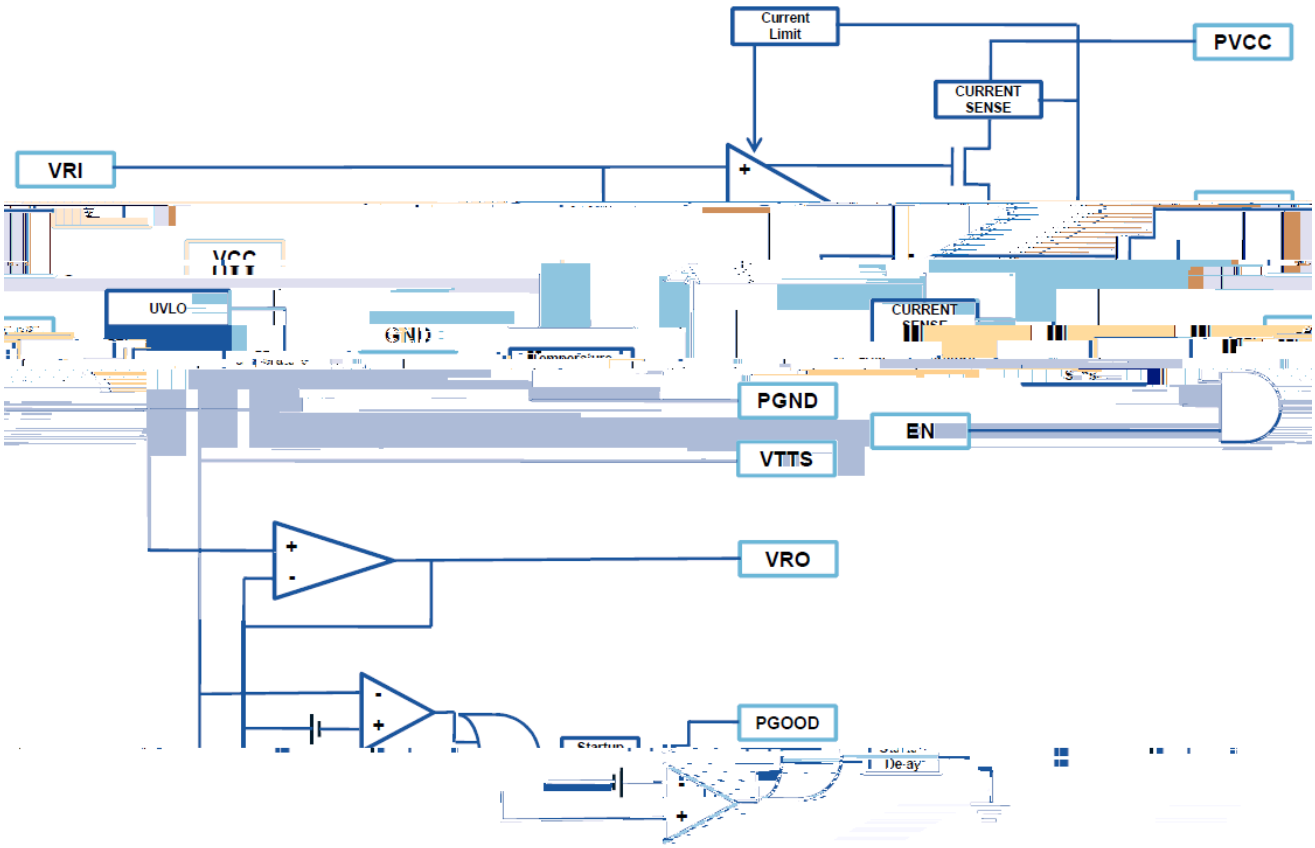


Figure 2. Block Diagram

General

The NCP51400 is a sink/source tracking termination regulator specifically designed for low input voltage and low external component count systems where space is a key application parameter. The NCP51400 integrates a high−performance, low−dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, V_{TTS}, should be connected to the positive terminal of the output capacitors as a separate trace from the high current path from V_{TT}.

V_{RI} Generation of Internal Voltage Reference

The output voltage, V_{TT}, is regulated to V_{RO}. When V_{RI} is configured for standard DDR termination applications, V_{RI} can be set by an external equivalent ratio voltage divider

capacitors, the effective capacitance drops rapidly with the applied DC bias voltage (refer the capacitor's datasheet for details). Larger capacitance and lower ESR improves the load transient response and PSRR. In the PCB layout, design the traces short and wide and place the capacitor at the same PCB layer as the device (do not use layers changing for the traces).

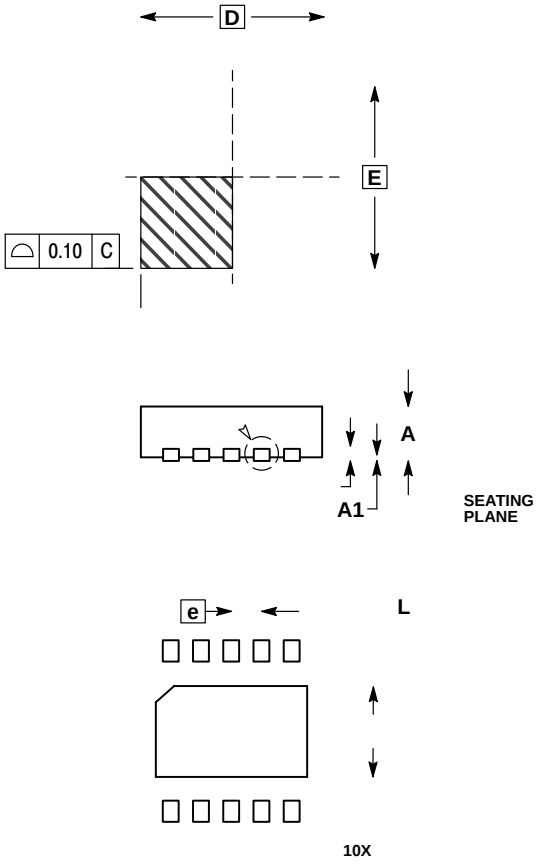
PVCC Input Capacitor

Power input capacitor, connected as close as possible to PVCC and PGND pins, is also necessary to ensure device stability and good transient response. The value of the input capacitor should be 10 μF or greater (max. value is not limited). This capacitor provides needed energy during load

DFN10, 3x3, 0.5P
CASE 506CL
ISSUE O

SCALE 2:1

DATE 02 APR 2013



GENERIC
MARKING DIAGRAM*

(Note: Microdot may be in either location

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.