August, 2021 − Rev. 1
Publication Order Number:

RECOMMENED OPERATING CONDITIONS

Rating	Symbol	Value	Unit

ELECTRICAL CHARACTERISTICS

General

The NCP51401 is a sink/source tracking termination regulator specifically designed for low input voltage and low external component count systems where space is a key application parameter. The NCP51401 integrates a high−performance, low−dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, V_{TTS}, should be connected to the positive terminal of the output capacitors as a separate trace from the high current path from V_{TT}.

V_{RI} − Generation of Internal Voltage Reference

The output voltage, V_{TT}, is regulated to V_{RO}. When V_{RI} is configured for standard DDR termination applications, V_{RI} can be set by an external equivalent ratio voltage divider connected to the memory supply bus (V_{DDQ}). The NCP51401 supports V_{RI} voltage from 0.5 V to 1.8 V, making it versatile and ideal for many types of low−power LDO applications.

V_{RO} − Reference Output

When it is configured for DDR termination applications, V_{RO} generates the DDR V_{TT} reference voltage for the memory application. It is capable of supporting both a sourcing and sinking load of 10 mA. V_{RO} becomes active when V_{RI} voltage rises to 435 mV and V_{CC} is above the UVLO threshold. When V_{RO} is less than 360 mV, it is disabled and subsequently discharges to GND through an internal 10 kΩ MOSFET. V_{RO} is independent of the EN pin state.

EN − Enable Control

When EN is driven high, the NCP51401 V_{TT} regulator begins normal operation. When EN is driven low, V_{TT} is discharges to GND through an internal 18−Ω MOSFET. V_{REF} remains on when EN is driven low.

P_{GOOD} − PowerGood

The NCP51401 provides an open−drain P_{GOOD} regut2lROoo eJsure rovidaci TD0 Tc.0326 Tw[(LDO r219.8(it vx3(ef)ternen EN ismA

DDR3/DDR4 SELECTOR GUIDE

VTT Startup Time

In order to speed up the time it takes a modern computer to Boot−up or Resume after Stand−by, some newer motherboard specs require VTT to rise from 0 V to 95% of VTT in less than 35 μsec. This new requirement is met in the new ON Semiconductor NCP51401, NCP51402 and NCP51403 devices.

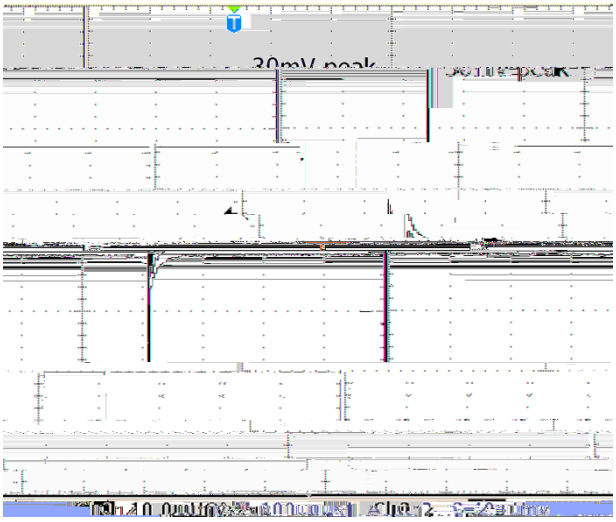

Figure 3.

Legacy DDR2/3, DDR4 and Droop Compensation

When the popular, now industry−standard, 51200−compatible devices were first introduced, the PC memory industry was transitioning from DDR2 (VTT = 900 mV) to DDR3 (VTT = 750 mV) and a value of ±14 mV of droop compensation per ±1.5 amps of DC current was designed−in. This value of droop was appropriate for the DDR2 and DDR3 memory in use at the time, but this amount of droop has now become excessive for DDR4. For example for DDR4 with a VTT voltage of 600 mV, the 5% error tolerance is ±30 mV, which leaves no transient−response margin for a DC load of ±2 amps. This excessive DDR2/3 droop compensation issue of using 51200 devices in newer DDR4 applications has been solved in the new ON Semiconductor NCP51402 and NCP51403 devices, which have no droop compensation for improved, high−current DDR4 transient response.

VTT Droop Compensation

Droop compensation is a technique to reduce error voltage due to a transient, or as a design tradeoff, to reduce system cost for a given transient magnitude, by using smaller, less expensive capacitors. Figure 3 shows the transient response in a system without droop compensation and is showing a peak−to−peak error voltage of ±30 mV. Figure 4 shows the same magnitude of transient response, but this time the regulation is performed *with* droop compensation. For example the magnitude of the transient in Figure 4 is +30 mV = +20 mV – (−10 mV) which is the same magnitude as in Figure 3, but since the output voltage is allowed to sag 10 mV when loaded (as opposed to the “perfect” Load Regulation, i.e. 0 mV of VTT output voltage sag as shown in Figure 3) then this same +30 mV transient starts at −10 mV and now only peaks to +20 mV. The net result is that with 10 mV of droop, the overall, peak−to−peak error voltage has been reduced from ±30 mV to ±20 mV.

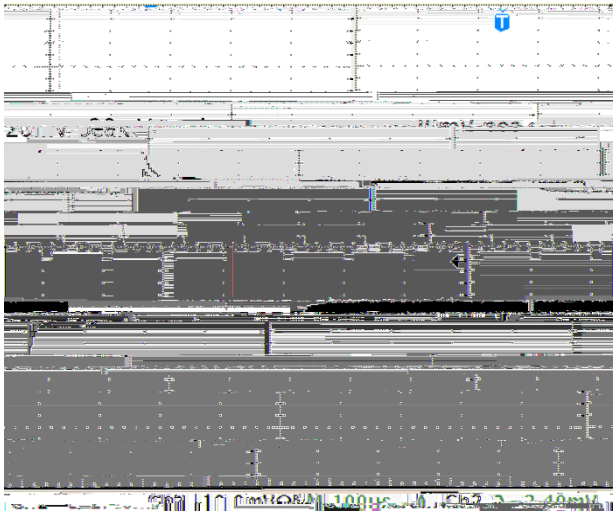

Figure 4.

VTT Capacitor Selection

Many 51200−compatible devices have specified VTT capacitor ESR requirements and must be loaded with at least 20 μF of ceramic capacitance in order to guarantee stability. In contrast, the NCP51400, NCP51401 and NCP51402 were all designed to be stable with a wide range of ESR and can use both ceramic and higher−ESR, polymer capacitors.

Extending the NCP5140x family of parts, in applications that have specified phase margin requirements, we have introduced the NCP51403 which has 45° of phase margin when VTT is loaded with a ceramic capacitance of 40 μF. However just like our competitor’s 51200−compatible devices, the NCP51403 cannot be loaded solely with polymer capacitors because the 45° phase margin reduces the ESR−stability range of the VTT capacitor.

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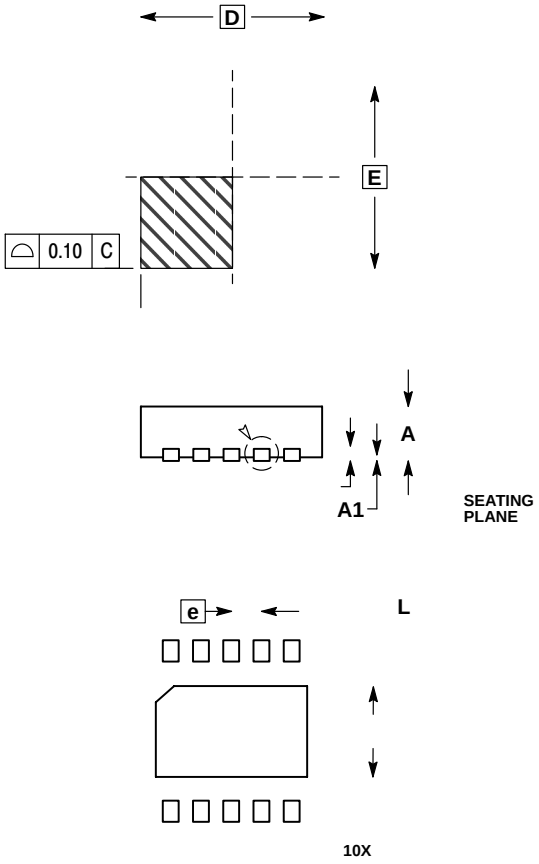

GENERIC
MARKING DIAGRAM*

(Note: Microdot may be in either location

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.