[redacted]

The NCP51403 is a source/sink Double Data Rate (DDR) termination regulator specifically designed for low input voltage and low−noise systems where space is a key consideration.

The NCP51403 maintains a fast transient response and only requires a minimum output capacitance of 20 μF. The NCP51403 supports a remote sensing function and all power requirements for DDR V_{TT} bus termination. The NCP51403 can also be used in low−power chipsets and graphics processor cores that require dynamically adjustable output voltages.

The NCP51403 is available in the thermally−efficient DFN10 Exposed Pad package, and is rated both Green and Pb−free.

Features

- Input Voltage Rails: Supports 2.5 V, 3.3 V and 5 V Rails
- PV_{CC} Voltage Range: 1.1 to 3.5 V
- Integrated Power MOSFETs
- Phase Margin >45° with Recommended 20 μF V_{TT} Capacitance
- P_{GOOD} − Logic output pin to Monitor V_{TT} Regulation
- EN − Logic input pin for Shutdown mode
- V_{RI} − Reference Input Allows for Flexible Input Tracking Either Directly or Through Resistor Divider
- Remote Sensing (V_{TTS})
- Built−in Under Voltage Lockout and Over Current Limit
- Thermal Shutdown
- Small, Low−Profile 10−pin, 3x3 DFN Package
- These Devices are Pb−Free and are RoHS Compliant

Applications

- DDR Memory Termination
- Desktop PC's, Notebooks, and Workstations
- Servers and Networking equipment
- Telecom/Datacom, GSM Base Station
- Graphics Processor Core Supplies
- Set Top Boxes, LCD−TV/PDP−TV, Copier/Printers
- Chipset/RAM Supplies as Low as 0.5 V
- Active Bus Termination

DDR3/DDR4 SELECTOR GUIDE

(see notes on page 7)

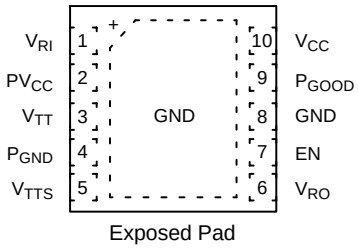
DFN10, 3x3, 0.5P
CASE 506CL

MARKING DIAGRAM

51403	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTION



Exposed Pad

ORDERING INFORMATION

Device	Package	Shipping†
NCP51403MNTXG	DFN10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Pin Function
1	V_{RI}	V_{TT} External Reference Input (set to V_{DDQ} / 2 thru resistor network).
2	PV_{CC}	Power input. Internally connected to the output source MOSFET.
3	V_{TT}	Power Output of the Linear Regulator.
4	P_{GND}	Power Ground. Internally connected to the output sink MOSFET.
5	V_{TTS}	V_{TT} Sense Input. The V_{TTS} pin provides accurate remote feedback sensing of V_{TT}. Connect V_{TTS} to the remote DDR termination bypass capacitors.
6	V_{RO}	Independent Buffered V_{TT} Reference Output. Sources and sinks over 5 mA. Connect to GND thru 0.1 μF ceramic capacitor.
7	EN	Shutdown Control Input. CMOS compatible input. Logic high = enable, logic low = shutdown. Connect to V_{DDQ} for normal operation.
8	GND	Common Ground.
9		

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 125°C$; V_{CC} = 3.3 V; PV_{CC} = 1.8 V; $V_{RI} = V_{TTS}$ = 0.9 V; EN = V_{CC}; C_{OUT} = 3 x 10 μF (Ceramic); unless otherwise noted.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
SUPPLY CURRENT						
V_{CC} Supply Current	T_A = +25°C, EN = 3.3 V, No Load	I_{VCC}		0.7	1	mA
V_{CC} Shutdown Current	T_A = +25°					

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 125°C$; V_{CC} = 3.3 V; PV_{CC} = 1.8 V; $V_{RI} = V_{TTS}$ = 0.9 V; EN = V_{CC}; C_{OUT} = 3 x 10 μF (Ceramic); unless otherwise noted.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
EN − ENABLE LOGIC						
Logic Input Threshold	EN Logic high	V_{IH}	1.7			V
	EN Logic low	V_{IL}			0.3	
Hysteresis Voltage	EN pin	V_{ENHYS}		0.5		V
Logic Leakage Current	EN pin, T_A = +25°C					

General

The NCP51403 is a sink/source tracking termination regulator specifically designed for low input voltage and low external component count systems where space is a key application parameter. The NCP51403 integrates a high−performance, low−dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, V_{TTS}

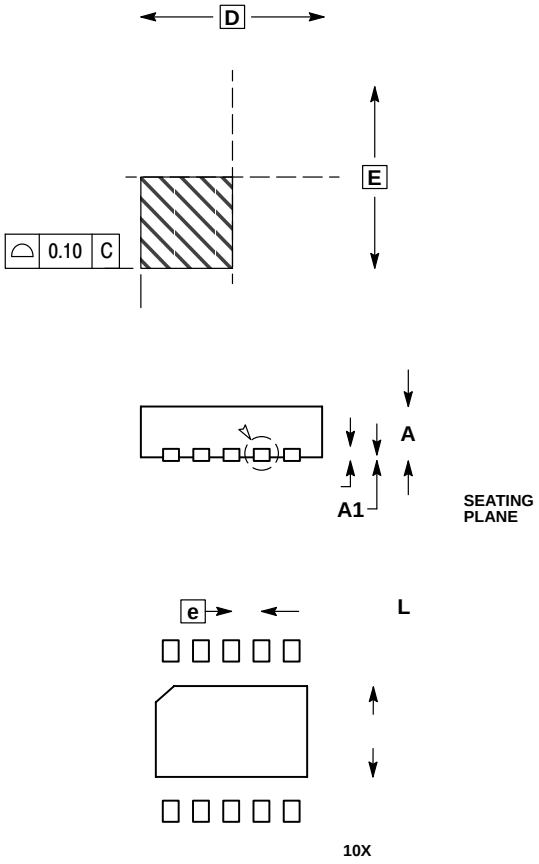
DDR3/DDR4 SELECTOR GUIDE

VTT Startup Time

DFN10, 3x3, 0.5P
CASE 506CL
ISSUE O

SCALE 2:1

DATE 02 APR 2013



GENERIC
MARKING DIAGRAM*

(Note: Microdot may be in either location

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.