3 Amp V_{TT} Termination Source / Sink Regulator for DDR, DDR-2, DDR-3, DDR-4

NCP51510, NCV51510

The NCP51510 is a source/sink Double Data Rate (DDR) termination regulator specifically designed for low input voltage and low−noise systems where space is a key consideration. The NCP51510 maintains a fast transient response and only requires a minimum V load capacitance of 10 μF for output stability. The NCP51510 supports remote sensing and all power requirements for DDR V bus termination. The NCP51510 can also be used in low−power chipsets and graphics processor cores that require dynamically adjustable output voltages. The NCP51510 is available in

PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Pin Function
1	V_{RO}	OUTPUT − Buffered Output of V_{RI} Reference Input pin.
2	V_{CC}	INPUT − Regulator Analog Power Input pin. Connect to the system supply voltage. Bypass V_{CC} to A_{GND} with a 1 μF or greater ceramic capacitor.
3	A_{GND}	Analog Ground
4	V_{RI}	INPUT − External Reference Input for V_{TT} Output (see Figure 1 for typical application)
5	P_{GOOD}	OUTPUT − V_{TT} “Power Good” pin (open drain output)
6	V_{TTS}	INPUT − Remote Sense Input for V_{TT}. The V_{TTS} pin provides accurate remote feedback sensing of the V_{TT} output.
7	$\overline{SS}$	INPUT − Suspend Shutdown Control Input. CMOS compatible. Logic HIGH = enable, logic LOW = shutdown. Connect to VDDQ for normal operation.
8	P_{GND}	Power Ground. Internally connected to Low−side MOSFET
9	V_{TT}	OUTPUT − Regulated Power Output pin
10	PV_{CC}	INPUT − Regulator Power Input pin. Internally connected to High−side MOSFET
−	THERMAL PAD	Pad for thermal connection. The exposed pad must be connected to the ground plane using multiple vias for maximum power dissipation performance.

ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
PV_{CC} to P_{GND}	(Note 2)	−	−0.3 to 4.3	V
V_{CC} to A_{GND}	(Note 2)	V_{CC}	−0.3 to 4.3	
V_{RI}, V_{RO}, $\overline{SS}$, P_{GOOD} to A_{GND}	(Note 2)	−	−0.3 to (V_{CC} + 0.3)	
V_{TT} to P_{GND}	(Note 2)	−	−0.3 to (PV_{CC}ï	

RECOMMENED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
V_{TT} Output Voltage Range	V_{TT}, V_{TTS}	0.5 to 1.5	V
PV_{CC} Input Voltage Range (Power)	PV_{CC}	1.1 to 3.6	
V_{CC} Input Voltage Range (Analog)	V_{CC}	2.7 to 3.6	
Logic Voltage Range	$\overline{SS}$, P_{GOOD}	0 to V_{CC}	
Operating Ambient Temperature Range	T_A	−40 to +125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

PV_{CC} = 1.8 V; V_{CC} = 3.3 V; V_{RI} = V_{TTS} = 1.25 V; $\overline{SS}$ = V_{CC}; (circuit of Figure 1, −40°C ≤ (T_J = T_A) ≤ 125°C; unless otherwise noted. Typical values are at T_A = +25°C

Parameter	Conditions		Symbol	Min	Typ	Max	Unit
OUTPUT							
V_{TT} Output Voltage Range	PV_{CC} > (V_{TT} + $V_{DROPOUT}$)		V_{TT}	0.5		1.5	V
V_{TT} Load Regulation	−1 A ≤ I_{TT} ≤ +1 A		ΔV_{LOAD}	−4		+4	mV
V_{TT} Line−Regulation	1.4 V ≤ PV_{CC} ≤ 3.3 V, I_{OUT} = ±100 mA		ΔV_{LINE}		1		
Feedback−Voltage Error	V_{RI} to V_{TTS}, I_{TT} = ±200 mA	T_A = −40°C to 125°C	V_{TTS}	−17		+17	

ELECTRICAL CHARACTERISTICS

PV_{CC} = 1.8 V; V_{CC} = 3.3 V; V_{RI} = V_{TTS} = 1.25 V; $\overline{SS}$ = V_{CC}; (circuit of Figure 1, −AGE LOCKOUT6189 Tm0 Tw(P-14.10 64-1 8992 58 0 TD-.008(m.0018 Tc

General*

The NCP51510 is a source/sink tracking termination regulator specifically designed for low input voltage and low external component count systems where space is a key application parameter. The NCP51510 integrates a high−performance, low−dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, a remote sensing input (V) should be connected to the positive terminal of the output capacitors as a separate trace from the high current path of the V output.

Generation of Internal Voltage Reference

The V output voltage is regulated to (and tracks with) the voltage on the V Reference input. When the V input is configured for standard DDR termination applications, the V Reference input can be set by an external equivalent ratio voltage divider connected to the memory supply bus (V). The NCP51510 supports V voltages from 0.5 V to 1.5 V.

Generation of Internal Voltage Reference (cont)

When the V output is configured for DDR termination applications, it provides a separate V output reference voltage for the memory application. The V Reference Output pin is a buffered version of the V Reference Input, and is capable of sourcing and sinking a load of ±5 mA. The V output becomes active when the V input > 0.45 V and the V power rail is above the UVLO threshold. The V Reference Output is independent of the $\overline{SS}$ pin (Suspend Shutdown) state.

Fault Detection and Shutdown Function

When the $\overline{SS}$ “Suspend Shutdown” input pin is driven high, the NCP51510 regulator begins normal operation, with the Soft Start circuit gradually increasing output current during the first 200 μs in order to reduce the input surge currents at startup, with full current available after the 200 μs Soft−Start circuitry has timed out.

When the $\overline{SS}$ input is driven low, the V output is discharged to P through an internal 8 Ω MOSFET. The V output remains on when the $\overline{SS}$ input is driven low. The NCP51510 provides an open−drain P “Power Good” output that goes high when the V Sense input is within ±150 mV of the V Reference Input. The P output de−asserts within 10 μs after the V Sense input exceeds the size of the P window. During initial V startup, P asserts high 2 ms after the V Sense input enters P window. Because the P output is open−drain, an external pull−up resistor is required (100 kΩ*) between P and a stable active supply voltage rail.

Thermal Shutdown with Hysteresis

If the NCP51510 is to operate in elevated temperatures for long durations, care should be taken to ensure that the maximum operating junction temperature is not exceeded. To guarantee safe operation, the NCP51510 provides on−chip thermal shutdown protection. When the chip junction temperature exceeds 165°C*, the part will shutdown. When the junction temperature falls back, to 150°C*, the device resumes normal operation. If the junction temperature exceeds the thermal shutdown threshold, the V output is shut off, discharged by the 8 Ω internal discharge MOSFET.

Output Capacitor

Output stability is guaranteed for V output capacitance C from 10 μF to 220 μF. The ESR of C between 2 mΩ and 50 mΩ is required to maintain stability. Use the formula below to calculate the application’s transient response:

$$\Delta I_{TT(pp)} \times ESR = \Delta V_{TT(pp)}$$

Where:
$\Delta I_{TT(pp)}$ is the maximum peak−to−peak load current delta and $\Delta V_{TT(pp)}$ is the allowable peak−to−peak voltage tolerance.

*Typical values are used with the application description text. Please refer to the Electrical Specifications Table for a more detailed list of MIN, MAX and TYPICAL values.

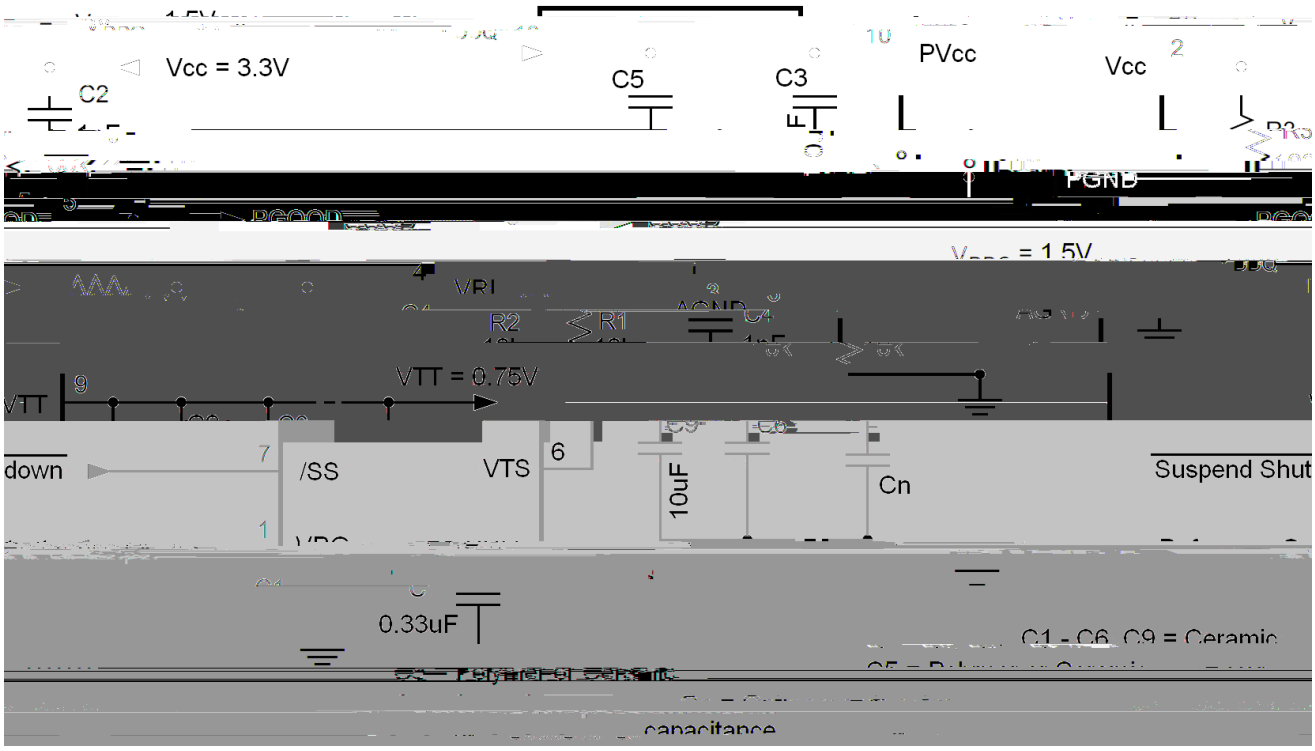

Figure 1. Standard Application Schematic for NCP51510