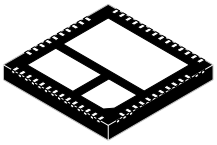
NCP5360R

Integrated Driver and MOSFET

The NCP5360R integrates a MOSFET driver, high-side MOSFET and low-side MOSFET into a 8mm x 8mm 56-pin QFN package. The driver and MOSFETs have been optimized for high-current DC-DC buck power conversion applications. The NCP5360R integrated solution greatly reduces package parasitics and board space compared http/onsemi.com



–

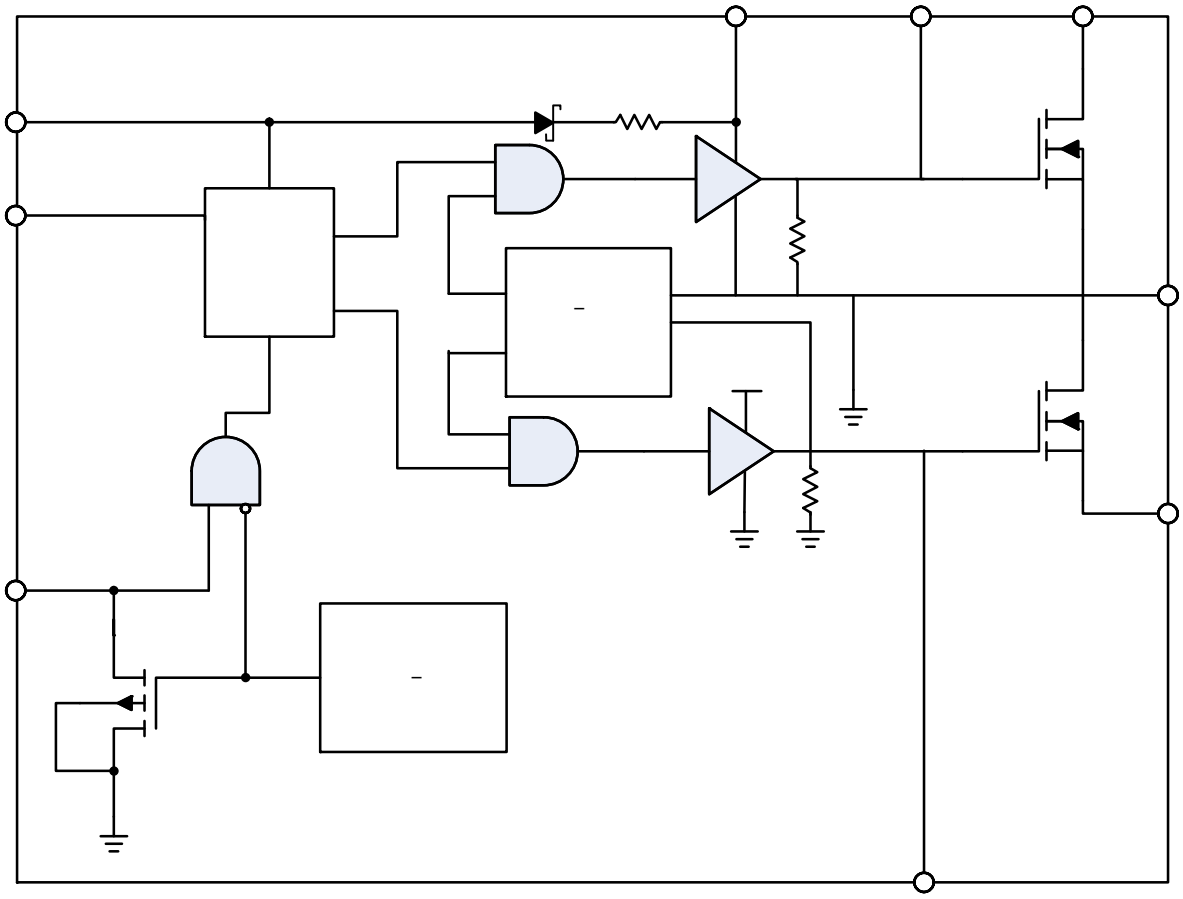


Figure 2. Simplified Block Diagram

PIN CONNECTIONS

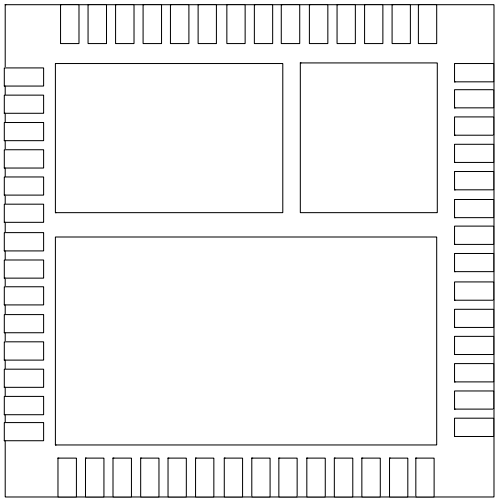


Figure 3. Pin Connections

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
–		
–		
–		

Table 2. ABSOLUTE MAXIMUM RATINGS

Pin Symbol	Pin Name	Min	Max
		–	
		–	
		–	
		– –	
		–	
		–	

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
–	θ		°
–	θ		°
			°
		–	°

Table 4. OPERATING RANGES

Rating	Symbol	Min	Typ	Max	Unit

ELECTRICAL CHARACTERISTICS

APPLICATION INFORMATION

Theory of Operation

The NCP5360R is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high−side and low−side MOSFETs.

Undervoltage Lockout

GH and GL are held low until VCIN reaches 4.5 V during startup. The PWM signals will control the gate status when the VCIN threshold is exceeded.

Power-On Reset

Power-On Reset feature is used to protect against an abnormal status during startup. When the initial soft-start voltage is greater than 2.75 V, the switch node pin is monitored. If VSWH is higher than 2.25 V, the low-side FET is turned on to discharge the output capacitors. The fault mode will latch and DISB# will be forced low until the part is recycled. When the input voltage is higher than 4.5 V and DISB# is high, the part will enter normal operation.

Bi-Directional DISB# Signal

Fault modes such as Power-On Reset, Overtemperature and Undervoltage Lockout will assert the DISB# pin. This will pull down the DRON of the controller as well, thus shutting the controller down.

Low−Side Driver

The low−side driver is designed to drive a ground referenced low $R_{DS(on)}$ N−Channel MOSFET. The voltage rail for the low−side driver is internally connected to VCIN and CGND.

High−Side Driver

The high−side driver is designed to drive a floating low $R_{DS(on)}$ N−channel MOSFET. The gate voltage for the high-side driver is developed by a bootstrap circuit referenced to Switch Node (VSWH) pin.

The bootstrap circuit is comprised of the internal bootstrap diode, and an external bootstrap capacitor. When the NCP5360R is starting up, the VSWH pin is at ground, so the bootstrap capacitor will charge up to VCIN through the bootstrap diode. When the PWM input goes high, the high−side driver will begin to turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the VSWH pin will rise. When the high−side MOSFET is fully on, the switch node will be at 12 V, and the BST pin will be at 12 V plus the charge of the bootstrap capacitor (approaching 24 V).

The bootstrap capacitor is recharged when the switch node goes low during the next cycle.

Safety Timer and Overlap Protection Circuit

It is very important that MOSFETs in a synchronous buck regulator do not both conduct at the same time. Excessive shoot−through or cross−conduction can damage the MOSFETs, and even a small amount of cross−conduction will cause a decrease in the power conversion efficiency.

The NCP5360R prevents cross conduction by monitoring the status of the MOSFETs and applying the appropriate amount of “dead−time” or the time between the turn off of one MOSFET and the turn on of the other MOSFET.

When the PWM input pin goes high, the gate of the low-side MOSFET (GL pin) will go low after a propagation delay (tpdlDRVL). The time it takes for the low−side MOSFET to turn off (tfDRVL) is dependent on the total charge on the low−side MOSFET gate. The NCP5360R monitors the gate voltage of both MOSFETs and the switchnode voltage to determine the conduction status of the MOSFETs. Once the low−side MOSFET is turned off an internal timer will delay (tpdhDRVH) the turn on of the high−side MOSFET.

Likewise, when the PWM input pin goes low, the gate of the high-side MOSFET (GH pin) will go low after the propagation delay (tpdlDRVH). The time to turn off the high−side MOSFET (tfDRVH) is dependent on the total gate charge of the high−side MOSFET. A timer will be triggered once the high−side MOSFET has stopped conducting, to delay (tpdhDRVL) the turn on of the low−side MOSFET.

When the PWM input is between V_{PWM_LO} and V_{PWM_HI} for longer than 200 ns, both the high-side and low-side MOSFETs will be turned off. The PWM input will need to exceed V_{PWM_HI} to resume normal switching of the MOSFETs.

Power Supply Decoupling

The NCP5360R can source and sink relatively large currents to the gate pins of the MOSFETs. In order to maintain a constant and stable supply voltage (VCIN) a low ESR capacitor should be placed near the power and ground pins. A 1 μF to 4.7 μF multi layer ceramic capacitor (MLCC) is usually sufficient.

Input Pins

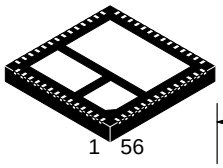
The PWM input and the Output Disable pins of the NCP5360R have internal protection for Electro Static Discharge (ESD), but in normal operation they present a relatively high input impedance. If the PWM controller does not have internal pull−down resistors, they should be added externally to ensure that the driver outputs do not go high before the controller has reached its undervoltage lockout threshold.

Bootstrap Circuit

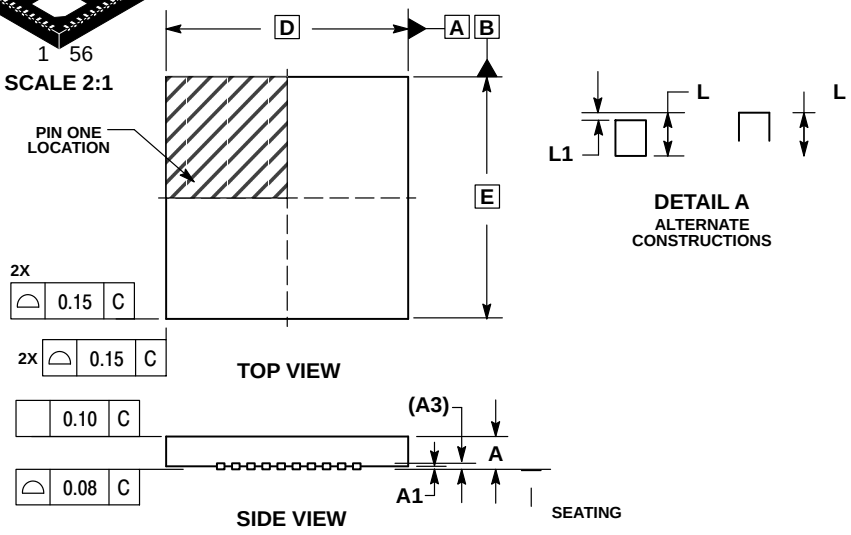
The bootstrap circuit uses a charge storage capacitor (C_{BST}) and the internal diode. The bootstrap capacitor must have a voltage rating that is able to withstand twice the maximum supply voltage. A minimum 50 V rating is recommended. A bootstrap capacitance greater than 100 nF is recommended. A good quality ceramic capacitor should be used.

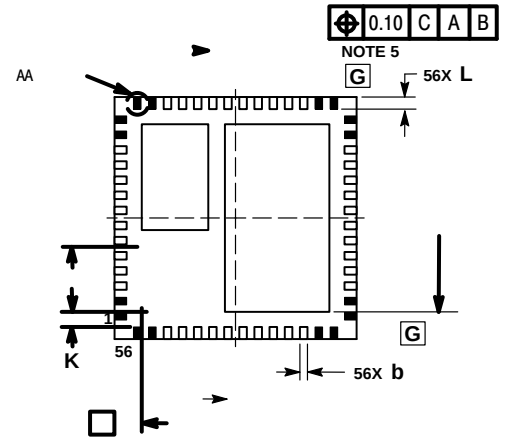
QFN56 8x8, 0.5P
CASE 485AY
ISSUE O

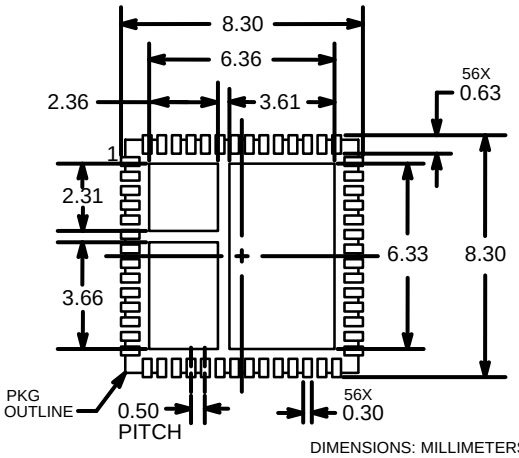
DATE 12 FEB 2009



SCALE 2:1







DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	**98AON38216E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**QFN56 8x8, 0.5P**	**PAGE 1 OF 1**