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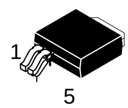
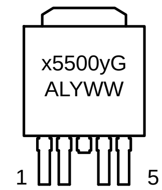
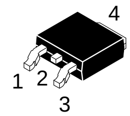
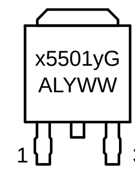


Pin 1. EN
2. V_{in}
TAB, 3. GND
4. V_{out}
5. NC/ADJ

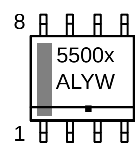




Pin 1. V_{in}
TAB, 2. GND
3. V_{out}

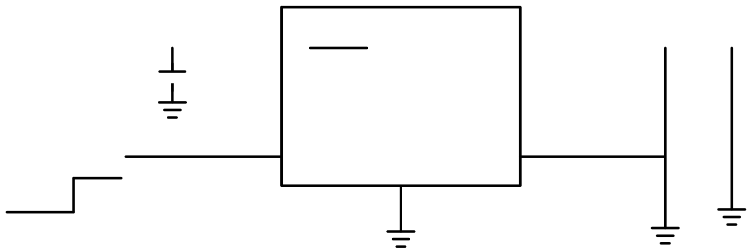


x	= P (NCP), V (NCV)
5500/1	= Device Code
y	= Output Voltage
	L = 1.5 V
	T = 3.3 V
	U = 5.0 V
	W = Adjustable
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package



See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

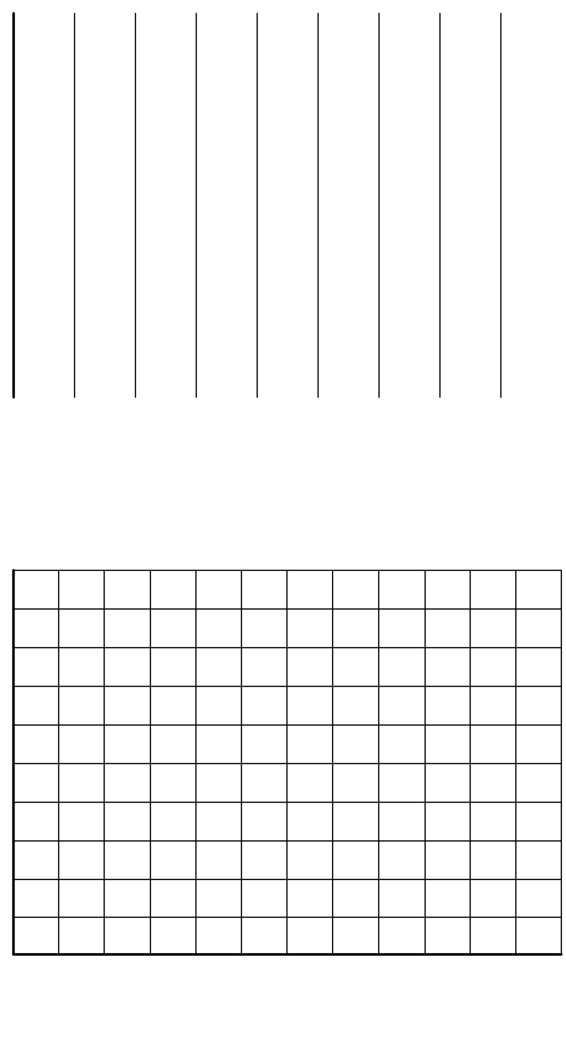
NOTE: Some of the devices on this data sheet have been . Please refer to the table on page 10.

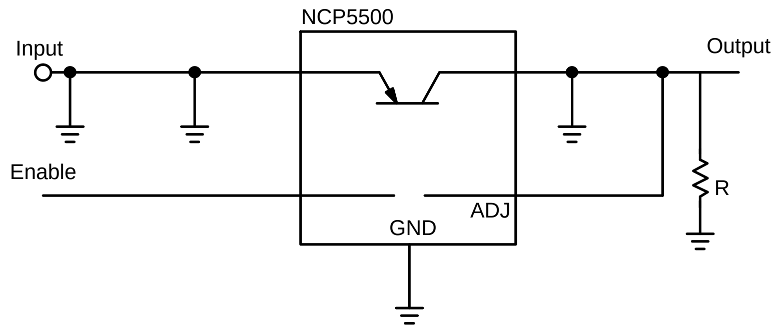


Input Voltage (Note 1)				

V_{in} = 2.5 V or V_{out} + 1.0 V (whichever is higher), C_{in} = 10 µF, C_{out} = 4.7 µF, for typical values T_A = 25°C, for min/max values T_A = −40°C to 85°C (NCP Version), T_A = −40°C to 125°C (NCV Version) unless otherwise noted (Note 13).

Output Voltage (Note 14) 5 V Regulator 3.3 V Regulator 1.5 V Regulator ADJ Regulator	V_{out}	T_A = 25°C, I_{out} = 50 mA		V_{NOM}±2.9%		 V V V
Output Voltage (Note 8) 5 V Regulator 3.3 V Regulator 1.5 V Regulator ADJ Regulator	V_{out}	1.0 mA < I_{out} < 500 mA	(−4.9%) 4.755 3.138 1.427 1.189	V_{NOM} 5.0 3.3 1.5 1.25	(+4.9%) 5.245 3.462 1.574 1.311	 V V V
Line Regulation	REG_{LINE}	I_{out} = 50 mA 2.5 V or (V_{out} + 1.0 V) < V_{in} < 16 V	−1.0	0.1	1.0	%
Load Regulation	REG_{LOAD}	1.0 mA < I_{out} < 500 mA	−1.0	0.35	1.0	%
Dropout Voltage (Note 9) 5.0 V Version 3.3 V Version 1.5 V Version (Note 10) Adjustable Version (Note 11)	V_{DO}	 I_{out} = 1.0 mA, ΔV_{out} = −2% I_{out} = 500 mA, ΔV_{out} = −2% I_{out} = 1.0 mA, ΔV_{out} = −2% I_{out} = 500 mA, ΔV_{out} = −2% I_{out} = 1.0 mA, ΔV_{out} = −2% I_{out} = 500 mA, ΔV_{out} = −2% I_{out} = 1.0 mA, ΔV_{out} = −2% I_{out} = 500 mA, ΔV_{out} = −2%	 – – – – – – – –	 5 230 5 230 – – 5 230	 90 700 90 700 1073 1073 90 700	mV
Ground Current	I_{GND}	I_{out} = 100 µA I_{out} = 500 mA		300 10	500 20	µA mA
Disable Current in Shutdown (NCP5500, NCV5500)	I_{SD}	Adjustable and 1.5 V versions All other versions		30 40	50 50	µA
Current Limit	$I_{out(LIM)}$	V_{out} = 90% of $V_{out(nom)}$	500	700	900	mA
Ripple Rejection Ratio (Notes 9 & 14)	RR	120 Hz I_{out} = 100 mA, 1 kHz 10 kHz	– – –	75 75 70	– – –	dB
Output Noise Voltage (Notes 12 & 14)	V_n	f = 10 Hz to 100 kHz, V_{in} = 2.5 V V_{out} = 1.25 V, I_{out} = 1.0 mA f = 10 Hz to 100 kHz, V_{in} = 2.5 V V_{out} = 1.25 V, I_{outo} u t				




NCP5500
Input
Output
Enable
R
ADJ
GND

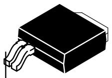
$$V_{out} = \left(1.25\ V - \left[60E{-}9 \cdot \frac{(R_1 \cdot R_2)}{(R_1 + R_2)}\right]\right) \cdot \left(\frac{(R_1 + R_2)}{R_2}\right)$$

$$P_{D(max)} = \left[V_{in(max)} - V_{out(min)}\right] I_{out(max)} + V_{in(max)} I_{GND} \qquad \text{(eq. 1)}$$

$$R_{\theta JA} = \frac{(150^{\circ}C - T_A)}{P_D} \qquad \text{(eq. 2)}$$

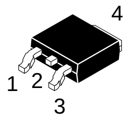
$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \qquad \text{(eq. 3)}$$

[redacted]00 / Tape & Reel
[redacted]3 0 0 8 361.7008 547.T)
[redacted]



DPAK−5, CENTER LEAD CROP
CASE 175AA
ISSUE B

DATE 15 MAY 2014



SCALE 1:1

DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

SOIC 8 NB
CASE 751–07
ISSUE AK

DATE 16 FEB 2011