

NCP59801

PIN FUNCTION DESCRIPTION

Pin No. DFNW8	Pin No. WDFNW6	Pin Name	Description
1, 2	1	OUT	Regulated output voltage. The output should be bypassed with small 4.7 μ F ceramic capacitor
7, 8	6	IN	Input voltage supply pin
5	4	EN	Chip enable: Applying $V_{EN} < 0.4$ V disables the regulator, Pulling $V_{EN} > 1$ V enables the LDO
6	5	PG	Power Good, open collector. Use 10 k Ω to 100 k Ω pull-up resistor connected to output or input voltage
4	3	GND	Common ground connection
3	2	FB	Adjustable output feedback pin (for adjustable version only)
3	2	SNS	

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THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, WDFNW6–2x2, 0.65 Pitch Package			
Thermal Resistance, Junction–to–Ambient (Note 3)	$R_{\theta JA}$	60	°C/W
Thermal Resistance, Junction–to–Case (top)	$R_{\theta JC(top)}$	167	°C/W
Thermal Resistance, Junction–to–Case (bottom) (Note 4)	$R_{\theta JC(bot)}$	6.9	°C/W
Thermal Resistance, Junction–to–Board	$R_{\theta JB}$	6.6	°C/W
Characterization Parameter, Junction–to–Top	Ψ_{JT}	4.6	°C/W
Characterization Parameter, Junction–to–Board	Ψ_{JB}	6.5	°C/W

Thermal Characteristics, DFNW8–3x3, 0.65 Pitch Package

Thermal Resistance, Junction–to–Ambient (Note 3)	$R_{\theta JA}$	44.4	°C/W
Thermal Resistance, Junction–to–Case (top)	$R_{\theta JC(top)}$	115	°C/W
Thermal Resistance, Junction–to–Case (bottom) (Note 4)	$R_{\theta JC(bot)}$	6.9	°C/W
Thermal Resistance, Junction–to–Board	$R_{\theta JB}$	6.3	°C/W
Characterization Parameter, Junction–to–Top	Ψ_{JT}	5.7	°C/W
Characterization Parameter, Junction–to–Board	Ψ_{JB}	6.3	°C/W

- The junction–to–ambient thermal resistance under natural convection is obtained in a simulation on a high–K board (2s2p, 1in², 1oz Cu) following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51–2a.
- The junction–to–case (bottom) thermal resistance is obtained by simulating a cold plate test on the IC exposed pad. Test description can be found in the ANSI SEMI standard G30–88.

ELECTRICAL CHARACTERISTICS

–40°C ≤ T_J ≤ 125°C; V_{IN} = V_{OUT(NOM)} + 0.5 V or 1.6 V, whichever is greater, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 4.7 μF, V_{EN} = V_{IN}, unless otherwise noted. Typical values are at T_J = +25°C (Note 5).

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Input Voltage	V _{IN}		1.6	–	5.5	V
Under Voltage Lock Out	V _{UVLO}		–	1.5	–	V
Output Voltage Accuracy	V _{OUT}	V _{IN} = V _{OUT(NOM)} + 0.5 V, I _{OUT} = 1 mA T _J = +25°C	–0.7	V _{NOM}	+0.7	%

V_{IN} = V_{OUT(NOM)} + 0.5 V to 5.5 V,
0.1 mA ≤ I_{OUT} ≤

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ELECTRICAL CHARACTERISTICS (continued)

$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$; $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 1.6 V , whichever is greater, $I_{OUT} = 1\text{ mA}$, $C_{IN} = C_{OUT} = 4.7\text{ }\mu\text{F}$, $V_{EN} = V_{IN}$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$ (Note 5).

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
EN Pin Threshold Voltage	V_{ENH}	EN Input Voltage "H"	1	–	V_{IN}	V
	V_{ENL}	EN Input Voltage "L"	0	–	0.4	
EN Pull Down Current	I_{EN}	$V_{EN} = 5\text{ V}$	–	0.2	0.6	μA
Power Good Threshold Voltage	V_{PGUP}	Output Voltage Raising	–	95	–	%
	V_{PGDW}	Output Voltage Falling	–	90	–	
Power Good Output Voltage Low	V_{PGLO}	$I_{PG} = 1\text{ mA}$, Open drain	–	30	100	mV

Turn–

TYPICAL CHARACTERISTICS

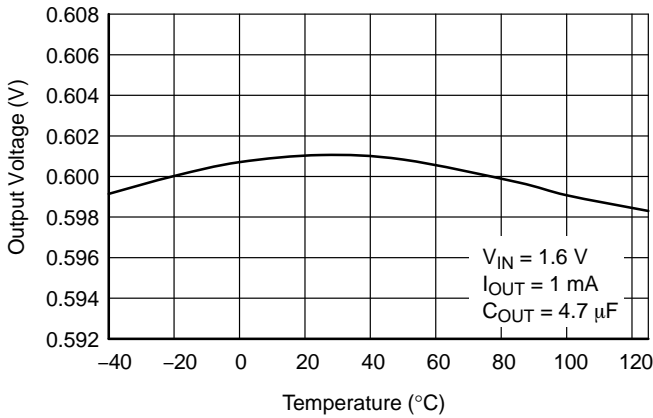


Figure 2. Output Voltage vs. Temperature – $V_{OUT} = 0.6\text{ V}$ (Adjustable Reference)

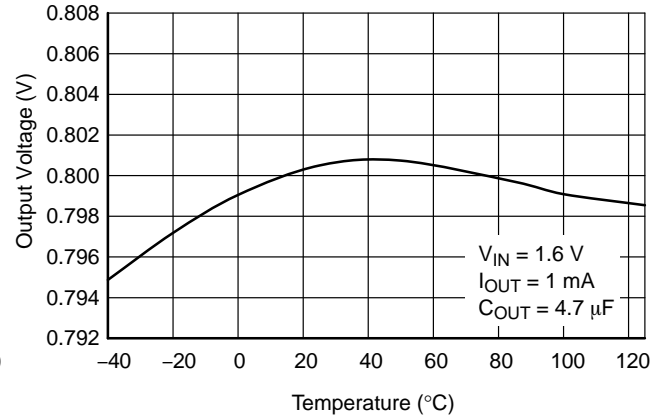


Figure 3. Output Voltage vs. Temperature – $V_{OUT} = 0.8\text{ V}$

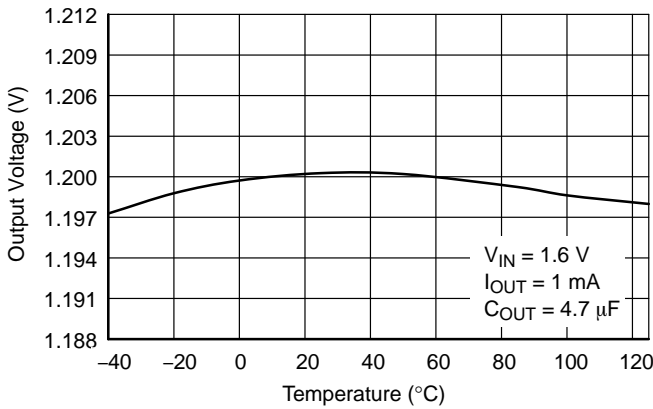


Figure 4. Output Voltage vs. Temperature – $V_{OUT} = 1.2\text{ V}$

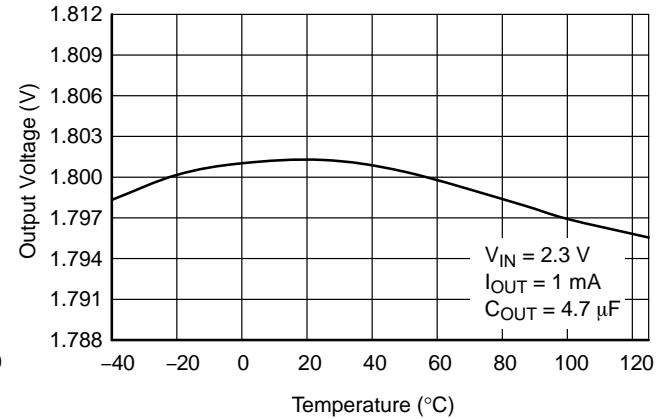


Figure 5. Dropout Voltage vs. Temperature – $V_{OUT} = 1.8\text{ V}$

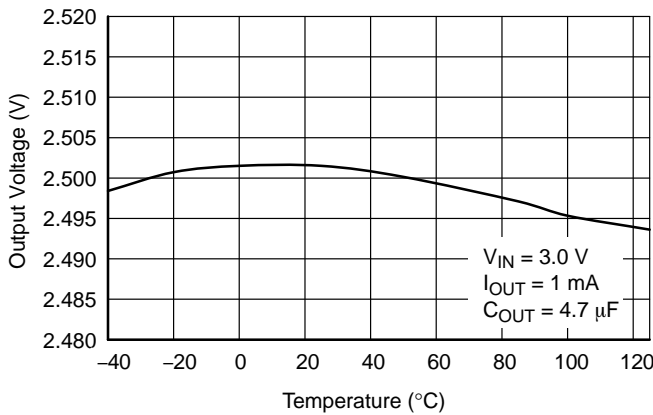


Figure 6. Output Voltage vs. Temperature – $V_{OUT} = 2.5\text{ V}$

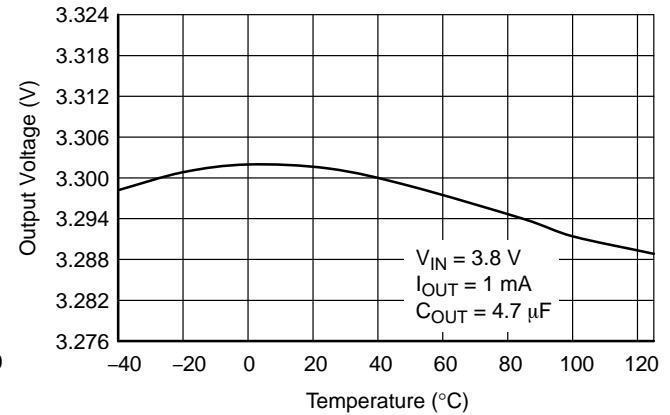


Figure 7. Dropout Voltage vs. Temperature – $V_{OUT} = 3.3\text{ V}$

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TYPICAL CHARACTERISTICS (continued)

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TYPICAL CHARACTERISTICS (continued)

Figure 14. Line Regulation vs. Temperature

Figure 15. Load Regulation vs. Temperature

Figure 16. Quiescent Current vs. Temperature

Figure 17. Quiescent Current vs. Input Voltage

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TYPICAL CHARACTERISTICS (continued)

Figure 20. Enable Threshold vs. Temperature

Figure 21. Power Good Threshold vs.
Temperature

Figure 22. Power Good Saturation Voltage vs.
Temperature

Temperature

TYPICAL CHARACTERISTICS (continued)

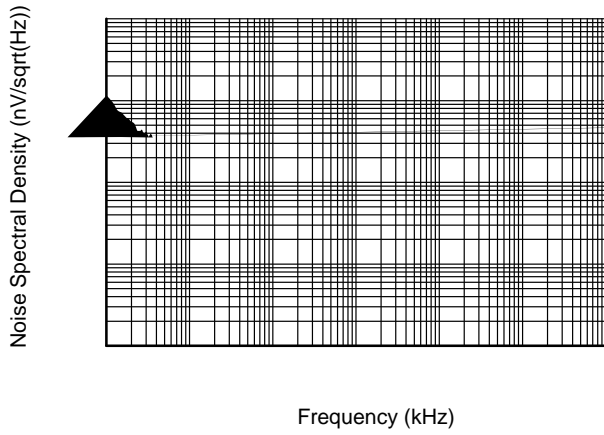


Figure 26. Output Voltage Noise Spectral Density for $V_{OUT} = 2.5\text{ V}$, $C_{OUT} = 4.7\ \mu\text{F}$

Figure 27. Controlled Output Voltage Slew Rate

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ORDERING INFORMATION

Device part no. *	Voltage Option	Marking	Option	Package	Shipping†
NCP59801CMTWADJTAG	ADJ	AM	With Active Output Discharge, Slew Rate 5 mV/μs	WDFNW6 2x2 (Pb-Free)	3000 / Tape & Reel
NCP59801CMLADJTGC	ADJ	P9801 ADJ	With Active Output Discharge, Slew Rate 5 mV/μs	DFNW8 3x3 (Pb-Free)	3000 / Tape & Reel
NCP59801CML180TCG	1.8 V	P9801 180	With Active Output Discharge, Slew Rate 5 mV/μs	DFNW8 3x3 (Pb-Free)	3000 / Tape & Reel
NCP59801CML330TCG	3.3 V	P9801 330	With Active Output Discharge, Slew Rate 5 mV/μs	DFNW8 3x3 (Pb-Free)	3000 / Tape & Reel

*Other voltage options and slew rate options (D / E / F) upon request.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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PACKAGE DIMENSIONS

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PACKAGE DIMENSIONS

DFNW8 3x3, 0.65P
CASE 507AD
ISSUE A

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION *b* APPLIES TO PLATED TERMINAL

