Buck Converter - Synchronous
3 MHz, 2 A

NCP6324, NCV6324

The NCP/NCV6324, a family of synchronous buck converters, which is optimized to supply different sub systems of portable applications powered by one cell Li−ion or three cell Alkaline/NiCd/ NiMH batteries. The devices are able to deliver up to 2 A on an external adjustable voltage. Operation with 3 MHz switching frequency allows employing small size inductor and capacitors. Input supply voltage feedforward control is employed to deal with wide

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NCP6324/D

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP6324BMTAATBG			

PIN DESCRIPTION

Pin	Name	Type	Description
1	PGND	Power Ground	Power Ground for power, analog blocks. Must be connected to the system ground.
2	SW	Power Output	Switch Power pin connects power transistors to one end of the inductor.
3	AGND	Analog Ground	Analog Ground analog and digital blocks. Must be connected to the system ground.
4	FB	Analog Input	Feedback Voltage from the buck converter output. This is the input to the error amplifier. This pin is connected to the resistor divider network between the output and AGND.
5			

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		Min	Max	
Analog Pins DC non switching: AVIN, PG, FB, EN	V_{A-DC}	−0.3	6.0	V
Power Pins DC non switching: PVIN, SW	V_{P-DC}	−0.3	6.0	V
Between PVIN, PGND pins, transient 3 ns − 3 MHz	V_{P-TR}	−0.3	7.5	V
Human Body Model (HBM) ESD Rating are (Note 1)	ESD HBM		2000	V
Machine Model (MM) ESD Rating (Note 1)	ESD MM		200	V
Latchup Current (Note 2)	I_{LU}	−100	100	mA
Junction Temperature Range (Note 3)	T_{JMAX}	−40	TSD	°C
Storage Temperature Range	T_{STG}	−55	150	°C
Thermal Resistance Junction−to−Top Case (Note 4)	R_{JC}	12		°C/W
Thermal Resistance Junction−to−Board (Note 4)	R_{JB}	30		°C/W
Thermal Resistance Junction−to−Ambient (Note 4)	R_{JA}	62		°C/W
Power Dissipation (Note 5)	P_D	1.6		W
Moisture Sensitivity Level (Note 6)	MSL	1		−

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115.
2. Latchup Current per JEDEC standard: JESD78 Class II.
3. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.

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ELECTRICAL CHARACTERISTICS (V_{IN} = 3.6 V, V_{OUT} = 1.8 V, L = 1 μH, C = 10 μF, typical values are referenced to T_J = 25°C, Min

ELECTRICAL CHARACTERISTICS

TYPICAL OPERATING CHARACTERESTICS

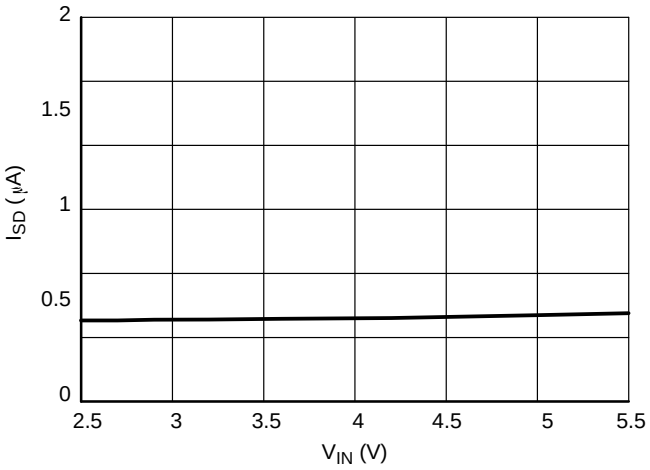


Figure 3. Shutdown Current vs. Input Voltage (EN = Low, T_A = 25°C)

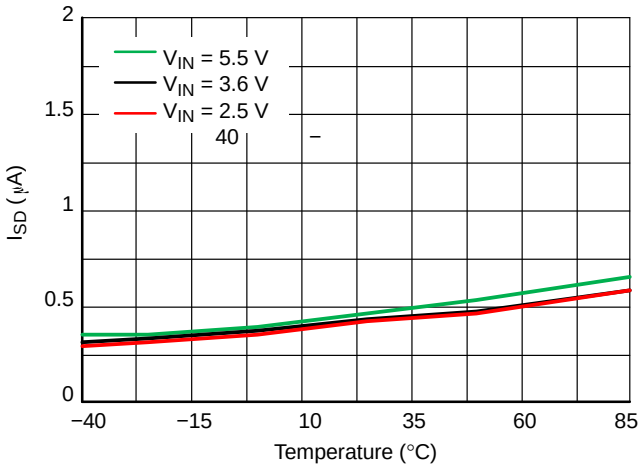


Figure 4. Shtudown Current vs. Temperature (EN = Low, V_{IN} = 3.6 V)

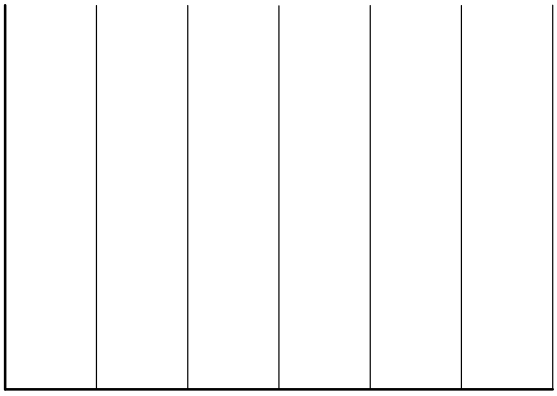


Figure 5. Quiescent Current vs. Input Voltage (EN = High, Open Loop, V_{OUT} = 1.8 V, T_A = 25°C)

Figure 6. Quiescent Current vs. Temperature (EN = High, Open Loop, V_{OUT} = 1.8 V, V_{IN} = 3.6 V)

Figure 7. Efficiency vs. Output Current and Input Voltage (V_{OUT} = 1.05 V, T_A = 25°C)

Figure 8. Efficiency vs. Output Current and Input Voltage (V_{OUT} = 1.8 V, T_A = 25°C)

TYPICAL OPERATING CHARACTERESTICS

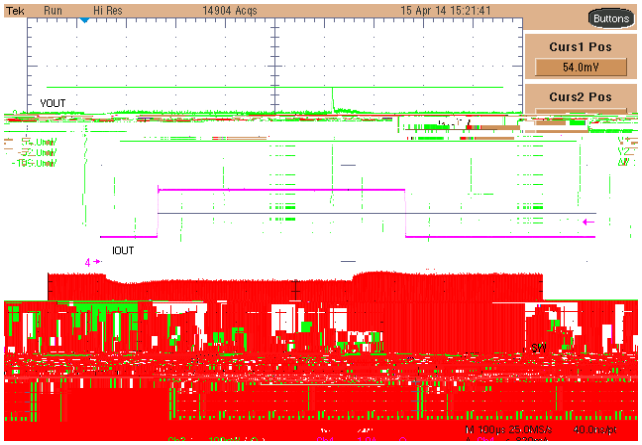
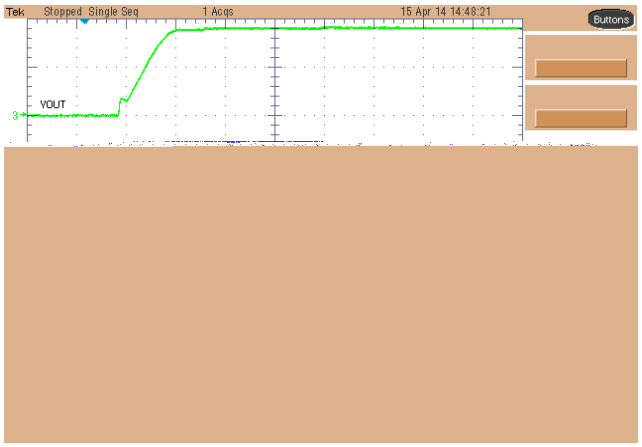


Figure 13. Load Transient Response (V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 500 mA to 1500 mA, L = 1 μH, C_{OUT} = 10 μF)

Figure 14. Power Up Sequence and Inrush Current in



hysteresis is required on power good comparator before signal going high again. When not used, it is allowed to leave this pin unconnected.

Soft Start

A soft start limits inrush current when the converter is enabled. After a minimum 80 μs delay time following the enable signal, the output voltage starts to ramp up. Ramping from 10% to 90% of the target voltage takes 100 μs, typical.

Active Output Discharge

An output discharge operation is active in when EN is low. A discharge resistor (500 Ω typical) is enabled in this condition to discharge the output capacitor through SW pin.

Cycle

APPLICATION INFORMATION

Output Filter Design Considerations

The output filter introduces a double pole in the system at a frequency of

$$f_{LC} = \frac{1}{2 \cdot \quad \cdot \sqrt{L \cdot C}} \qquad \text{(eq. 2)}$$

The internal compensation network design of the NCP/NCV6324 is optimized for the typical output filter comprised of a 1.0 μH inductor and a 10 μF ceramic output capacitor, which has a double pole frequency at about 50 kHz. Other possible output filter combinations may have a double pole around 50 kHz to have optimum operation with the typical feedback network. Normal selection range of the inductor is from 0.47 μH to 4.7 μH, and normal selection range of the output capacitor is from 4.7 μF to 22 μF.

Inductor Selection

The inductance of the inductor is determined by given peak−to−peak ripple current IL_PP of approximately 20% to 50% of the maximum output current IOUT_MAX for a trade−off between transient response and output ripple. The inductance corresponding to the given current ripple is

$$L = \frac{\left(V_{IN} - V_{OUT}\right) \cdot V_{OUT}}{V_{IN} \cdot f_{SW} \cdot I_{L\_PP}} \qquad \text{(eq. 3)}$$

The selected inductor must have high enough saturation current rating to be higher than the maximum peak current that is

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{I_{L\_PP}}{2} \qquad \text{(eq. 4)}$$

The inductor also needs to have high enough current rating based on temperature rise concern. Low DCR is good for efficiency improvement and temperature rise reduction. Table 1 shows some recommended inductors for high power applications and Table 2 shows some recommended inductors for low power applications.

Table 1. LIST OF RECOMMENDED INDUCTORS FOR HIGH POWER APPLICATIONS

Manufacturer	Part Number	Case Size (mm)	L (μH)	Rated Current (mA) (Inductance Drop)

In applications with all ceramic output capacitors, the main ripple component of the output ripple is VOUT_PP(C). So that the minimum output capacitance can be calculated regarding

LAYOUT CONSIDERATIONS

Electrical Layout Considerations

Good electrical layout is a key to make sure proper operation, high efficiency, and noise reduction. Electrical layout guidelines are:

- Use wide and short traces for power paths (such as PVIN, VOUT, SW, and PGND) to reduce parasitic inductance and high−frequency loop area. It is also good for efficiency improvement.
- The device should be well decoupled by input capacitor and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission.
- SW node should be a large copper pour, but compact because it is also a noise source.
- It would be good to have separated ground planes for PGND and AGND and connect the two planes at one point. Directly connect AGND pin to the exposed pad and then connect to AGND ground plane through vias. Try best to avoid overlap of input ground loop and output ground loop to prevent noise impact on output regulation.
- Arrange a “quiet” path for output voltage sense and feedback network, and make it surrounded by a ground plane.

Thermal Layout Considerations

Good thermal layout helps high power dissipation from a small package with reduced temperature rise. Thermal layout guidelines are:

- The exposed pad must be well soldered on the board.
- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC and/or underneath the exposed pad to connect the inner ground layers to reduce thermal impedance.
- Use large area copper especially in top layer to help thermal conduction and radiation.
- Do not put the inductor to be too close to the IC, thus the heat sources are distributed.