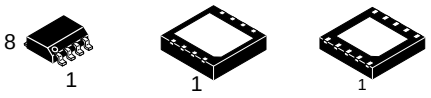
D al MOSFET Ga e D i e , High Pe f mance

NCP81075



SOIC−8 NB CASE 751−07 | **DFN8 CASE 506CY** | **WDFN10 CASE 511CE**

Introduction

The NCP81075 is a high performance dual MOSFET gate driver optimized to drive the gates of both high and low side power MOSFETs in a synchronous buck converter. The NCP81075 uses an on−chip bootstrap diode to eliminate the external discrete diode. A high floating top driver design can accommodate HB voltage as high as 180 V. The low−side and high−side are independently controlled and match to 4 ns between the turn−on and turn−off of each other. Independent Under−Voltage lockout is provided for the high side and low side driver forcing the output low when the drive voltage is below a specific threshold.

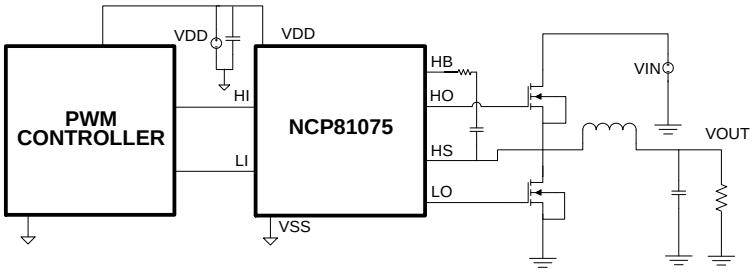
Features

- Drives Two N-Channel MOSFETs in High-Side and Low-Side Configuration
- Floating Top Driver Accommodates Boost Voltage up to 180 V
- Switching Frequency up to 1 MHz
- 20 ns Propagation Delay Times
- 4 A Sink, 4 A Source Output Currents
- 8 ns Rise / 7 ns Fall Times with 1000 pF Load
- UVLO Protection
- Specified from −40°C to 140°C
- Offered in SOIC−8 (D), DFN8 (MN), WDFN10 (MT) Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

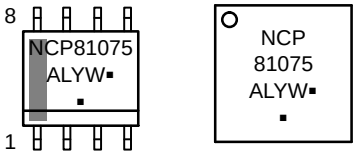
Applications

- Telecom and Datacom
- Isolated Non−Isolated Power Supply Architectures
- Class D Audio Amplifiers
- Two Switch and Active Clamp Forward Converters

Simplified Application Diagram

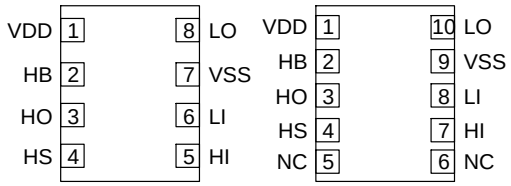


MARKING DIAGRAMS



NCP81075 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PINOUT DIAGRAMS



NCP81075
(top views)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81075DR2G	SOIC8 (Pb−Free)	2500 / Tape & Reel
NCP81075MNTXG	DFN8 (Pb−Free)	4000 / Tape & Reel
NCP81075MTTXG	WDFN10 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Table 1. PIN DESCRIPTION

Pin No. SOIC/DFN8	Pin No. WDFN10	Symbol	Description
1	1	VDD	Positive Supply to the Lower Gate Driver
2	2	HB	High Side Bootstrap Supply
3	3	HO	High Side Output
4	4	HS	High−Side Source
5	7	HI	High−Side Input
6	8	LI	Low−Side Input
7	9	VSS	Negative Supply Return
8	10	LO	Low−Side Output
−	5,6	NC	No Connect

Table 2. MAXIMUM RATINGS

Parameter		Value	Units
VDD		−0.3 to 24	V
V_{HB}		−0.3 to 200	V
V_{HO}	DC	V_{HS} – 0.3 to V_{HB} + 0.3	V
	Repetitive Pulse < 100 ns	V_{HS} − 2 to V_{HB} + 0.3, (V_{HB} − V_{HS} < 24)	
V_{HS}	DC	−20 to 200 − VDD	V
V_{LO}	DC		

I_{HBSO}	HB to V_{SS} operating current	f = 500 kHz, C_{LOAD} = 0		0.1		mA
INPUT						
V_{HIH}, V_{LIH}	Input rising threshold		2.7			V
V_{HIL}, V_{LIL}	Input fai707 ref4.577					

Table 5. ELECTRICAL CHARACTERISTICS
Unless otherwise stated: $T_A = T_J = -40°C$ to 140°C; VDD = VHB = 12 V, VHS = VSS = 0 V, No load on LO or HO

Parameter		Test Condition	Min	Typ	Max	Units
HO GATE DRIVER						
V_{HOL}	Low level output voltage	I_{HO} = 100 mA		0.1	0.40	V
V_{HOH}	High level output voltage	I_{HO} = −100 mA, $V_{HOH} = V_{HB} - V_{HO}$		0.15	0.40	
	Peak pull−up current	V_{LO} = 0 V		4		A
	Peak pull−down current	V_{LO} = 12 V				

Internal Block Diagram

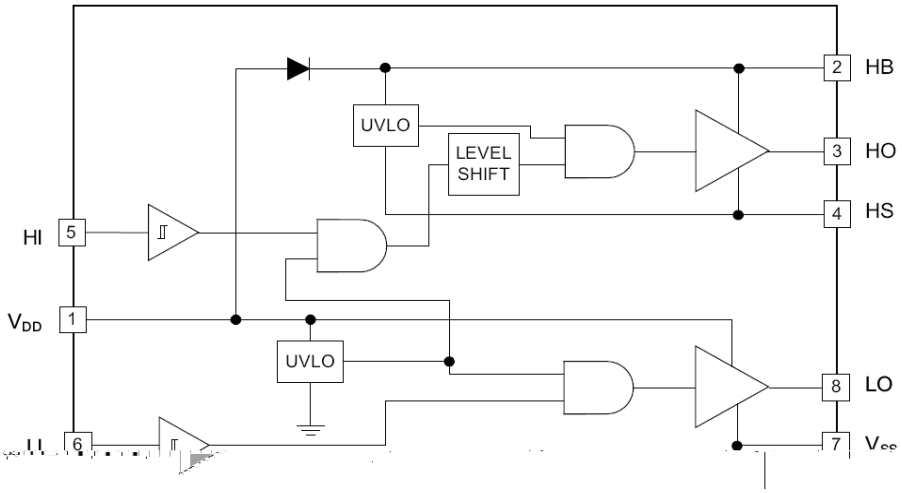


Figure 1. Internal Block Diagram

Timing Diagrams

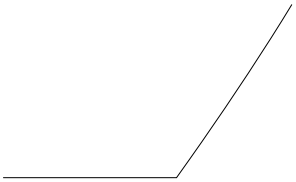


Figure 2. UVLO

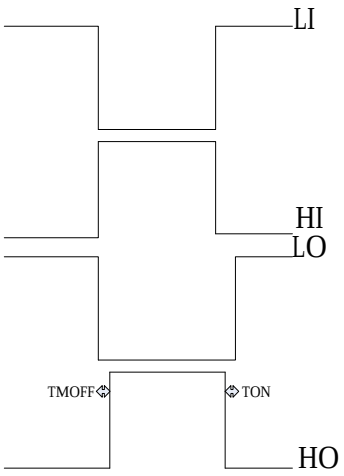
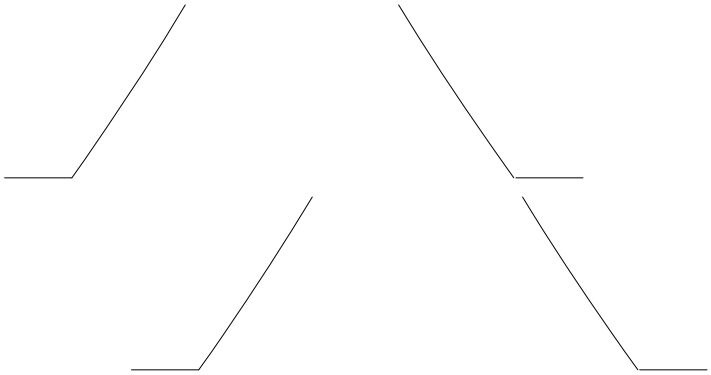
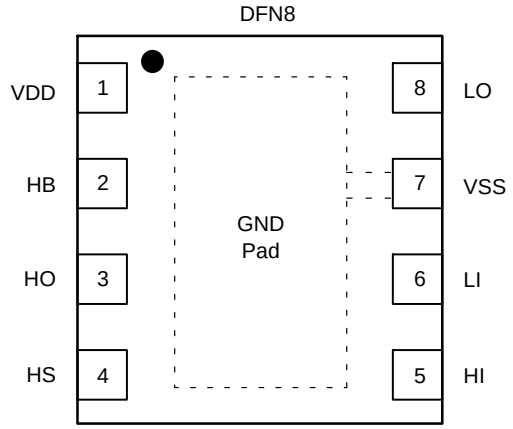
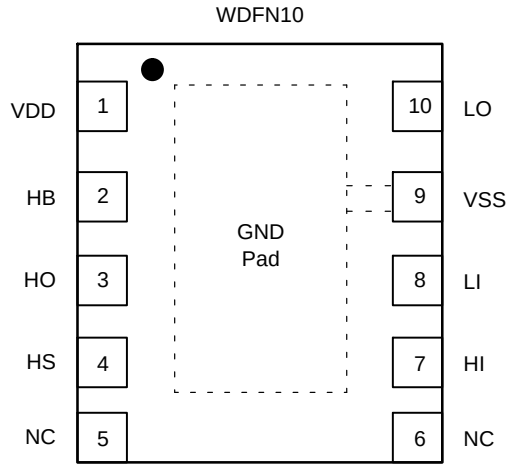


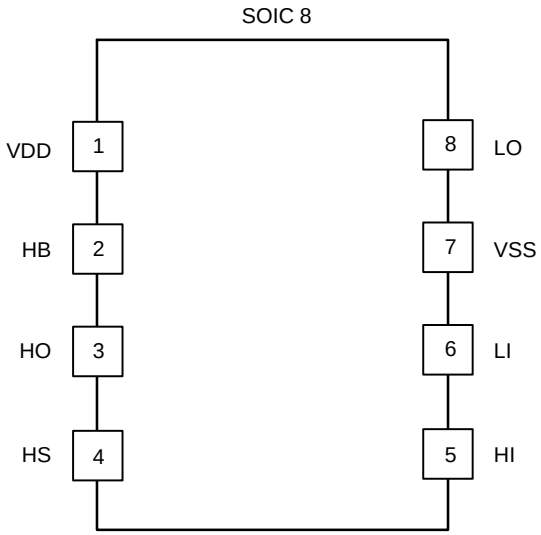
Figure 3. TMON and TMOFF



PINOUT DIAGRAMS







Note: The V_{SS} Pin and the GND Pad are internally connected.

Figure 5. NCP81075 Top View

TYPICAL CHARACTERISTICS

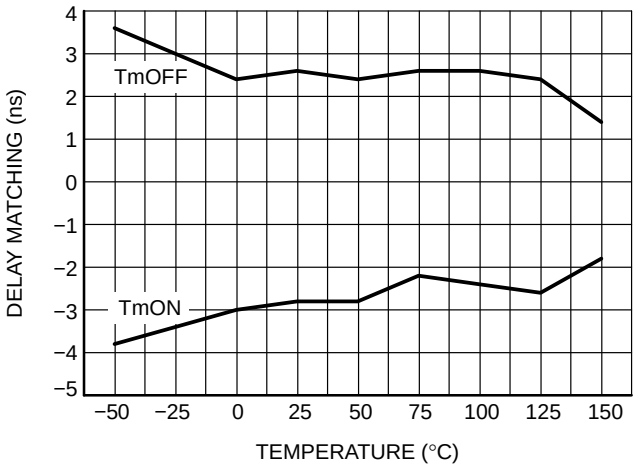


Figure 6. Delay Matching vs. Temperature

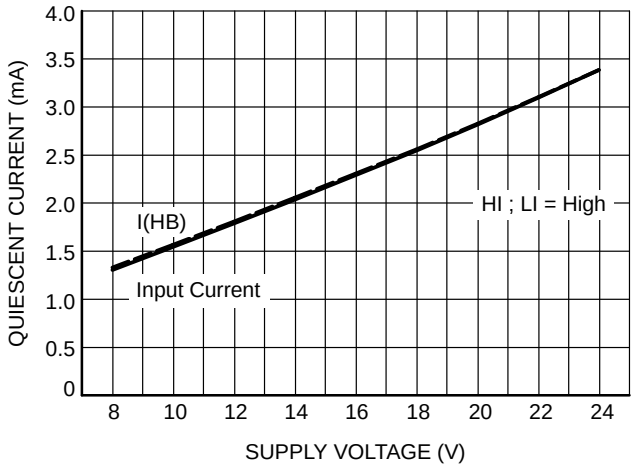


Figure 7. Quiescent Current vs. Supply Voltage High

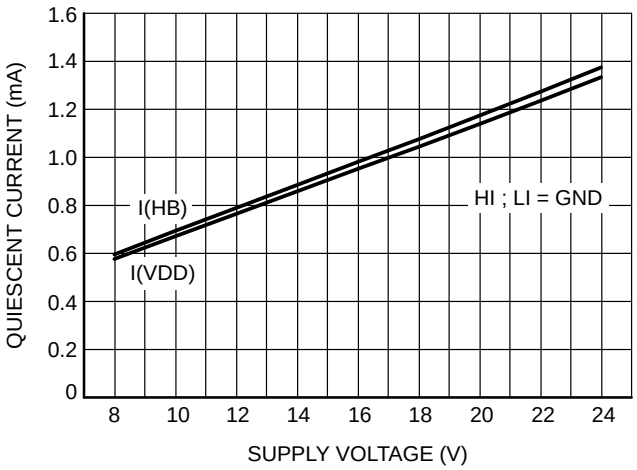


Figure 8. Quiescent Current vs. Supply Voltage Low

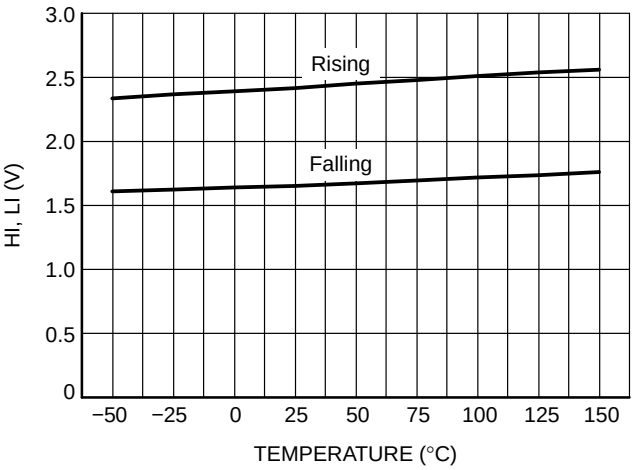


Figure 9. Input Threshold vs. Temperature

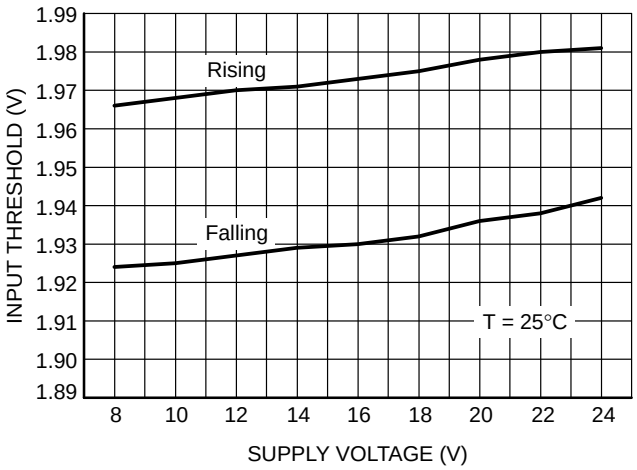


Figure 10. Input Threshold vs. Supply Voltage

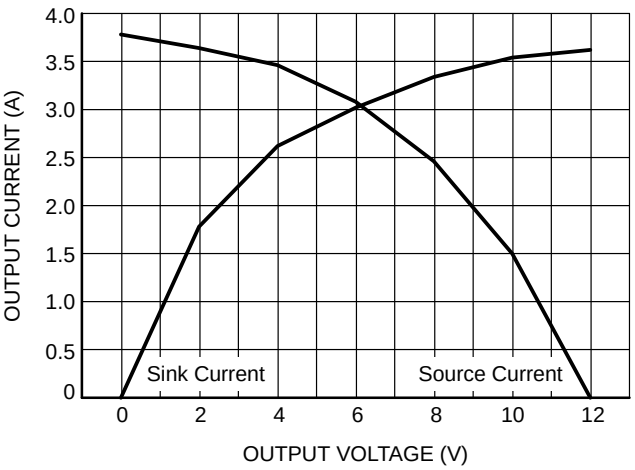


Figure 11. Output Current vs. Output Voltage

TYPICAL CHARACTERISTICS

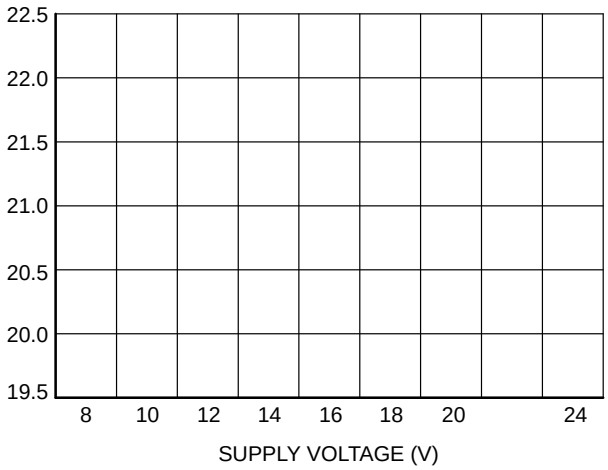


Figure 12. Propagation Delay vs. Supply Voltage

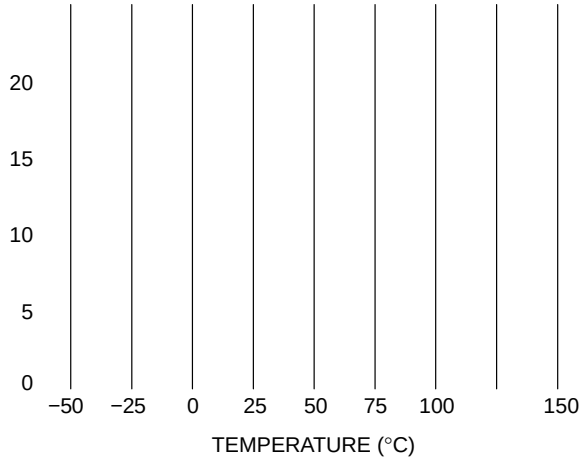


Figure 13. Propagation Delay vs. Temperature

APPLICATION INFORMATION

The NCP81075 is a high performance dual MOSFET gate driver optimized for driving the gates of both high side and low side power MOSFETs in a synchronous buck converter topology. A high and a Low input signals are all that is required to properly drive the high side and low side MOSFETs.

Low−Side Driver

The low side driver is designed to drive low RDS_{ON} N−channel MOSFETs. The typical output resistances for the driver are 1.5 ohms for sourcing and 1 ohm for sinking gate current. Due to the parasitic inductances of the packages, drive circuits and the nonlinearity of the MOSFETs output resistances the recorded peak current is close to 4 A.

The low output resistances allow the driver to have 8 ns rise and 7 ns fall times into a 1 nF load. When the driver is enabled, the driver's output is in phase with LI. When the NCP81075 is disabled, the low side gate is held low.

High−Side Driver

The high side driver is designed to drive a floating low RDS_{ON} N−channel MOSFET. The output resistances for the driver are 1.5 ohms for sourcing and 1 ohm for sinking gate current. The bias voltage for the high side driver is realized by an external bootstrap supply circuit which is connected between the HB and HS Pins.

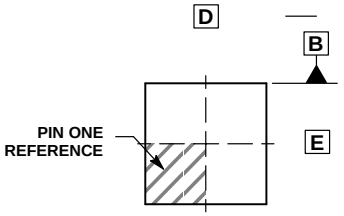
The bootstrap circuit is comprised of only the bootstrap capacitor since the bootstrap diode is internal. When the NCP81075 is starting up, the HS Pin is at ground, the bootstrap capacitor will charge up to VDD through the internal diode. When the HI goes high, the high side driver will begin to turn the high side MOSFET On by pulling charge out of the bootstrap capacitor. As the external MOSFET turns ON, the HS Pin will rise up to VIN, forcing the HB Pin to VIN + V_{BstCap} which is enough gate to source voltage to hold the switch On. To complete the cycle, the MOSFET is switched OFF by pulling the gate down to the voltage at the HS Pin. When the low side MOSFET turns On, the HS Pin is pulled to ground. This allows the bootstrap capacitor to charge up to VDD again. The high−side driver's output is in phase with the HI input. When the driver is disabled, the high side gate is held low.

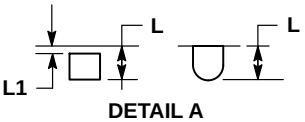
Unlike a Buck regulator at power−up, Boost regulators typically require starting when the HS pin is at the V_{IN} level, instead of GND or the prevailing V_{OUT}ï

DFN8, 4x4, 0.8P
CASE 506CY
ISSUE O

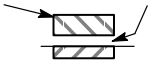
DATE 31 JUL 2014

1
SCALE 2:1





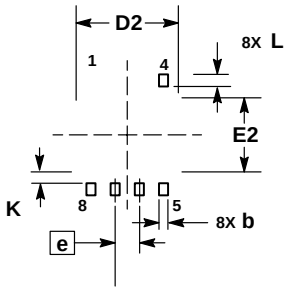
DETAIL A
OPTIONAL CONSTRUCTIONS



DETAIL B

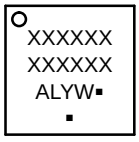
NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	3.28	3.48
E	4.00 BSC	
E2	2.35	2.55
e	0.80 BSC	
K		
L	0.30	0.50



NOTE 3

GENERIC MARKING DIAGRAM*

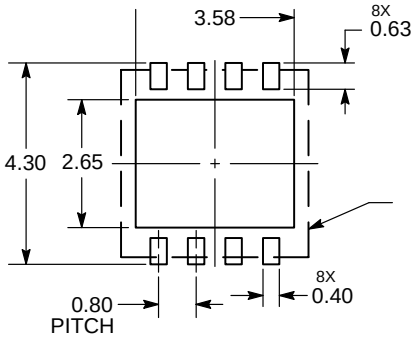


XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

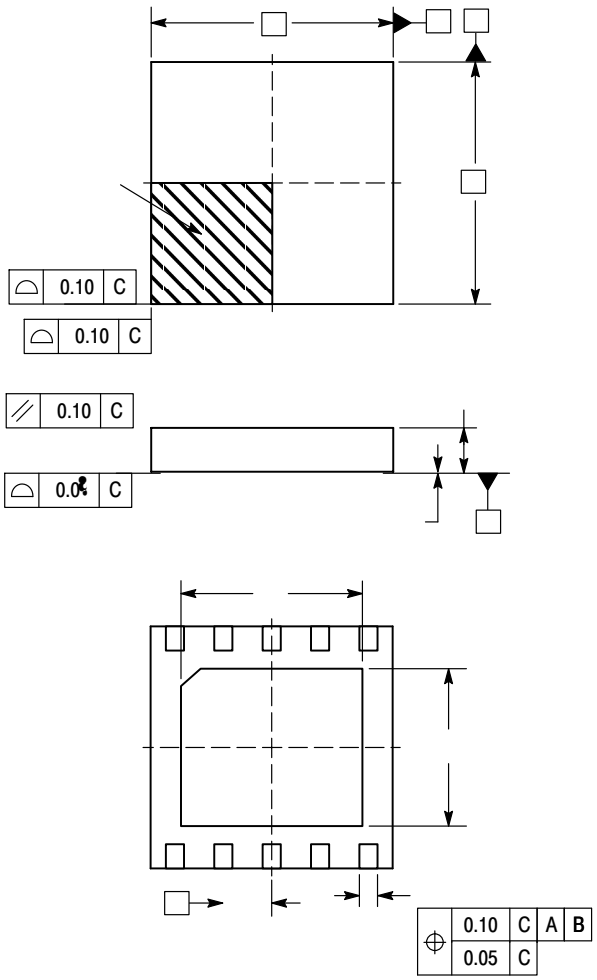
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED

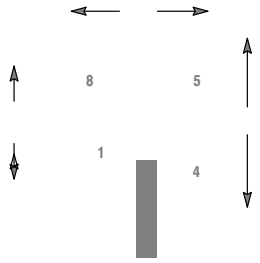


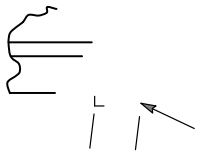
*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.


0.10 C
0.10 C
0.10 C
0.08 C
0.10 C A B
0.05 C

SOIC 8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011





SEATING
PLANE