NCP81381

I g a d D · a d MOSFET

The NCP81381 integrates a MOSFET driver, high−side MOSFET and low−side MOSFET into a single package.

The driver and MOSFETs have been optimized for high−current DC−DC buck power conversion applications. The NCP81381 integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

Features

- Capable of Average Currents up to 25 A
- Capable of Switching at Frequencies up to 2 MHz
- Capable of Peak Currents up to 60 A
- Compatible with 3.3 V or 5 V PWM Input
- Responds Properly to 3−level PWM Inputs
- Option for Zero Cross Detection with 3−level PWM
- ZCD_EN Input for Diode Emulation with 2−level PWM
- Internal Bootstrap Diode
- Undervoltage Lockout
- Supports Intel® Power State 4
- Thermal Warning output
- Thermal Shutdown
- This is a Pb−Free Device

Applications

- Desktop & Notebook Microprocessors

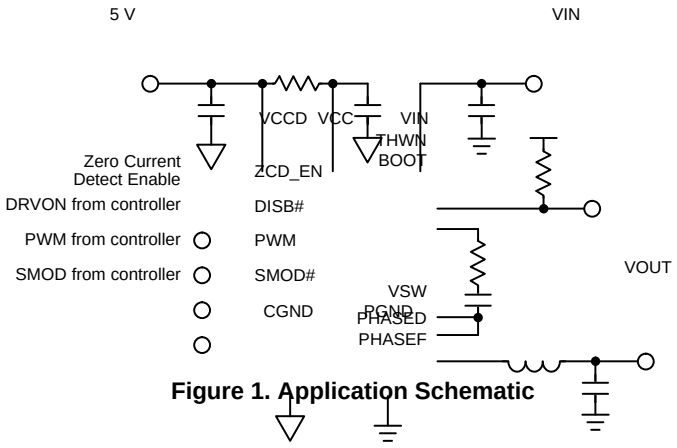
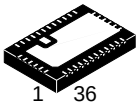


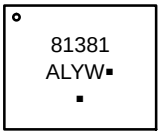
Figure 1. Application Schematic

www.onsemi.com

MARKING DIAGRAM



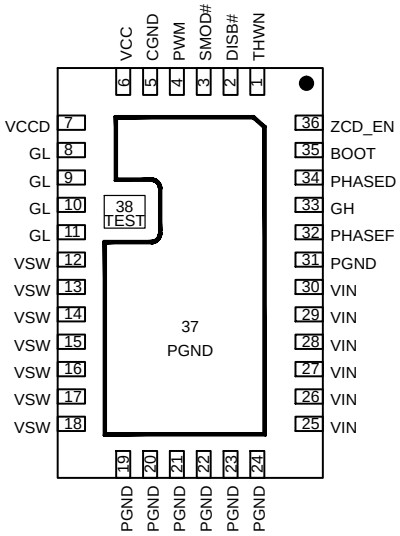
QFN36 6x4
CASE 485DZ



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PINOUT DIAGRAM



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81381MNTXG	QFN36 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

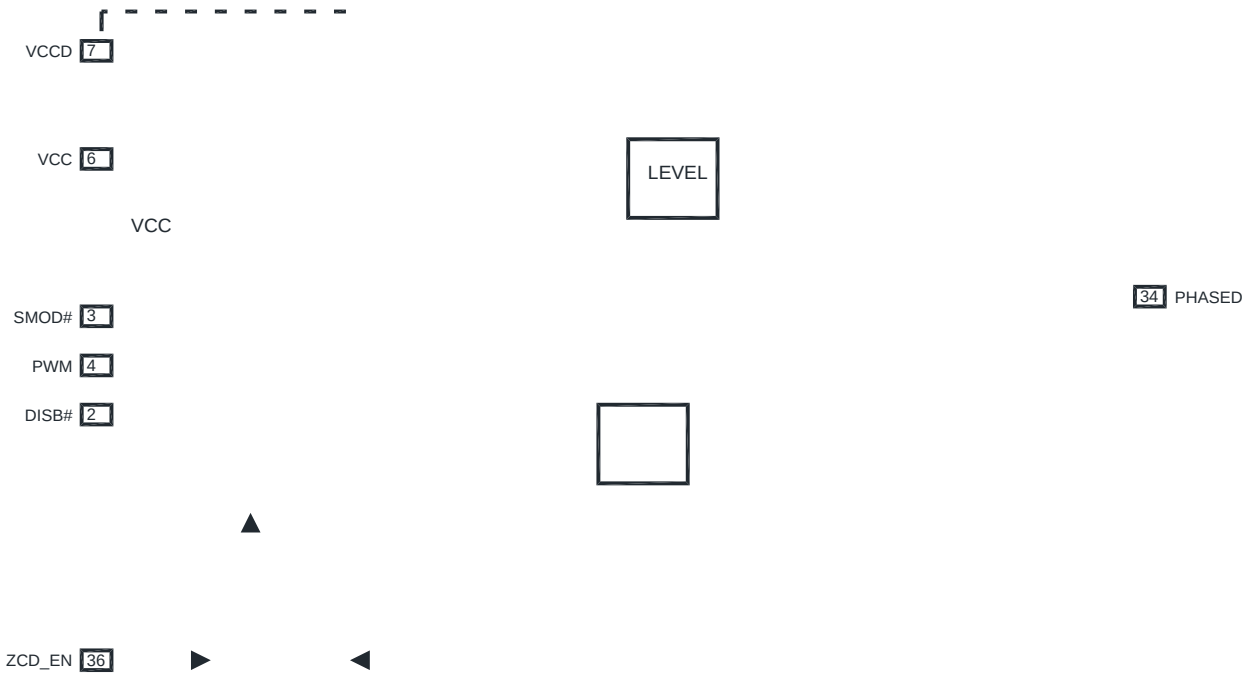


Figure 2. Block Diagram

PIN LIST AND DESCRIPTIONS (continued)

Pin No.	Symbol	Description
19	PGND	

THERMAL INFORMATION

Rating	Symbol	Value	Unit
Thermal Resistance	θ_{JA}	22	°C/W
	$R\Psi_{J-BT}$	2.0	°C/W
	$R\Psi_{J-CT}$	4.0	°C/W

ELECTRICAL CHARACTERISTICS (continued)
(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −10°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCCD SUPPLY CURRENT						
Operating		DISB# = 5 V, ZCD_EN = 5 V, PWM = 400 kHz	–	–	15	mA
Enabled, No switching		DISB# = 5 V, PWM = 0 V, V_{PHASED} = 0 V	–	175	300	μA
Disabled		DISB# = 0 V	–	0.1	1	μA
DISB# INPUT						
Input Resistance		To Ground, @ 25°C	–	461	–	kΩ
Upper Threshold	V_{UPPER}		–	–	2.0	V
Lower Threshold	V_{LOWER}		0.8	–	–	V
Hysteresis		V_{UPPER} – V_{LOWER}	200	–	–	mV
Enable Delay Time	t_{ENABLE}	Time from DISB# transitioning HI to when VSW responds to PWM.	–	–	40	μs
Disable Delay Time	$t_{DISABLE}$	Time from DISB# transitioning LOW to when both output FETs are off.	–	25	50	ns
PWM INPUT						
Input High Voltage	V_{PWM_HI}		2.65	–	–	V
Input Mid−state Voltage	V_{PWM_MID}		1.4	–	2.0	V
Input Low Voltage	V_{PWM_LO}		–	–	0.7	V
Input Resistance	R_{PWM_HIZ}	SMOD# = $V_{SMOD\#\_HI}$ or $V_{SMOD\#\_LO}$	10	–	–	MΩ
Input Resistance	R_{PWM_BIAS}	SMOD# = $V_{SMOD\#\_MID}$	–	63	–	kΩ
PWM Input Bias Voltage	V_{PWM_BIAS}	SMOD# = $V_{SMOD\#\_MID}$	–	1.7	–	V
PWM Propagation Delay, Rising	$tpdl_{GL}$	PWM = 2.25 V to GL = 90%; SMOD# = LOW	–	25	35	ns
PWM Propagation Delay, Falling	$tpdl_{GH}$	PWM = 0.75 V to GH = 90%	–	15	25	ns
Exiting PWM Mid−state Propagation Delay, Mid−to−Low	$T_{PWM\_EXIT\_L}$	PWM = Mid−to−Low to GL = 10%, ZCD_EN = High	–	13	25	ns
Exiting PWM Mid−state Propagation Delay, Mid−to−High	$T_{PWM\_EXIT\_H}$	PWM = Mid−to−High to GH = 10%	–	13	25	ns
SMOD# INPUT						
SMOD# Input Voltage High	V_{SMOD_HI}		2.65	–	–	V
SMOD# Input Voltage Mid−state	$V_{SMOD\#\_MID}$		1.4	–	2.0	V
SMOD# Input Voltage Low	V_{SMOD_LO}		–	–	0.7	V
SMOD# Input Resistance	$R_{SMOD\#\_UP}$	Pull−up resistance to VCC	–	440	–	kΩ
SMOD# Propagation Delay, Falling	$T_{SMOD\#\_PD\_F}$	SMOD# = Low to GL = 90%, PWM = Low	–	26	30	ns
SMOD# Propagation Delay, Rising	$T_{SMOD\#\_PD\_R}$	SMOD# = High to GL = 10%, ZCD_EN = High, PWM = Low	–	15	30	ns
ZCD_EN INPUT						
ZCD_EN Input Voltage High	$V_{ZCD\_EN\_HI}$					

ELECTRICAL CHARACTERISTICS (continued)
(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the

Table 1. LOGIC TABLE

INPUT TRUTH TABLE					
DISB#	**PWM**	**SMOD#** (Note 5)	**ZCD_EN**	**GH**	**GL**
L	X	X	X	L	L
H	H	X	X	H	L
H	L	X	L	L	L
H	L	X	H	L	H
H	MID	H or MID	H	L	ZCD (Note 6)
H	MID	X	L	L	L (Note 7)
H	MID	L	X	L	L (Note 7)

5. PWM input is driven to mid−state with internal divider resistors when SMOD# is driven to mid−state and PWM input is undriven externally.
6. GL goes low following 80 ns de−bounce time, 250 ns blanking time and then SW exceeding ZCD threshold.
7. There is no delay before GL goes low.

Figure 4. Efficiency − 12 V Input, 1.2 V Output, 500 kHz

Figure 5. Efficiency − 19 V Input, 1.2 V Output, 500 kHz

If $V_{SMOD\#\_LO}$ < SMOD# < $V_{SMOD\#\_HI}$ (Mid−State), internal resistances will set undriven PWM pin voltage to Mid−State.

Disable Input (DISB#)

The DISB# pin is used to disable the GH to the High−Side FET to prevent power transfer. The pin has a pull−down resistance to force a disabled state when it is left unconnected. DISB# can be driven from the output of a logic device or set high with a pull−up resistance to VCC.

VCC Undervoltage Lockout

The VCC pin is monitored by an Undervoltage Lockout Circuit (UVLO). VCC voltage above the rising threshold enables the NCP81381.

Table 2. UVLO/DISB# LOGIC TABLE

UVLO	DISB#	Driver State
L	X	Disabled (GH = GL = 0)
H	L	Disabled (GH = GL = 0)
H	H	Enabled (See Table x)
H	Open	Disabled (GH = GL = 0)

Thermal Warning/Thermal Shutdown Output

The THWN pin is an open drain output. When the temperature of the driver exceeds T_{THWN}, the THWN pin will be pulled low indicating a thermal warning. At this point, the part continues to function normally. When the temperature drops T_{THWN_HYS} below T_{THWN}, the THWN pin will go high. If the driver temperature exceeds T_{THDN}, the part will enter thermal shutdown and turn off both MOSFETs. Once the temperature falls T_{THDN_HYS} below T_{THDN}, the part will resume normal operation.

Skip Mode Input (SMOD#)

The SMOD# tri−state input pin has an internal pull−up resistance to VCC. When driven high, the SMOD# pin enables the low side synchronous MOSFET to operate independently of the internal ZCD function. When the SMOD# pin is set low during the PWM cycle it disables the low side MOSFET to allow discontinuous mode operation.

The NCP81381 has the capability of internally connecting a resistor divider to the PWM pin. To engage this mode, SMOD# needs to be placed into mid−state. While in SMOD# mid−state, the IC logic is equivalent to SMOD# being in the high state.

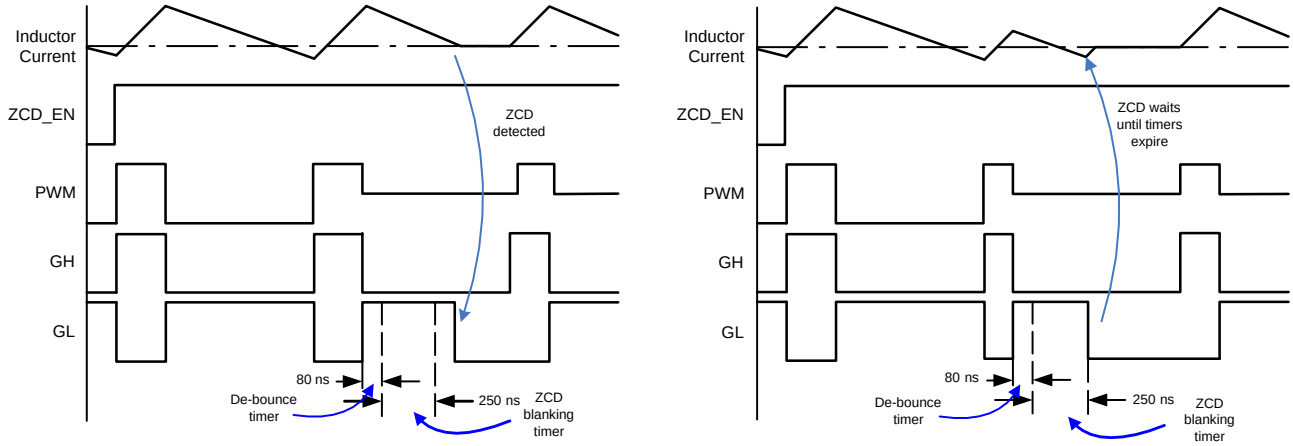


Figure 6. PWM Timing Diagram

NOTES: If the Zero Current Detect circuit detects zero current after the ZCD Wait timer period, the GL is driven low by the Zero Current Detect signal.
If the Zero Current Detect circuit detects zero current before the ZCD Wait timer period has expired, the Zero Current detect signal is ignored and the GL is driven low at the end of the ZCD Wait timer period.

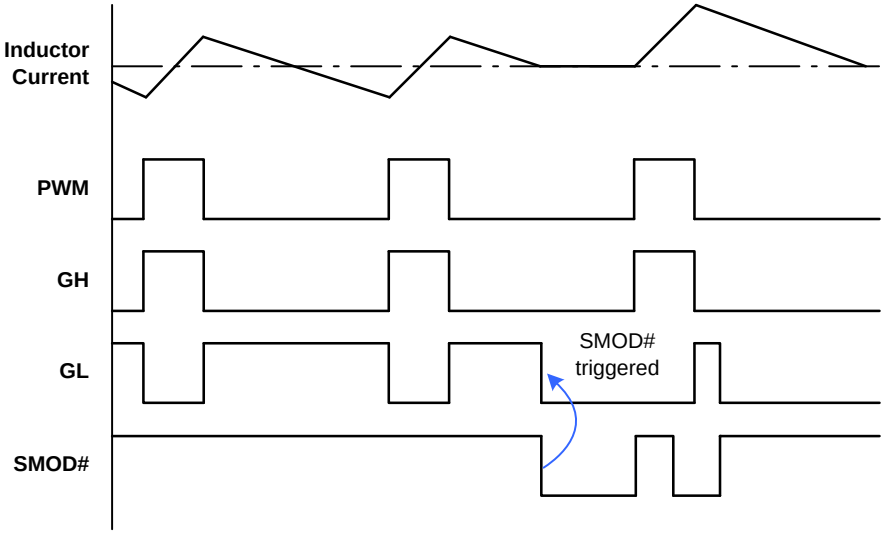


Figure 7. SMOD# Timing Diagram

NOTE: If the SMOD# input is driven low at any time after the GL has been driven high, the SMOD# Falling edge will trigger the GL to go low.
If the SMOD# input is driven low while the GH is high, the SMOD# input is ignored.

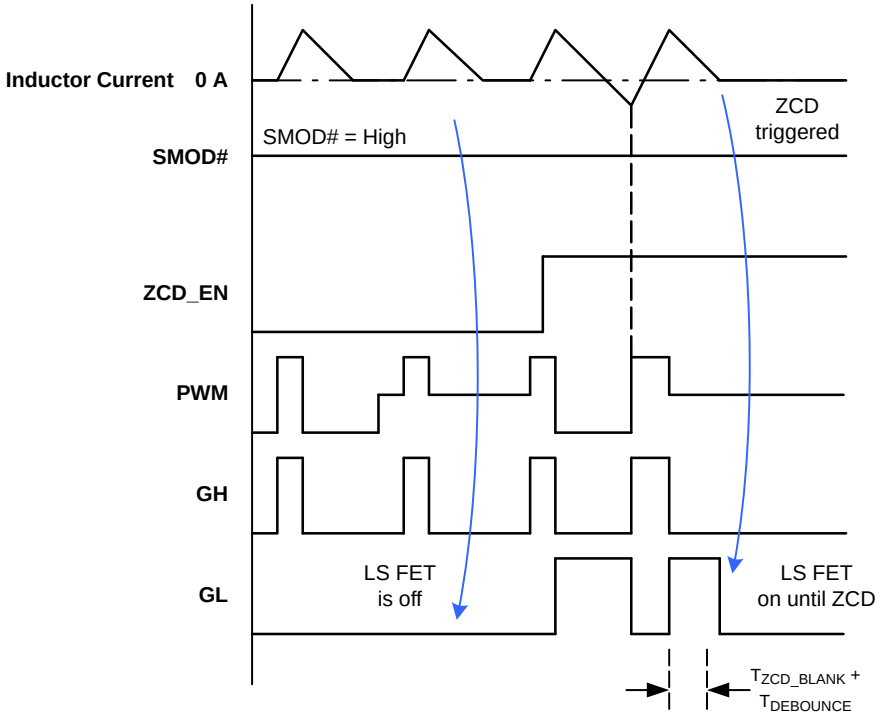


Figure 8. ZCD_EN Timing Diagram

NOTE: When ZCD is enabled by pulling ZCD_EN# high, the NCP81381 keeps the LS FET on until it detects zero current, reducing power loss.

For Use with Controllers with 3−State PWM and No Zero Current Detection Capability:

Table 3. LOGIC TABLE − 3−STATE PWM CONTROLLERS WITH NO ZCD

PWM

For Use with Controllers with 3−state PWM and Zero Current Detection Capability:

Table 4. LOGIC TABLE − 3−STATE PWM CONTROLLERS WITH ZCD

PWM	SMOD#	ZCD_EN	GH	GL
H	L	H	ON	OFF
M	L	H	OFF	OFF
L	L	H	OFF	ON

This section describes operation with controllers that are capable of 3 PWM output levels and have zero current detection during discontinuous conduction mode (DCM).

The SMOD# pin needs to be pulled low (below $V_{SMOD\#\_LO}$).

The ZCD_EN pin needs to either be set to 5 V or left

Recommended PCB Layout
(viewed from top)

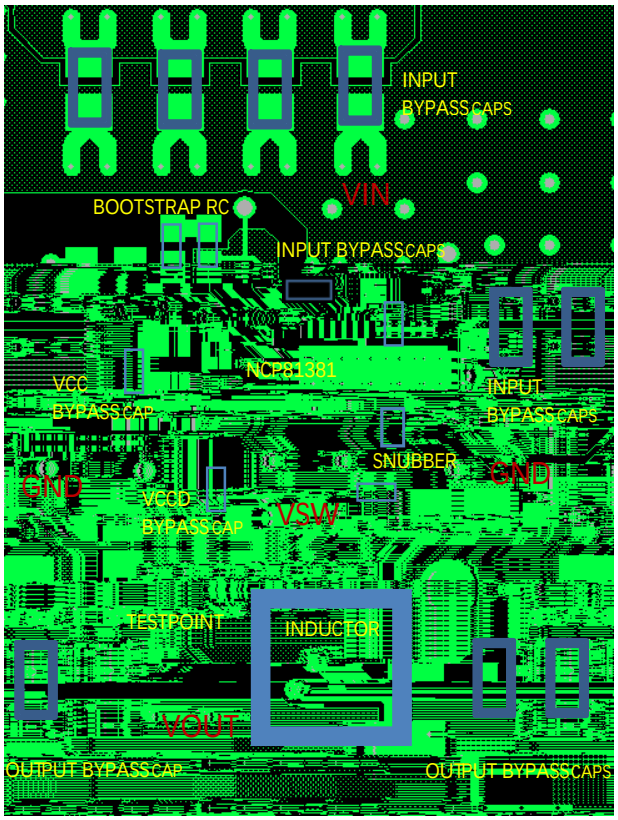


Figure 12. Top Copper Layer

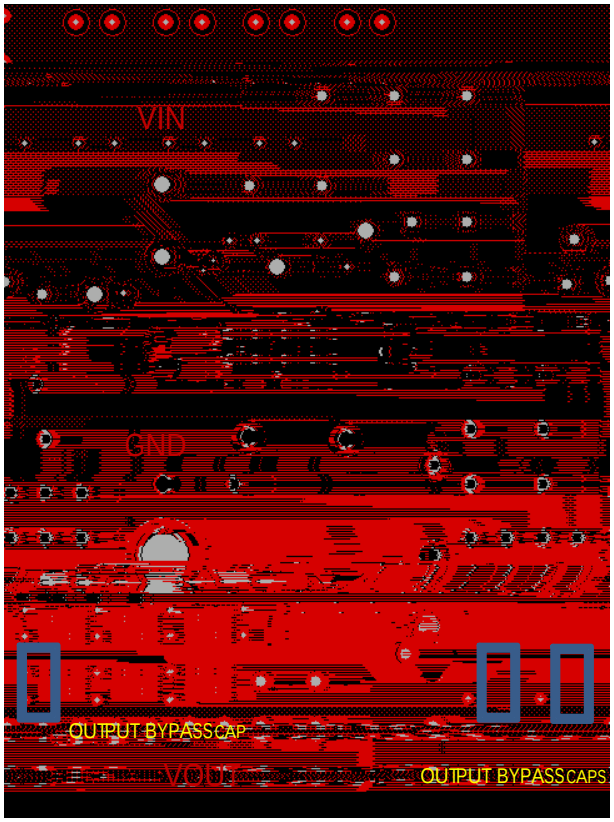


Figure 13. Bottom Copper Layer

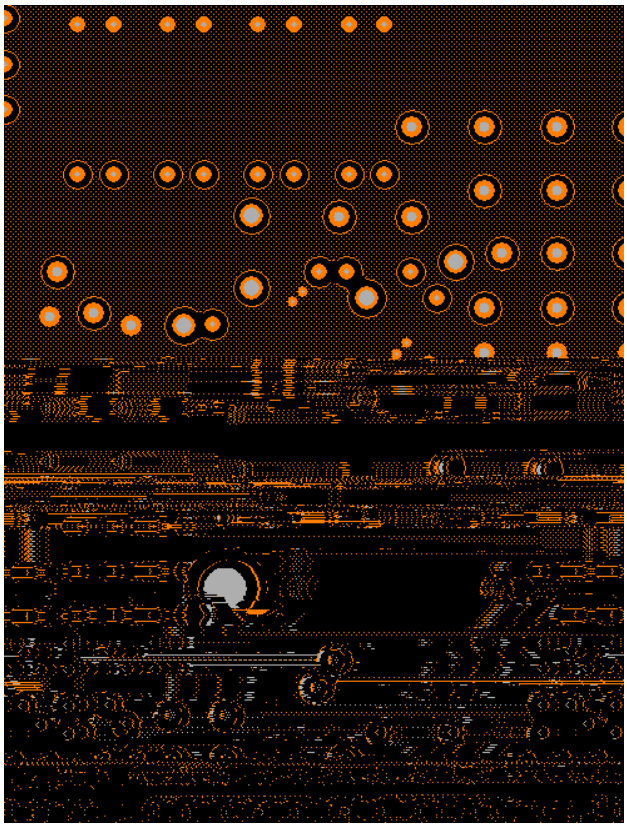


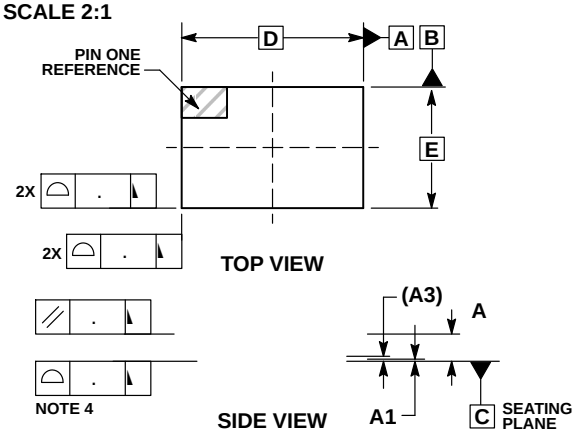
Figure 14. Layer 2 Copper Layer (Ground Plane)

QFN36 6x4, 0.4P
CASE 485DZ
ISSUE A

1 36

DATE 19 JUN 2015

SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.90	1.20
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	4.95	5.05

E	4.00 BSC	
E2	2.44	2.54

e	0.40 BSC	
G	0.52	0.62

*For additional information on our Pb−Free strategy and soldering details, please download the