



NCP81391, NCP81391A

Table 5. ELECTRICAL CHARACTERISTICS

($V_{VCC} = V_{VCCD} = 12\text{ V}$, $V_{VIN} = 12\text{ V}$, $V_{EN} = 5.0\text{ V}$, $C_{VCCD} = C_{VCC} = 0.1\text{ }\mu\text{F}$ unless specified otherwise) Min/Max values are valid for the temperature range $-40^{\circ}\text{C} \leq T_A \leq 100^{\circ}\text{C}$ unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
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PWM INPUT

Input Leakage	$I_{\text{PWM_LK}}$		–	–	5	μA
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HIGH SIDE DRIVER

Propagation Delay, PWM Falling	T
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Table 5. ELECTRICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

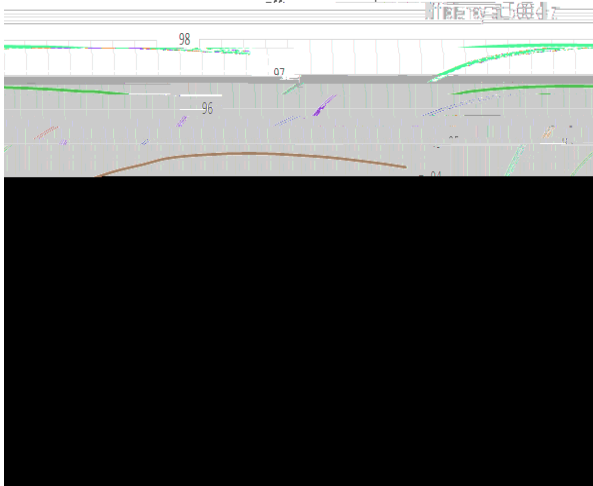


Figure 3. Efficiency – 12 V Input, 500 kHz

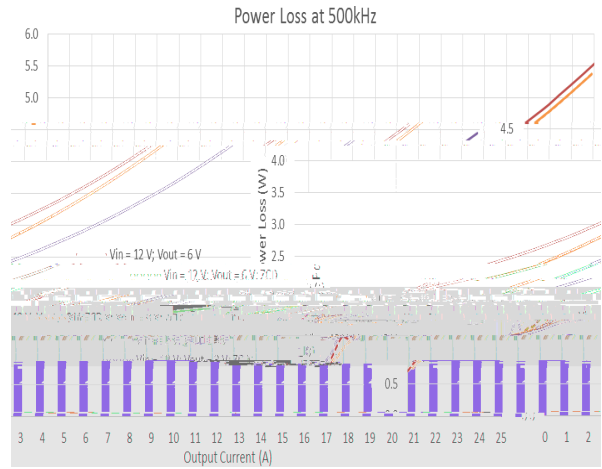


Figure 4. Power Loss – 12 V Input, 500 kHz

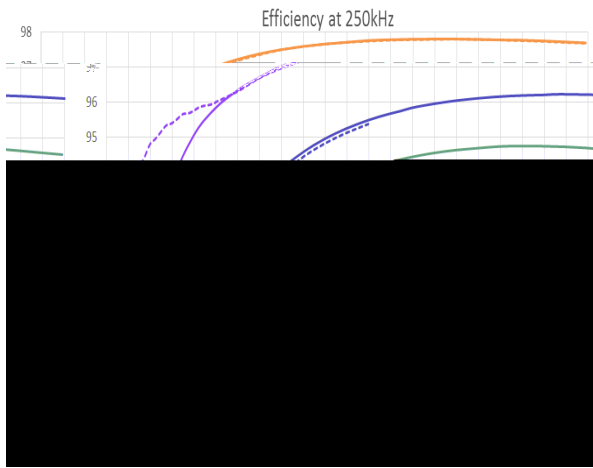


Figure 5. Efficiency – 12 V Input, 250 kHz



Figure 6. Power Loss – 12 V Input, 250 kHz

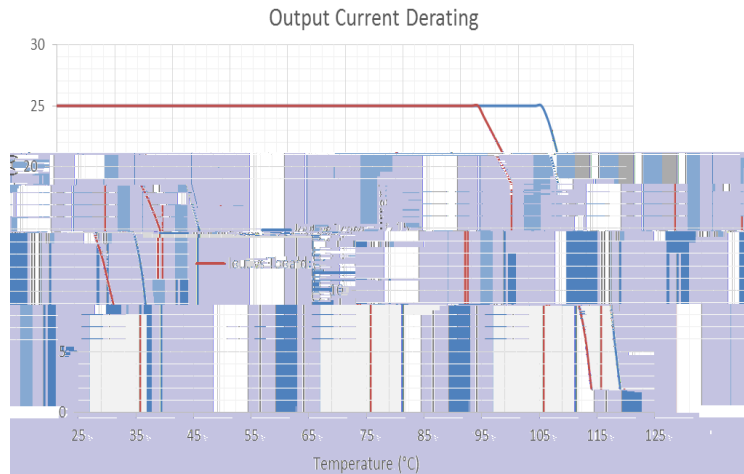


Figure 7. Output Current Derating
 $f_{SW} = 250 \text{ kHz}$; $V_{IN} = 12 \text{ V}$; $V_{CC} = V_{CCD} = 12 \text{ V}$; $V_{OUT} = 6 \text{ V}$; $L = 720 \text{ nH}$

APPLICATIONS INFORMATION

Theory of Operation

Low-Side Driver

The low-side driver drives a ground-referenced low- $R_{DS(on)}$ N-Channel MOSFET. The voltage rail for the low-side driver is internally connected to VCCD and CGND.

The GLD pin connects directly to the output of the low-side driver. The GLF pins connects directly to the gate of the low-side MOSFET. See Figure 2. GLD and GLF are not connected inside the package. For proper operation, these pins must be connected together on the PCB.

High-Side Driver

The high-side driver drives a floating low- $R_{DS(on)}$ N-channel

NCP81391, NCP81391A

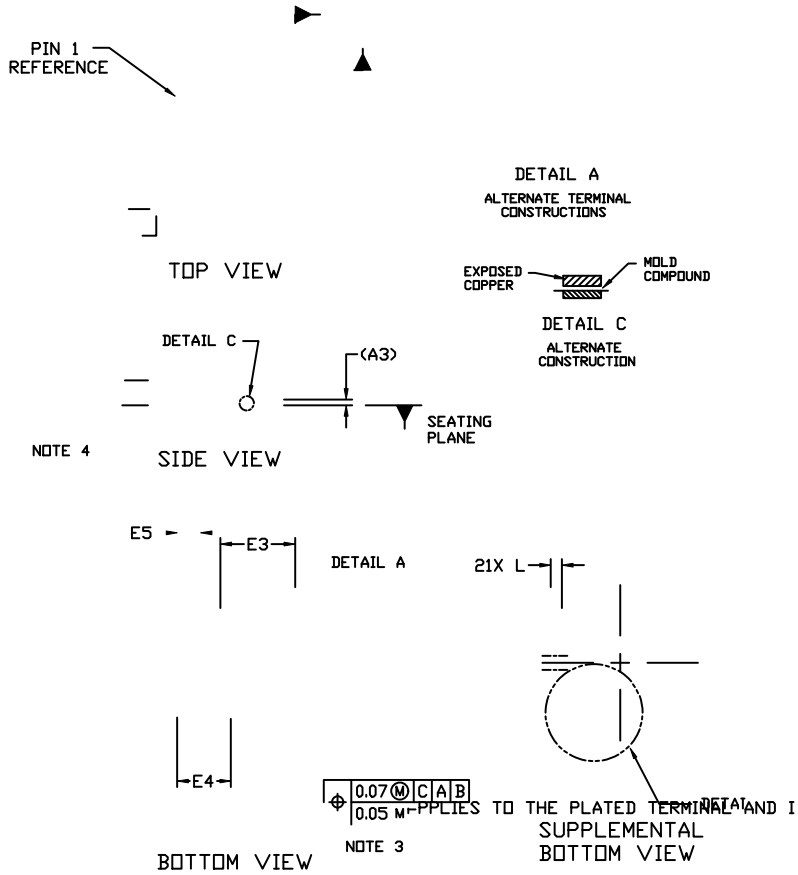
Power Supply Decoupling

The NCP81391/A sources relatively large currents into the MOSFET gates. In order to maintain a constant and stable input supply voltage, low-ESR capacitors should be

NCP81391, NCP81391A

QFN31 5x5, 0.5P
CASE 485FG
ISSUE A

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